TECHNICAL MANUAL

OPERATOR'S, ORGANIZATIONAL AND DIRECT SUPPORT MAINTENANCE MANUAL

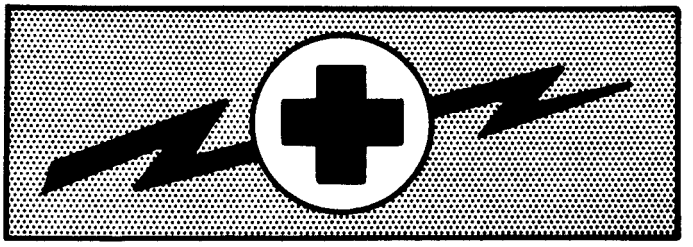
RADIO RECEIVER
(R-2081/TRQ-35(V))
MODEL RCS-4B
(NSN 5820-01-005-4247)

HEADQUARTERS, DEPARTMENT OF THE ARMY
30 AUGUST 1985

5 SAFETY STEPS TO FOLLOW IF SOMEONE IS THE VICTIM OF ELECTRICAL SHOCK

1. DO NOT TRY TO PULL OR GRAB THE INDIVIDUAL
2. IF POSSIBLE, TURN OFF THE ELECTRICAL POWER
3. IF YOU CANNOT TURN OFF THE ELECTRICAL POWER, PULL, PUSH OR LIFT THE PERSON TO SAFETY USING A WOODEN POLE OR A ROPE OR SOME OTHER INSULATING MATERIAL
4. SEND FOR HELP AS SOON AS POSSIBLE
5. AFTER THE INJURED PERSON IS FREE OF CONTACT WITH THE SOURCE OF ELECTRICAL SHOCK, MOVE THE PERSON A SHORT DISTANCE AWAY AND IMMEDIATELY START ARTIFICIAL RESUSCITATION

WARNING



HIGH VOLTAGE

is used in the operation of this equipment

DEATH ON CONTACT

may result if personnel fail to observe safety precautions

Never work on electronic equipment unless there is another person nearby who is familiar with the operation and hazards of the equipment and who is competent in administering first aid. When the technician is aided by operators, he must warn them about dangerous areas.

Whenever possible, the power supply to the equipment must be shut off before beginning work on the equipment. Take particular care to ground every capacitor likely to hold a dangerous potential. When working inside the equipment, after the power has been turned off, always ground every part before touching it.

Be careful not to contact high-voltage connections or 115 volt ac input connections when installing or operating this equipment.

Whenever the nature of the operation permits, keep one hand away from the equipment to reduce the hazard of current flowing through the body.

Warning: Do not be misled by the term “low volt age.” Potentials as low as 50 volts may cause death under adverse conditions.

For Artificial Respiration, refer to FM 21-11.

SAFETY SUMMARY

The following are general safety precautions that are not related to any specific procedures and therefore do not appear elsewhere in this publication. These are recommended precautions that personnel must understand and apply during many phases of operation and maintenance.

KEEP AWAY FROM LIVE CIRCUITS

Operating personnel must at all times observe all safety regulations. Unless specifically directed by this manual, do not replace components or make adjustments inside the equipment with any power supply turned on. Under certain conditions, dangerous potentials may exist in the power supplies when the power control is in the off position. To avoid casualties, always remove power and discharge and ground a circuit before touching it.

DO NOT SERVICE OR ADJUST ALONE

Under no circumstances should any person reach into or enter the enclosure for the purpose of servicing or adjusting the equipment except in the presence of someone who is capable of rendering aid.

RESUSCITATION - FIRST AID

Each person engaged in electrical operations will be trained in first aid, partitularly in the technique of mouth to mouth resuscitation and closed chest heart massage (FM 21-11).

The following warnings appear in this volume, and are repeated here for emphasis.

WARNING

A 3-wire (line, neutral, and safety ground) AC line power connection is required when operating the equipment. If a 3-wire safety grounded AC power receptacle is not available, a separate ground wire must be installed from the chassis ground to an earth ground. Without an adequate ground., the equipment chassis and frame will float to a dangerously high potential. (pages 2-6 and 3-8)

WARNING

In the performance of some maintenance procedures, it is necessary to have the equipment energized and dust covers removed. Extreme care must be exercised in making internal measurements or adjustments since potentially lethal voltages are present. (page 5-2)

WARNING

Use extreme care when making internal adjustments with power on. Potentially lethal voltages are present in the transmitter. (page 5-6)

WARNING

Use extreme care when making internal adjustments with power on. Potentially lethal voltages are present in the transmitter.

WARNING

GASES GENERATED BY CHARGING BATTERIES

Extreme caution must be taken when making connections for the purpose of testing, charging, or repairing batteries that are charging or have been recently removed from charging. Such batteries probably will be gassing and the slightest spark, caused by a short circuit, can cause the battery to explode. Personnel working with these batteries are urged to wear a pair of tight fitting goggles, or better still, the newer types of plastic mask which covers the entire face.

Open frames, cigarettes, radio transmitters, generating sets, open-cage electric motors, or any other type of equipment that may cause sparks, must be kept clear of the charging line.

WARNING

Lifting heavy equipment incorrectly can cause serious injury. Do not try to lift more than 35 pounds by yourself. Get a helper. Bend legs while lifting. Don’t support heavy weight with your back.

FOREWORD

Different versions of the RCS- 4B have been manufactured, are currently in use, and are described in this technical manual. Functionally and operationally, all versions are the same. The differences between versions are in parts selection, changes to circuit card assemblies, and the attendant changes to higher assembly part numbers. In most cases, two-way interchangeability is possible at the major component (unit) and module assembly level (paragraph 1-14).

Units and assemblies of the RCS-4B are differentiated either by serial number or part number. Early units and assemblies are serial numbered 400100 and before; later units and assemblies are serial numbered 400101 and on. In some later units, different part numbered assemblies are used.

Text paragraphs and figures are annotated to denote applicability y to particular serial or part numbered units and assemblies. The same notation is reflected in the table of contents and list of illustrations. Absence of a restrictive notation means the text/illustration applies to all versions of the RCS-4B.

Technical Manual

No. 11-5820-917-13

HEADQUARTERS
DEPARTMENT OF THE ARMY
Washington, DC, 30 August 1985

OPERATOR'S, ORGANIZATIONAL, AND DIRECT SUPPORT MAINTENANCE MANUAL
RADIO RECEIVER MODEL RCS-4B (R-2081/TRQ-35(V))
(NSN 5820-01-005-4247)

REPORTING ERRORS AND RECOMMENDING IMPROVEMENTS

You can help improve this manual. If you find any mistakes or if you know of a way to improve the procedures, please let us know. Mail your letter, DA Form 2028 (Recommended Changes to Publications and Blank Forms) , or DA Form 2028-2 located in back of this manual direct to: Commander, US Army Communications-Electronics Command and Fort Monmouth, ATTN: AMSEL-ME-MP, Fort Monmouth, New Jersey 07703-5007.

In either case, a reply will be furnished direct to you.

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SECTION 0

GENERAL

0-1. SCOPE. This manual covers Radio Receiver, R-2081/TRQ-35(V). The manual provides instructions for installation, operation, and maintenance for operator, organizational, and direct support repair personnel.

0-2. CONSOLIDATED INDEX OF ARMY PUBLICATIONS AND BLANK FORMS. Refer to the latest issue of DA Pam 310-1 to determine whether there are new editions, changes or additional publications pertaining to the equipment.

0-3. MAINTENANCE FORMS, RECORDS, AND REPORTS.

a. Reports of Maintenance and Unsatisfactory Equipment. Department of the Arm–y forms and procedures used for equipment maintenance will be those prescribed by DA Pam 738-750 as contained in Maintenance Management Update.

b. Report of Packaging and Handling Deficiencies. Fill out and forward SF 364 (Report of Discrepancy ROD)) as prescribed in AR 735-11-2/DLAR 4140.55/ NAVMATINST 4355.73A/AFR 440-54/MCO 4430.3F.

Discrepancy in Shipment Report (DISREP) (SF 361). Fill out and forward Discrepancy in Shipment Report (DISREP) (SF 361) as prescribed in AR 55- 38/ NAVSUPINST 4610. 33 C/AFR 75-18/MCO P461O.19D/DLAR 4500.15.

0-4. REPORTING EQUIPMENT IMPROVEMENT RECOMMENDATIONS (EIR). If your Radio Receiver R- 2081/TRQ-35(V) needs improvement, let us know. Send us an EIR. You, the user, are the only one who can tell us what you don't like about your equipment. Let us know why you don't like the design. Put it on an SF 368 (Quality Deficiency Report). Mail it to Commander, US Army Communications-Electronics Command and Fort Monmouth, ATTN: AMSEL-ME-MP, Fort Monmouth, New Jersey 07703-5007. We'll send you a reply.

0-5. ADMINISTRATIVE STORAGE. Administrative Storage of equipment issued to and used by Army activities will have preventive maintenance performed in accordance with the PMCS charts before storing. When removing the equipment from administrative storage the PMCS should be performed to assure operational readiness. Disassembly and repacking of equipment for shipment or limited storage are covered in paragraph 2-27.

0-6. DESTRUCTION OF ARMY ELECTRONICS MATERIEL. Destruction of Army electronics materiel to prevent enemy use shall be in accordance with TM 750-244-2.

SECTION 1

GENERAL INFORMATION

1-1. INTRODUCTION

1-2. This manual provides operating and service instructions for the RCS-4B Receiver. The information is presented in seven sections. Section 1 provides a brief description of the equipment and operating specifications. Unpacking instructions, site requirements, cabling data, and installation instructions are included in Section 2. Section 3 provides operator controls and indicator information and describes operating procedures. In Section 4 are functional descriptions of receiver circuits. Section 5 describes preventive and corrective maintenance procedures for the receiver and provides a performance verification test. Section 6 contains the wire lists for reference during maintenance. All oversize drawings, such as schematic diagrams, are grouped at the back of this manual as foldout sections. Section 7 presents procedures for managing HF circuits using the supplied equipment.

1-3. GENERAL DESCRIPTION

1-4. The RCS-4B receiver (figure 1-1) is one part of an HF Radio Sounder Set (also designated the TFMS) used for frequency management of HF radio circuits. It is a sweeping HF receiver that tunes through the HF spectrum at a 50-kHz per second or 100 - kHz per second rate beginning at 2 MHz. When synchronized with a TCS-4B transmitter located at the other end-of an HF circuit, the receiver provides a measurement of ionospheric propagation conditions for the circuit. A TCS-4B transmitter at one end of the HF circuit emits a CW signal which starts at 2 MHz and sweeps upward in frequency at a constant linear rate (50 kHz /second for a 2-16 MHz sweep; 100 kHz/second for a 2-30 MHz sweep.) An internal clock in the RCS-4B receiver starts the receiver sweep synchronously with the transmitter and precisely tracks the sweeping transmitter signal. Any radio frequency that can propagate over the HF circuit is received by the RCS-4B. The radio energy propagates by various modes (e. g. surface wave, one- hop, t we-hop, etc.) which have different propagation delays. The time delay created by the travel of the RF signals from the transmitter to the ionosphere and to the receiver causes the ionospherically returned signal to arrive "late" or slightly behind the exact tuned frequency of the receiver. That is, since the transmit and receive sweeps are started at exactly the same time, the receiver sweep has advanced to a slightly higher frequency by the time the transmit signal arrives at the receiver. Thus, the receiver is tuned to a slightly different (higher) frequency than the arriving transmit signal. This received frequency difference is amplified in the receiver IF and converted to a “baseband audio” tone. A tone at zero hertz indicates no time delay and tones of increasing audio frequency (up to 500 Hz) indicates increasing time delay of the ionospherically returned signal. In practice, multiple tones are present in the sounder’s baseband audio output which represent the various delays caused by the different layers, or modes, of the ionosphere. These multiple tones are processed by the sounder's spectrum analyzer to separate the tones into discrete components which identify corresponding ionospheric modes. A speaker and headphone jack are provided for audio monitoring. The output spectrum analyzer is displayed on the 6025 CRT display versus the RF sweep of the sounder. The CRT vertical axis indicates received

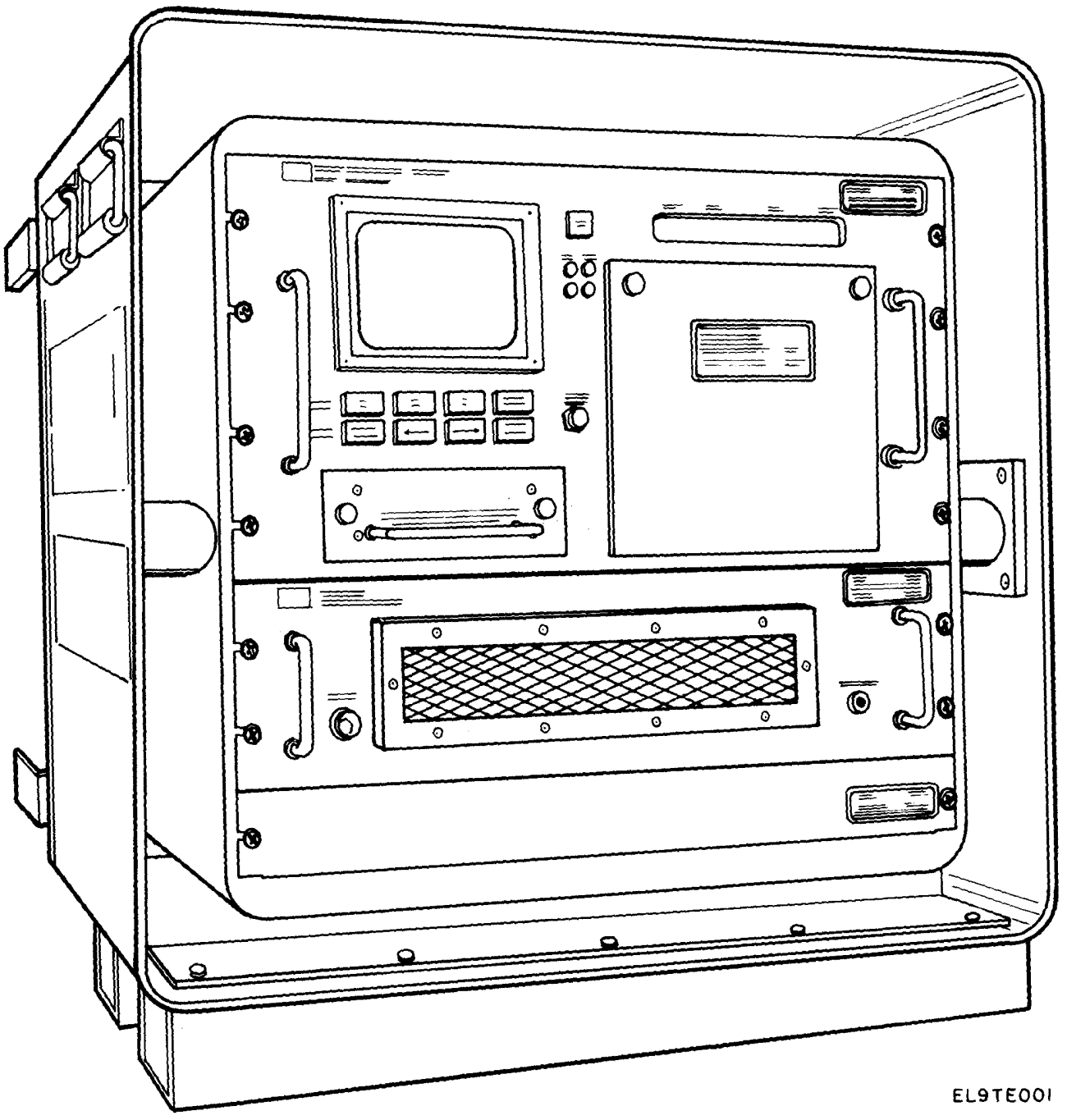


FIGURE 1-1. RCS-4B Receiver.

signal time delay (ionospheric mode structure) versus the CRT horizontal axis of radio frequency; 2-16 or 2-30 MHz. The result is a display of propagating modes versus frequency, referred to as a Chirp sounder record (or ionospheric sounding) as shown in figure 1-2. In addition, as radio energy at various levels is received, the receiver gain is automatically adjusted to provide a constant level output to the spectrum analyzer. The automatic gain control (AGC) voltage versus radio frequency provides a measure of received signal strength vs frequency which is also displayed on the CRT (refer to top of figure 1-2) . Thus, the receiver operating at one end of a radio circuit in association with a transmitter at the other end of the circuit provides a real-time measurement of propagation conditions on the circuit. The receiver is designed to be synchronized with up to three different TCS-4B transmitters and can receive transmissions from one of the three transmitters every five minutes. The latest Chirpsounder record for each of the three circuits is stored in memory within the receiver and can be displayed at any time upon operator command.

1-5. The RCS-4B receiver consists of three units. Unit 1, the 6025 control display unit contains the internal clock and control circuits of the receiver, the spectrum analysis, and CRT display. Unit 2, the 4028 HF receiver, contains the radio receiver, sweeping frequency synthesizer and power supply. Unit 3, the 6043 power divider, contains three, 4-way power dividers that allow the RCS-4B to share up to three antennas (one for each path) with other HF receiving equipment, for example, an RSS-4 Spectrum Monitor and two HF communications receivers. Each of the three power dividers has one input (from an antenna) and four outputs (to the receivers) . One output of each power divider is prewired to one of the three RCS-4B inputs.

1-6. Unit 1, 6025 CONTROL/DISPLAY. The 6025 Control/Display unit contains electronics assemblies required to perform the following functions:

a. Provide accurate timing for each of three clocks used to maintain synchronization with up to three TCS-4B transmitters (each clock referenced to an oven-stabilized crystal oscillator with 5 MHz output drifting less than 5 parts in 10^{-9} per day) ;

b. Select the transmitter to be received during any of twelve 5-minute periods each hour:

c. Automatically lock onto, and synchronize with, each transmitter provided the receiver's sweep tuning is started within ± 1 second of transmitter sweep;

d. Control the sweeping frequency synthesizer used as the receiver's first local oscillator;

e. Spectrum analyze the receiver output and store in memory the spectra vs tuned frequency that results from receiving each propagating mode:

f. Display via a CRT upon operator command the latest Chirpsounder record and received signal strength versus frequency data for each of the three paths;

g. Provide a standby battery supply to maintain the three path clocks for up to 24 hours (at 23° C) in event of a primary AC line failure;

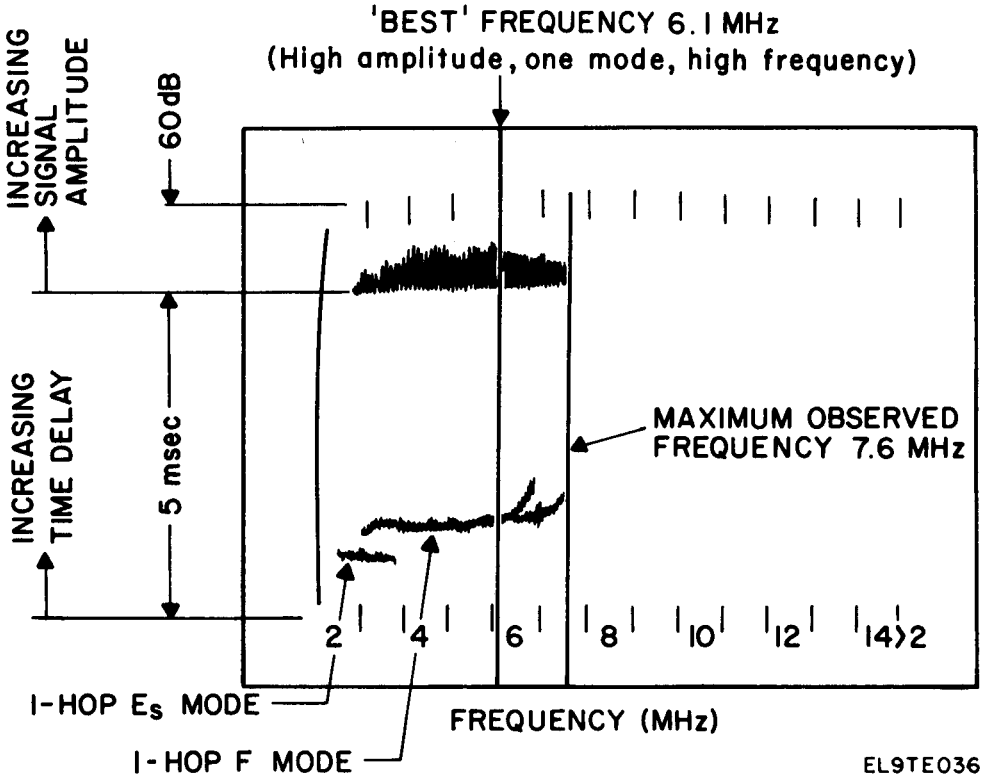


FIGURE 1-2. Example of RCS-4B Chirpsounder Record, 2-16 MHz Range, Path 2.

h. Provide a digital display of the actual frequency being received; and,

i. Provide self-test circuits and display to determine a go/no-go condition of the receiver power supplies, receiver sensitivity, proper synthesizer operation, and standby power supply voltage.

1-7. Unit 2, 4028 HF RECEIVER. The 4028 consists of a frequency synthesizer, an HF radio receiver, and power supply. The frequency synthesizer generates a precision frequency spectrally pure output signal, 40.2 MHz above the desired received frequency which is used for the HF receiver first mixer LO injection. The synthesizer frequency is programmed by digital control circuits and is phase-locked to an oven-enclosed 5 MHz crystal oscillator in the 6025 unit.

1-8. The receiver assembly mixes the sweeping first local oscillator signal from the frequency synthesizer with the input as selected from one of three antenna sources. The result is a 40.2 MHz first intermediate frequency (IF) which is crystal-filtered to provide a 10-kHz bandwidth. A 40-MHz second local oscillator and mixer converts the first IF to a 200-kHz second IF which is further bandwidth-limited to approximately 500 Hz by a second crystal filter. The receiver's AGC circuit seeks to maintain a constant amplitude second IF output which is then mixed with a 200-kHz third LO signal to provide a 0-500 Hz baseband audio output.

1-9. The receiver has a calibrator circuit for testing receiver sensitivity y. When the test function is initiated, this circuit injects a low level sweeping RF signal into the receiver input that produces a 350 Hz tone in the receiver output. The presence of this tone in the spectrum analyzer output verifies proper receiver operation. The front end of the receiver also supplies up to 30 dB antenna input attenuation, operator selected in 10 dB steps. Half-octave preselection filters in the receiver front end reduce the potential interference effects of high level out-of-band signals. A speaker and headphone jack are also provided enabling the operator to listen to the receiver's audio output.

1-10. The power supply for the RCS-4B receiver is contained within the 4028. This supply is a linear, series regulated solid state supply providing +5, +12, -12, and +24 VDC .

1-11. Unit 3, 6043 POWER DIVIDER. The power divider consists of three 4-way power dividers that can be connected to each of three broadband antennas. One output of each power divider goes to the corresponding antenna input of the 4028 receiver. The other three outputs of the power dividers are available for antenna connection to communication receivers. Because of the antenna sharing technique, the ionospheric sounding obtained by the RCS-4B accounts for receive characteristics of the antenna used by the communication receivers.

1-12. EQUIPMENT SUPPLIED

1-13. As supplied, the RCS-4B receiver includes the following standard items:

Control/Display, Unit 1	P/N 6025-1000
HF Receiver, Unit 2	P/N 4028-1000 or 4028-1100
Power Divider, Unit 3	P/N 6043-1000

Interconnecting Cables and Power Cable	Refer to Table 2-1
Environmental Case	P/N 6000-3110-1

1-14. An RCS-4B may be supplied with a Unit 2, HF Receiver either part number 4028-1000 or 4028-1100. These units are fully two-way interchangeable, and the different part numbered module within the units is also two-way interchangeable. The different part-numbered module in the 4028 unit is Sweep Synthesizer Assy, either 5030-1001 or 5030-1101.

1-15. Unit 1, 6025-1000, of the RCS-4B may include a standby battery supply assembly that is either a rechargeable type (P/N 6025-1018) or non-rechargeable type P/N 6025-1008). These different part numbered assemblies are not interchangeable. Specific information on the battery supply is provided in paragraph 2-21 and 4-53.

1-16. AIRCRAFT INSTALLATIONS. For airborne applications, the RCS-4B is supplied with a special aircraft installation kit. Aircraft installation using this kit is described in paragraph 2-10.

1-17. EQUIPMENT REQUIRED BUT NOT SUPPLIED

1-18. The RCS-4B receiver requires an antenna capable of efficiently receiving HF signals from 2 to 30 MHz. Best measurement results will be obtained if the RCS-4B receiver uses the same antenna as is used for the communication receivers. The 6043 power divider (supplied with the RCS-4B) provides for connection to three antennas with power divided to the RCS-4B and up to three communication receivers. The RCS-4B accepts a 50-ohm unbalanced signal input. If a balanced feed antenna is used, a suitable receive balun should be installed. Test equipment required for fault isolation and servicing of the receiver is listed in table 5-1.

1-19. SPECIFICATIONS

1-20. Table 1-1 lists the performance specifications for the RCS-4B receiver. Performance data are base-d on the standard system configuration.

1-21. RELATED PUBLICATIONS

1-22. Information in the following publications is relevant to operation and service of the receiver.

Title	Document number
Illustrated Parts Breakdown, RCS-4B Receiver	TM 11-5820-917-23P
Operation and Service Instructions TCS-4B Transmitter	TM 11-5820-918-13

Table 1-1. Specifications

Frequency Range (Sweep Limits)	2-16 MHz and 2-30 MHz, selectable by front panel switch
Input Waveform	Linear FM/CW
Sweep Rates	50 kHz/sec in 2-16 range. 100 kHz/sec in 2-30 MHz range
Operating Times	Automatic sweep start at any of 12 times spaced 5 minutes apart, each hour, for any of three paths. Sweep can be manually initiated, terminated, or reset at any time.
Long-Term Timing and Frequency Accuracy	Less than 5×10^{-9}/24 hours after 12 hours warmup
Standby Power	24 hours, minimum, for timing circuitry (at 23°C)
Sweep Linearity	Sufficient to obtain a nominal 100 microsecond or better time-delay resolution
Time Delay Window	5 msec (100 kHz/see sweep); 10 msec (50 kHz/sec sweep) ±5%
Time Delay Resolution	100 microseconds nominal, (50 kHz/sec sweep)
Synchronization	Manual/automatic search and lock-on of signal when receiver is started within ±1.0 second of the transmitter.
Manually Controlled Timing Slip	50, 10, or 1 msec/sec advance or retard, independent for each of three paths
RF Signal Level Display	CRT bargraph of received signal power over 55 dB range (±5 dB) starting from -120 dBm (excluding 6043 loss) versus frequency.

Table 1-1. Specifications - Continued

Chirp Propagation Display	Three digitally stored CRT graphic displays presenting time delay versus frequency of the sounded path's propagation.
Antenna Input	50 ohms, nominal, unbalanced
Baseband Audio Output	1-volt rms into 1000 ohms (for magnetic tape recorders)
Receiver Sensitivity	Minimum detectable Chirp signal on CRT display: -130 dBm into 6043 -137 dBm into 4028
Path Clock Output	TTL level, one pulse per second, selected by front-panel mode switch
Primary Power	115 or 230 VAC ± 10%, 47-440 Hz, 360 watts
Temperature	O to 50°C operating; -40 to +71°C non-operational and storage
Relative Humidity	Up to 85% operating; up to 96% non-operating and storage
Chirpsounder Record Data Output (S/N 400101 and on).	Outputs for external processor analysis of Chirp sounder record
Dimensions	See figure 2-1.
Weight	260 lbs (118 kg)

SECTION 2

INSTALLATION

2-1. INTRODUCTION

2-2. This section contains instructions for installing the receiver and for making all necessary cable interconnections before putting the system into use. Details on storage and reshipment are also included.

2-3. UNPACKING AND INSPECTION

2-4. The receiver is shipped from the factory in a fully assembled condition within its environmental protective case for shipment. It is enclosed in a moisture-resistant barrier material with desiccant and humidity indicator packed in a wooden box. The gross weight of the receiver in its shipping container is 371 pounds. When removed from the shipping container, the receiver weighs 260 pounds and should be transported by forklift to its operating site.

NOTE

The receiver case is marked to indicate position for the lifting forks.

The shipping container should be inspected for external damage, and if damage is evident, the carrier should be notified.

2-5. To unpack the RCS-4B, remove the top of the shipping container. Care should be exercised in removing nails and wood panels since the container is reusable. Roll the shipping container over so the top is on the bottom. Lift the container straight up off the RCS-4B. The receiver (now upside down) should be rolled upright. Check all items against the packing list. The shipping container and associated packing material should be retained for possible use in reshipment or storage of the receiver.

2-6. INSTALLATION REQUIREMENTS

2-7. GENERAL. The receiver operates satisfactorily within temperature limits of O to +50C and up to 85% non-condensing relative humidity. For long term operational stability, the equipment should not be exposed to excessive shocks (exceeding 15 g's), high dust levels or extreme fluctuations in temperature. The receiver has internal-mounted cooling fans with intake air filters on the front of the 4028 unit and on the rear of the 6025 unit. Adequate clearance must be allowed for the free flow of air.

2-8. RACK MOUNTING. All units have front panels designed for standard 19-inch rack mounting. If rack mounted, the units should be adequately supported by either rack slides or weight supporting brackets mounted between the rack and the rear of the units. Refer to figure 2-1 for suggested mounting details.

2-9. BENCH MOUNTING. For bench mounting, the units may be mounted one above the other, or side by side, within the limits of the cable lengths supplied. When mounted one above the other, the two units require a suitable packing shim (approximately 1/2 inch thick) to maintain proper alignment of the front panels.

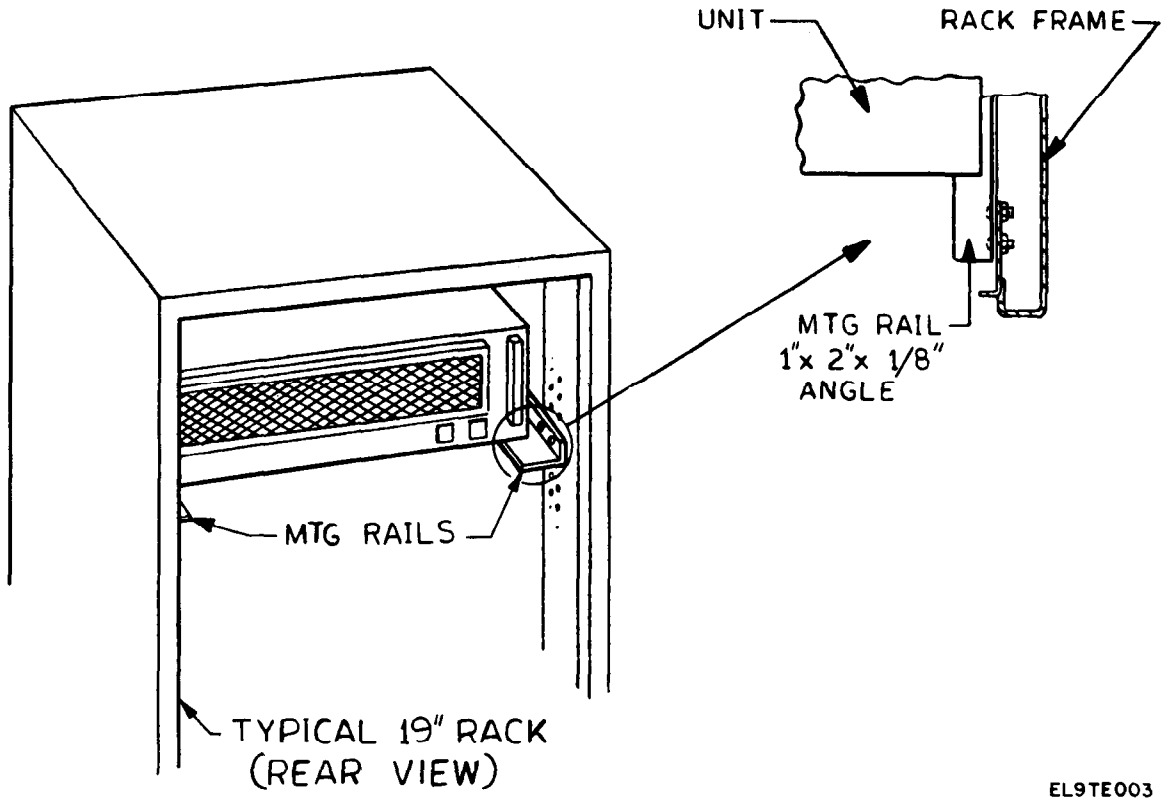


FIGURE 2-1. Rack Mounting.

2-10. AIRCRAFT INSTALLATION. The Aircraft Installation kit (part number 9125-1907) is primarily designed to assist installation of a RCS-4B Receiver in an E3A AWACS aircraft and is typical for other installations. The kit consists of an RF power divider, a 25W 10-dB attenuator (pad), a 30-MHz low pass filter, and cables. Figure 2-2 is the block diagram of a typical installation. The power divider must be connected as close as possible to an aircraft receive-only antenna. No active or passive filter elements should be between the antenna and the power divider. The antenna input coax should be disconnected from the existing receive system and attached to Port A of the power divider. Connector adapters are provided. The aircraft receive system should be connected to Port C; the Chirp sounder receiver to Port D. A 50-ohm termination is provided for Port B.

2-11. A 25-watt 10-dB attenuator is provided to reduce the possible effects of any RF energy picked up from an aircraft transmit antenna. This attenuator and the power divider should be secured to the aircraft structure. A long (approximately 50- foot) coax cable links the power divider and attenuator to a low pass filter which can be secured anywhere near the RCS-4B receiver. The filter, with a 30 MHz upper frequency limit, attenuates RF above the VHF band.

2-12. The aircraft installation kit P/N 9125-1907, consists of the following items which are keyed to figure 2-2.

Item	Qty	BR part number	Item
1	1	0950-8383	Power Divider, 2 way
2	1	0951-0035	Low Pass Filter, 30 MHz
3	1	0950-0049	Attenuator, 25 W, 10 dB
4	1	0950-8080	Resistor, RF Termination, 25 W 50 ohm
5	2	8120-2006-12	Cable Assy, N to N
6	1	8120-2006-600	Cable Assy, N to N
7	1	8120-2006-36	Cable Assy, N to N
8	1	8120-2006-36	Cable Assy, TNC to N
9	1	1250-0066	Adapter, Connector, TNC/N

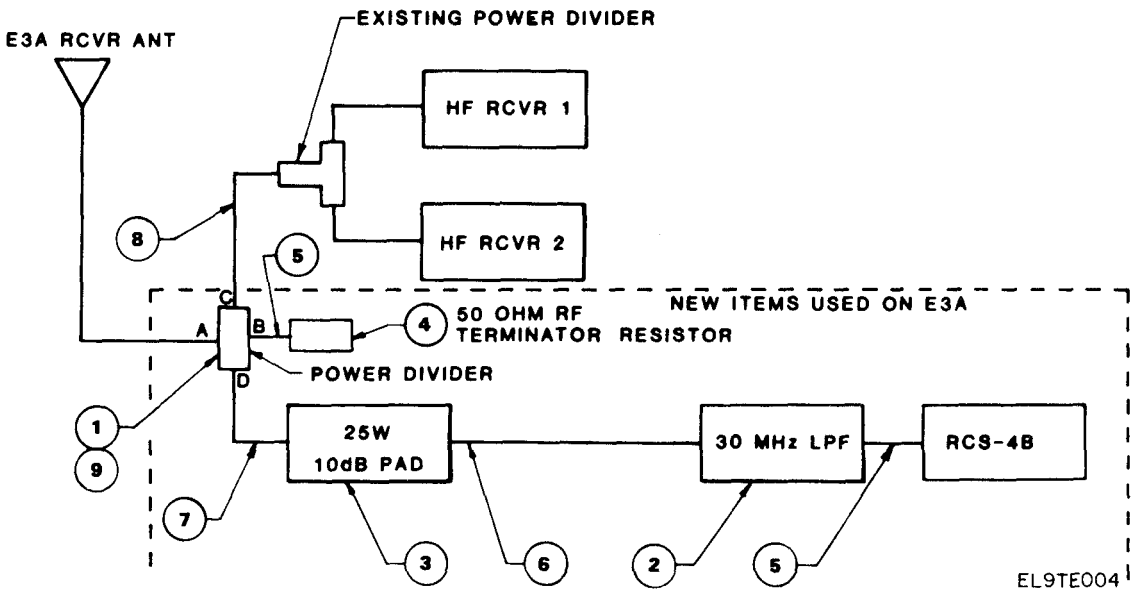
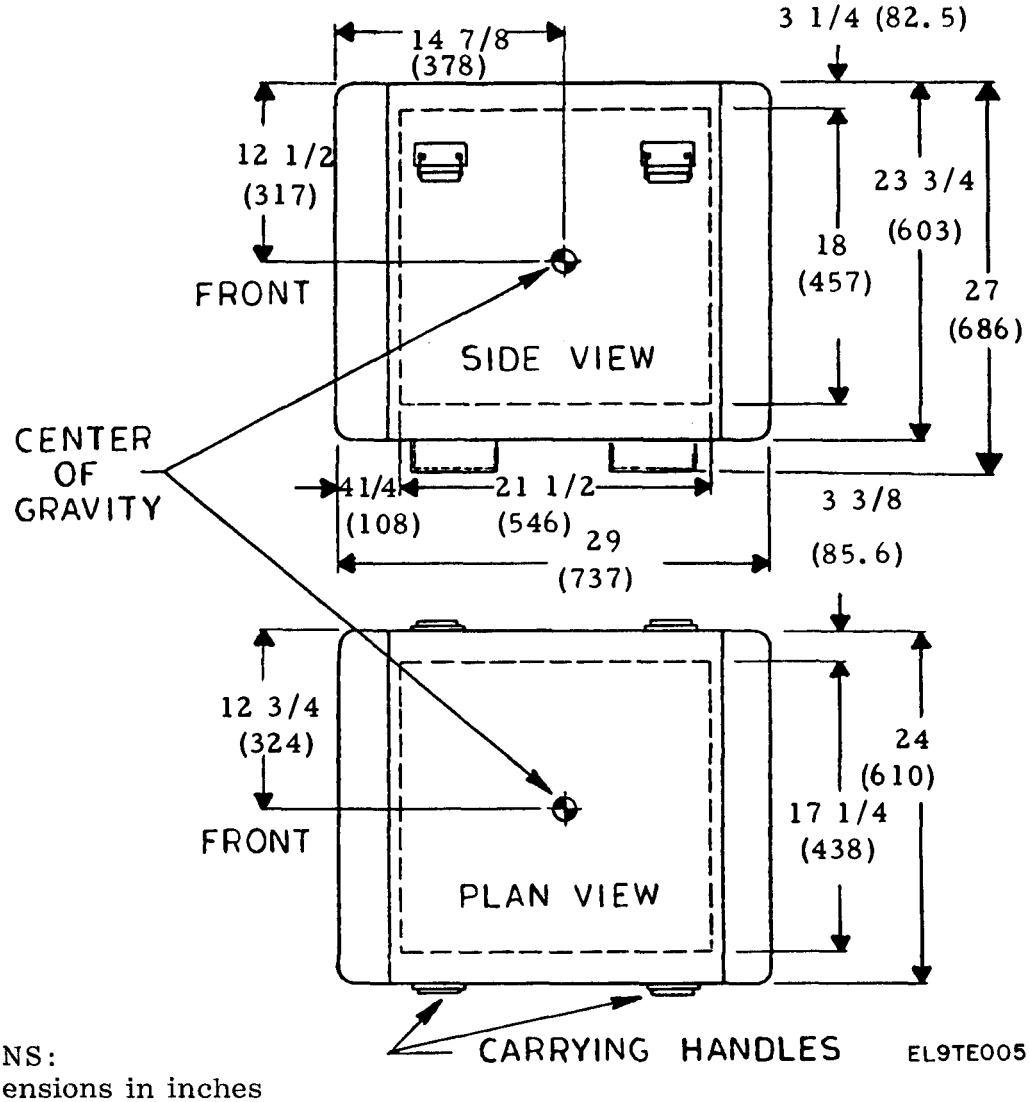


FIGURE 2-2. Typical Equipment for Aircraft Installation.

2-13. ENVIRONMENTAL CASE ENCLOSURE. The RCS-4B receiver is supplied in an environmental case. This configuration is particularly suitable for shock or vibration prone environments. The container comes complete with four carrying handles; however, because of the weight of the assembled receiver, a forklift should be used or the modular units removed from the case before moving the receiver. Front and rear doors on the case remove easily for access to equipment. The external dimensions and weight of the unit are shown on figure 2-3.

2-14. POWER CONNECTION

2-15. LINE VOLTAGE. The receiver may be operated from either 115 or 230 volts (±10%), 47 to 440 Hz power lines. A toggle switch mounted in the 4028 unit adjacent to the power transformer (figure 2-4) permits easy conversion for either voltage. Access to the switch is obtained by removing the top cover of the 4028 unit.



DIMENSIONS:
All dimensions in inches
and (millimeters)

SHIPPING DIMENSIONS (with environmental case):

Width: 24,0 inches (610 mm)

Depth: 29.0 inches (737 mm)

Height: 27.0 inches (686 mm)

VOLUME: 10.88 cu. feet (0.31 cu. meters)

SHIPPING VOLUME: 24.45 cu. feet (0.69 cu. meters)

WEIGHT: 260 lbs. (117.9 kg)

SHIPPING WEIGHT: 371 lbs (168.2 kg)

FIGURE 2-3. Receiver Outline Dimensions.

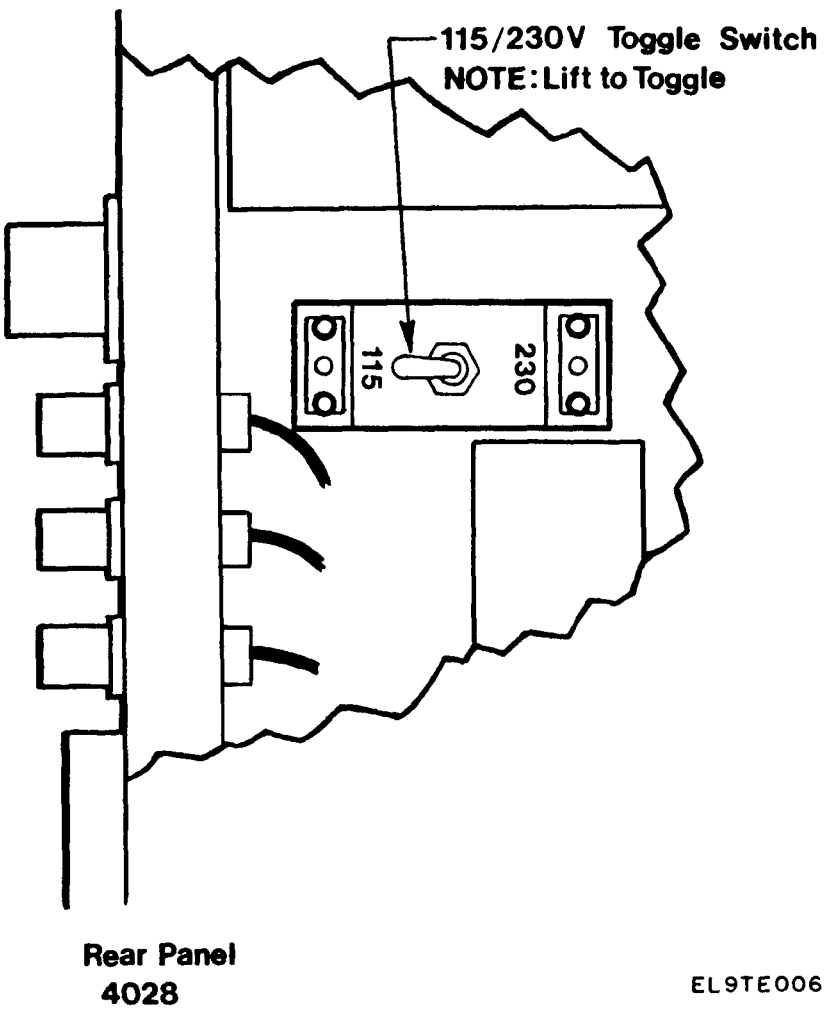


FIGURE 2-4. Power Supply Line Voltage Switch.

WARNING

A three-wire (line, neutral, and safety ground) AC line power connection is required when operating the equipment. If a 3-wire safety grounded AC power receptacle is not available, a separate ground wire must be installed from the chassis ground to an earth ground. Without an adequate ground, the equipment chassis and frame will float to a dangerously high potential.

NOTE

Before connecting AC power to unit, be sure the correct fuse is installed (4A for 115V, and 2.0A for 230V), and toggle switch (as marked on 4028 chassis) is in correct position.

2-16. POWER CABLE. The receiver is provided with a detachable line cord (10 feet long) having a standard EIA 5-15P, 15-ampere plug (2 blades with round grounding pin) at the supply end. Exposed portions of the equipment are grounded through the round pin of the plug for safety. A non-grounding two blade receptacle should not be used without use of a grounding type connector adaptor.

2-17. CABLES AND CONNECTORS

2-18. A list of cables used with the receiver are given in table 2-1. Connectors used are given in table 2-2. All connections are made at the rear of both units and are illustrated in figure 2-5.

2-19. Antenna connections to the RCS-4B (to either the 6043 power divider or directly to the 4028 inputs) are type N coaxial connectors requiring a mating antenna cable plug (type N) such as UG-21, UG-1185, or UG-536.

2-20. DATA I/O CONNECTOR. The remote data output connector J7 on the 6025 rear panel is a 12-pin circular connector (Amphenol 348-40E10-12S1) which mates with an Amphenol 348-46E10-12P1 cable plug or a MIL-C-81511 plug part number M81511/06EB01P1. Signals available on J7 allow data collection and processing of RCS-4B sounder data by external equipment such as the BR Frequency Management Terminals (FMT series) . For further information on the use of the remote data outputs contact BR communications. The pin out connections of J7 are listed in table 2-3.

2-21. BATTERY INSTALLATION

2-22. Two different types of standby battery supplies are used in the RCS-4B . Some receivers have a non-rechargeable battery supply (P/N 6025- 1008) that uses standard D-cell batteries. Other receivers have a rechargeable supply (P/N 6025-1018) that includes an integral charging circuit and uses sealed lead acid cells. Refer to either paragraph 2-23 or 2-24 as applicable.

Table 2-1. Interconnect Cables

Cable designation and BR part number	From	To	Remarks
W1 8120-4002-54	1J2	2J5	Control Signals from 6025 to 4028
W2 8120-2004-48	1J3	2J4	5 MHz signal from 6025 to 4028
W3 8120-2004-48	2J8	1J4	Synthesizer Count Signal to 6025 from 4028
W4 8120-5004-54	2J6	1J1	D.C. Power Supplies from 4028 to 6025
W5 8120-0203-120	A.C. Power	2J7	A.C. Line In to 4028
W6 8120-2006-36	3J1A	2J1	Antenna 1 from 6043 to 4028
W7 8120-2006-30	3J2A	2J2	Antenna 2 from 6043 to 4028
W8 8120-2006-24	3J3A	2J3	Antenna 3 from 6043 to 4028

Table 2-2. Connectors

Connector	Part no.	Name	Description
1J1	MS3102A-24-28P	D.C. Input (from 4028)	24 Pin Receptacle
1J2	348-40E14-37S1	Control	37 Socket Receptacle
1J3	28JS-129-3	5MHZ out	Coaxial Connector, BNC, Jack, Female
1J4	28JS 145-2	L.O. In	Coaxial Connector, BNC, Jack, Female
1J5	28JS 145-2	1 PPS	Coaxial Connector, BNC, Jack, Female
2J1	21850	Antenna Input 1	Coaxial Connector 'N' Type Receptacle

Table 2-2. Connectors - Continued

Connector	Part no.	Name	Description
2J2	21850	Antenna Input 2	Coaxial Connector 'N' Type Receptacle
2J3	21850	Antenna Input 3	Coaxial Connector 'N' Type Receptacle
2J4	28JS 129-3	5 MHz In	Coaxial Connector, BNC, Jack, Female
2J5	348-40E14-37S1	Control	37 Socket Receptacle
2J6	MS3102A-24-28S	D. C. Power	24 Socket Receptacle
2J7	MS3102A-16-10P	A.C. Line Input	3 Pin Power Receptacle
2J8	28JS-145-2	L.O. Out	Coaxial Connector, BNC, Jack, Female
3J1A	36000	ANT 1 Divider Output A	Coaxial Connector, 'N' Type Receptacle
3J2A	36000	ANT 2 Divider Output B	Coaxial Connector 'N' Type Receptacle
3J3A	36000	ANT 3 Divider Output C	Coaxial Connector 'N' Type Receptacle
3J1	36000	IN ANT 1	Coaxial Connector 'N' Type Receptacle
3J2	36000	IN ANT 2	Coaxial Connector 'N' Type Receptacle
3J3	36000	IN ANT 3	Coaxial Connector 'N' Type Receptacle

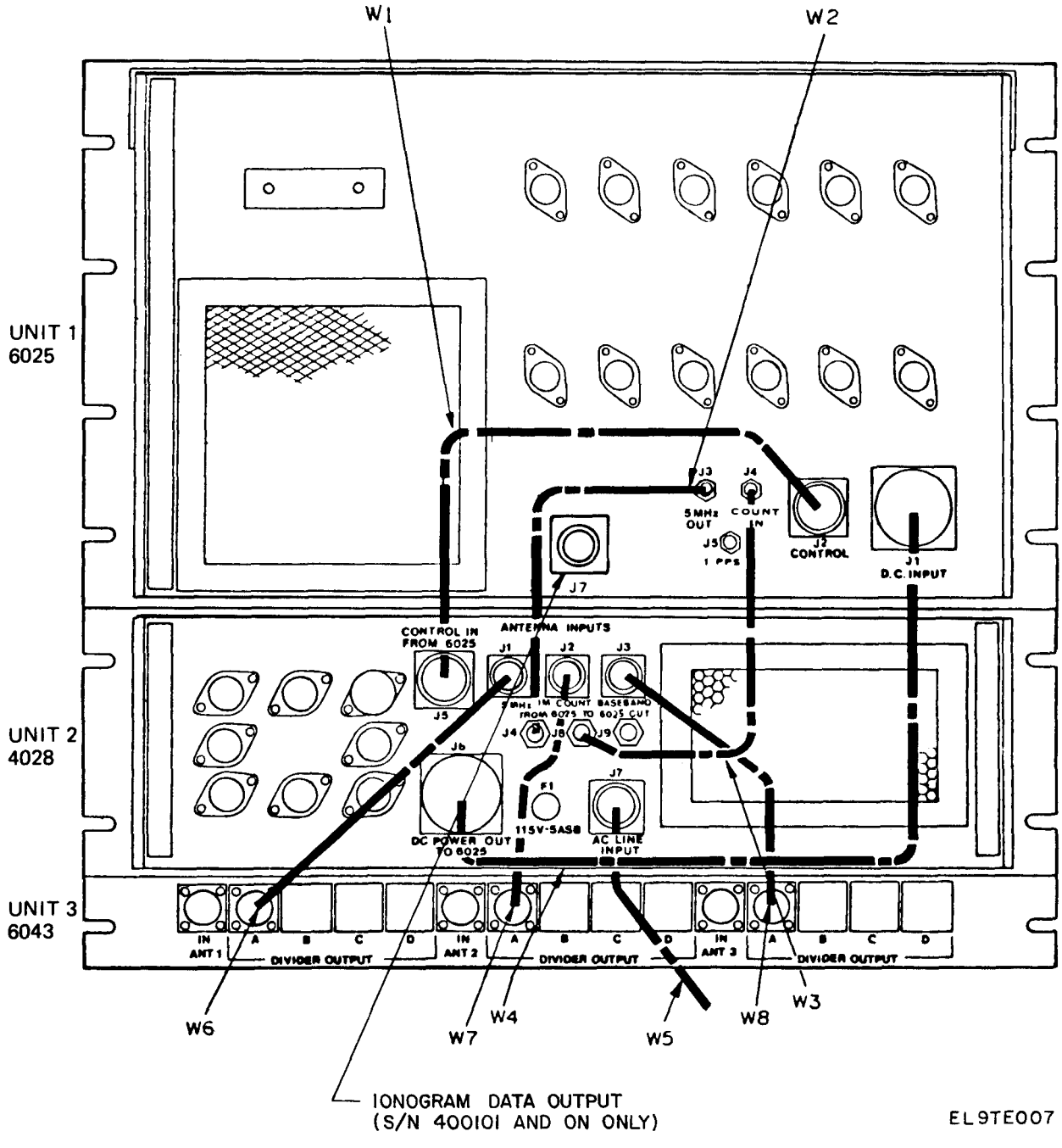


FIGURE 2-5. Receiver Interconnect Cabling.

Table 2-3. Remote Data Output Connector

Pin number	Function
J7-1	Ground
J7-2	S/A Sync, TTL Low = Scan
J7-3	S/A Spectrum Out (O to 5V analog)
J7-4	S/A Clock (3.3 kHz)
J7-5	Sweep Run/Stop (SRS) TTL Hi = sweeping
J7-6	Receiver AGC Voltage (O to 5V analog)
J7-7	Upper Frequency Limit (UFL) , TTL Low = 30 MHz TTL Hi = 16 MHz
J7-8	Path 1, TTL low = Path 1 Sweep in Progress
J7-9	Path 2, TTL low = Path 2 Sweep in Progress
J7-10	Path 3, TTL low = Path 3 Sweep in Progress

2-23. NON-RECHARGEABLE BATTERY SUPPLY (P/N 6025-1008). The standard D-cell batteries may or may not be installed in the receiver on arrival, depending on shipping destination and enroute climate, etc. With new batteries installed, the standby supply provides operating power for up to 24 hours (at 23°C). To install batteries, proceed as follows:

a. Loosen two captive thumbscrews at front of battery drawer on 6025 front panel.

b. Pull out battery drawer entirely.

c. Remove two screws at top rear of container and slide battery cover out from rear.

d. If existing batteries are being replaced, pry center front contact spring back and remove center tube. Repeat for other two tubes.

e. Replace all batteries in + to - sequence and re-insert each tube according to polarity markings on base of container.

2-24. RECHARGEABLE BATTERY SUPPLY (P/N 6025-1018). The rechargeable battery supply is installed for shipment in a drawer located in the front panel of the 6025 unit. Since the battery supply may have discharged during shipment, battery power should not be relied on for the first 12 hours of operation. An internal charging circuit maintains a continuous charge on the battery supply when AC line power to the 6025 is on. After a 12 hour charge (with the 4028 power turned on), the battery pack provides

standby power for up to 24 hours (at 23°C). Refer to paragraphs 3-16 and 3-17 for additional information.

2-25. POST-INSTALLATION CHECKOUT

2-26. The electrical performance of the receiver should be verified before being put into normal operation. The performance test described in section 5 is performed as the post-installation checkout and prior to operation.

2-27. STORAGE AND RESHIPMENT

2-28. STORAGE. The maximum recommended storage conditions should not exceed -40 to 71°C temperature to 96% humidity. For long term storage, repackaging of the equipment and sealing of the cables in moisture-proof bags are recommended. The shutdown and storage procedures of paragraph 3-16 or 3-17 should be followed to protect the standby battery supply.

2-29. RESHIPMENT. The environmental container offers adequate protection for reshipment of the RCS-4B. The container has bottom rails to facilitate handling with a forklift. The front and rear covers should be in place when moving the unit, and extreme care should be taken to avoid damaging the instrument.

SECTION 3

OPERATION

3-1. INTRODUCTION

3-2. This section provides the basic information required to operate the RCS-4B receiver. The operating controls and indicators are illustrated, and the function of each control and indicator is described.

3-3. CONTROLS AND INDICATORS

3-4. The controls and indicators required to operate the receiver are located on the front panel of the receiver units. Operator controls consist of pushbutton switch-indicators and toggle, thumbwheel, and rotary switches. Controls and indicators are illustrated in figure 3-1 and functionally described in table 3-1.

3-5. OPERATING INSTRUCTIONS

3-6. GENERAL . The RCS-4B receiver operates in synchronization with up to three TCS-4B transmitters. Once set up and synchronized, the receiver is capable of fully automatic operation or can be manually controlled. Four modes of operation are available: continuous, manual, set, and programmer. Each mode has a particular purpose and provides different functions. A mode of operation can be selected or the mode changed while the receiver is operating (frequency being swept) without affecting the frequency sweep or system time.

a. Continuous Mode. The continuous mode of operation provides a continuous scan on the operating frequency range and is intended for use during service test of the receiver. With the MODE switch in CONT position, the receiver sweeps and re-cycles continuously between the low of 2 MHz and the preset high of either 16 or 30 MHz. The PATH PROGRAMMER MINUTES switch and the RESET, START, and STOP switches have no affect on receiver operations in this mode. If the sweep is stopped, placing the MODE switch on CONT position starts the sweep. The sweep is terminated by switching to any other mode or by resetting the sweep to 2.00 MHz in manual mode. Continuous mode is used primarily for maintenance service of the receiver and is not intended for normal operation.

b. Manual Mode. In manual mode, the receiver sweep is controlled by the START, STOP, and RESET switches. This mode is used to reset the frequency sweep at start up and to exercise manual control of receiver frequency during maintenance. When started, the frequency sweep advances from 2.00 MHz to the preset high limit and then resets to 2.00 MHz and stops. If, during a frequency sweep , the STOP switch is activated, the sweep stops and the receiver remains tuned to the fixed frequency. System time is not affected by actuation of START, STOP, or RESET switches in manual mode; only the frequency sweep is controlled. In manual mode, data is displayed on the path 1 CRT display.

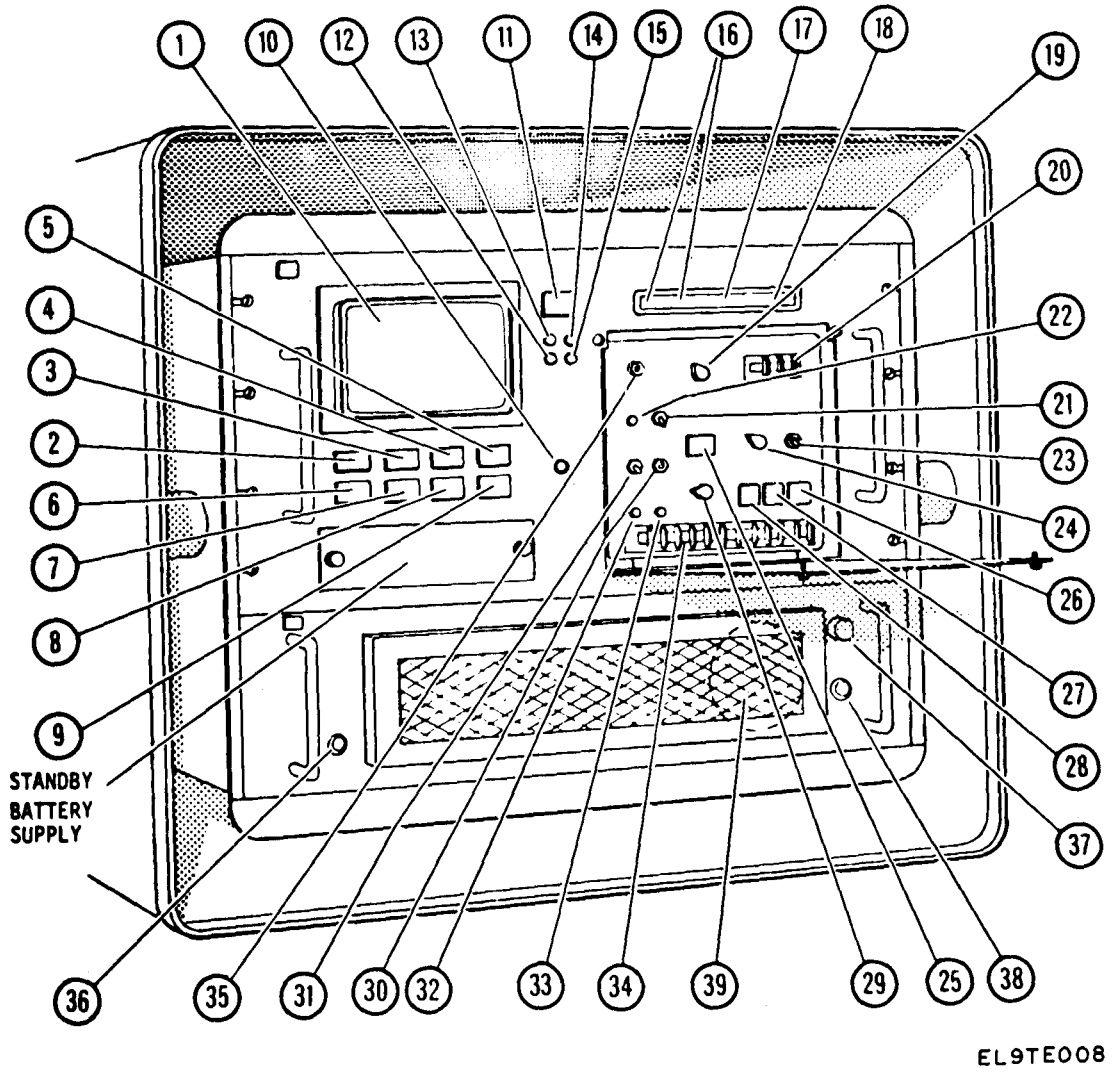


FIGURE 3-1. Receiver Controls and Indicators.

Table 3-1. Controls and Functions

Fig. ref.	Control or indicator	Function
1.	CRT Display	Displays relative signal mode time delay and signal amplitude in Y-axis, frequency in X-axis. Refer to figure 1-2.
2.	DISPLAY 1 switch-indicator	When pressed to lighted position, selects last received path 1 chirpsounder record for display on CRT.
3.	DISPLAY 2 switch-indicator	When pressed to lighted position, selects last received path 2 chirpsounder record for display on CRT.
4.	DISPLAY 3 switch-indicator	When pressed to lighted position, selects last received path 3 chirpsounder record for display on CRT.
5.	CYCLE switch-indicator	Sequentially cycles each of the three paths for display on the CRT. Displayed time (cycle rate) is about two seconds per path.
6.	CURSOR ERASE switch	When pressed, erases a stored cursor when overlapped with movable cursor.
7.	CURSOR switch	When pressed, moves cursor from right to left on CRT.
8.	CURSOR switch	When pressed, moves cursor from left to right on CRT.
9.	CURSOR STORE switch	When pressed, causes a cursor to be stored and displayed on the CRT screen in a fixed frequency position. The position corresponds to the position of the movable cursor. Up to six fixed cursors can be stored and displayed.
10.	CURSOR FREQ. pushbutton switch	Provides digital readout of movable cursor frequency on MHz display. Cursor frequency substitutes for receiver frequency when switch is actuated. When a fixed cursor frequency readout is required, the movable cursor is positioned behind the fixed cursor and the switch depressed.
11.	TEST switch-indicator	When pressed to lighted position, initiates both a receiver functional test cycle and a standby battery voltage test.

Table 3-1. Controls and Functions - Continued

Fig. ref.	Control or indicator	Function
12.	RCVR indicator (red)	If the lamp remains lighted for five seconds after initiation of test, indicates malfunction in synthesizer or receiver circuits (internal fault) or malfunction of one or more power supplies.
13.	RCVR indicator (green)	When lighted, indicates receiver, synthesizer, and power supplies, are fully operational. (Test may take up to five seconds to complete.)
14. 15.	BATT indicator (green) BATT indicator (red)	Two lamps indicate standby battery condition. Lamps are activated by circuitry that measures battery box terminal voltage. For the non-rechargeable battery supply (P/N 6025-1008) , a test is performed with AC line power either on or off, battery switch (31) on, and TEST switch (11) pressed. For the rechargeable battery supply (P/N 6025-1018) , the AC line power must be off to conduct an accurate test. However, if the rechargeable battery supply is in a low charge condition, turning off AC line power can cause loss of synchronization. If operating in synchronization with a transmitter, this test should be made with AC line power on. In this case for the rechargeable battery supply, the green BATT lamp should always light unless the supply is fully discharged or defective in which case the red /green or red lamps will light. (Refer to paragraphs 5-15 and 5-16 for test description.) For the non-rechargeable supply, the following indications apply: • Green ON only = Batteries good (voltage greater than 23V) . • Red and green ON together = Batteries weak but still operational - will need replacing soon. (Voltage between 18 and 23 volts) . • Red ON only = Battery condition unacceptable (voltage less than 19 volts) ; indicates very weak or dead batteries, or battery switch (13) is off. • Red and green both OFF = This condition occurs only when the AC line power is off and the battery voltage is less than 14 volts indicating that the battery switch is off or the batteries are totally dead.

Table 3-1. Controls and Functions - Continued

Fig. ref.	Control or indicator	Function
16.	MIN SEC Clock display	Provides a numeric display of path 1 clock in minutes and seconds with MODE switch in all positions except SET 2 and SET 3 positions. Displays path 2 time with MODE switch in SET 2; displays path 3 time in SET 3 position.
17.	MHZ frequency display	Provides digital readout of receiver tuned frequency for path being received. Frequency readout is truncated at 10 kHz decade. When CURSOR FREQ switch is actuated, readout is the frequency of movable cursor.
18.	PATH display	Provides numeric display of received path, indicating sounder channel currently being received and processed (display path shown on CRT may be different).
19.	INPUT ATTEN (dB) switch	Selects antenna input attenuation of 0, 10, 20, or 30 dB.
20.	ANTENNA SELECT switches	Three thumbwheel switches to select one of three receiving antenna inputs for designated path.
21.	FREQ switch	Selects 2-16 MHz sweep or 2-30 MHz sweep limits.
22.	ADV TIMER pushbutton switch	When actuated, advances selected path clock in one minute increments. Active only when MODE switch (29) is in SET position.
23.	MANUAL SYNC ADV-RET switch	Three-position toggle switch to advance or retard timing of selected paths in increments as selected by the SLIP RATE switch. This switch is used to center the displayed path on the CRT and is enabled only with MODE switch (29) in SET position.
24.	MANUAL SYNC SLIP RATE switch	Three-position rotary switch used in conjunction with item 23 to produce path timing changes at 1, 10 or 50 milliseconds per second rates.
25.	AUTO SYNC pushbutton switch-indicator	When actuated, starts automatic signal acquisition and synchronization for path selected by MODE switch (SET 1, SET 2, or SET 3). Switch indicator lamp flashes during signal search; lamp lights steady when synchronization is achieved.

Table 3-1. Controls and Functions - Continued

Fig. ref.	Control or indicator	Function
26.	RESET switch-indicator	When MODE switch is in MAN or SET position, switch lights to indicate reset function is enabled. When actuated in manual mode, resets frequency sweep to lower limit, 2.00 MHz. When actuated in set mode, resets selected path time to zero.
27.	STOP switch-indicator	Stops sweep in manual mode. The switch lamp lights when MODE switch is in MAN position to indicate that switch function is enabled. NOTE STOP switch is illuminated when in SET mode, but switch function is not active.
28.	START switch-indicator	Starts sweep in manual mode; starts path clock in SET mode. The switch lamp lights when MODE switch is in MAN or SET position to indicate that switch function is enabled.
29.	MODE switch	Four-position rotary switch selects receiver mode of operation: a. CONT: Enables continuous sweeping. b. MAN: Enables START, STOP, and RESET switches for manual sweep control. c. SET 1, SET 2, SET 3: Enables RESET and START switches for control of path 1, path 2, or path 3 clock. d. PROG: Enables automatic sweep under control of the MINUTES PATH PROGRAMMER switches.
30.	CRT BRIGHT potentiometer	Controls brightness of CRT screen.
31.	BATT switch	ON-OFF control for battery circuit of program timer standby power supply. NOTE Once the receiver is synchronized to any transmitter this switch should be left on. When on, battery control of the timer becomes automatic in the event of primary AC power failure.

Table 3-1. Controls and Functions - Continued

Fig. ref.	Control or indicator	Function
32.	LAMP TEST pushbutton switch	When actuated, energizes all indicator lamps and the digital LED displays on the receiver front panel.
33.	DISPLAY TIME PATH 1 pushbutton switch	When pressed, provides numeric readout of path 1 time on MIN SEC display. Active only when mode switch is in SET 2 or SET 3 position. Used for setting path 2 or path 3 clocks relative to path 1 clock.
34.	PATH PROGRAM-MER MINUTES switches	Twelve 4-position thumbwheel switches to select path 1, 2, 3 or 0 (off) for each 5-minutes in the hour.
35.	STD ADJ potentiometer	A 20 turn potentiometer provides fine adjustment of internal 5 MHz frequency standard. One full turn of potentiometer adjustment will compensate timing drifts of approximately 0.5 milliseconds per 24 hours.
36.	POWER switch	Main power pushbutton switch/indicator. Controls power to both receiver units.
37.	AUDIO GAIN control	Gain control for audio monitor circuit (speaker and headphones).
38.	Headphones Jack	Connector for optional headphones (insertion of mating plug disables speaker).
39.	Speaker	Three inch audio monitor speaker (located behind cooling air inlet grill) .

c. Set Mode. In set mode, the receiver clock for each of three paths can be started or reset to zero depending on MODE switch position, SET 1, SET 2, or SET 3. Although the STOP switch is illuminated with the MODE switch in SET position, the STOP function is inoperative. The PATH PROGRAMMER MINUTES switches are active in the SET mode, and the frequency sweep starts automatically at each 5-minute interval that is enabled in the same way as described below for the programmer mode. The set mode can be used for normal, automatic operation; however, since the START and RESET switches are active in this mode, it is better practice to operate in the programmer mode to prevent accidental reset of the system clock. In set mode, the position of the Chirp sounder record on the CRT screen for a selected path (SET 1, SET 2, or SET 3) can be adjusted using the MANUAL SYNC controls. An adjustment of the MANUAL SYNC controls alters the timing of the path clock permanently.

d. Programmer Mode. The programmer mode is typically used for normal, automatic operation after the receiver and associated transmitters are synchronized. In this mode, a sweep is initiated at each 5-minute interval of the hour depending on the position selected for the PATH PROGRAMMER MINUTES switches. The START, STOP, and RESET switches are disabled in this mode. A frequency sweep is initiated in a particular 5-minute period for the path number set into the PATH PROGRAMMER

MINUTES switch. The sweep is inhibited for the 5-minute period when the MINUTES switch is in the 0 position. At the end of each clock hour (end of the 55th minute sweep interval), the cycle automatically repeats.

3-7. INITIAL CONTROL SETTINGS. Before turning power on, open small front panel control door, and make the following preliminary control settings:

WARNING

Make sure that the RCS-4B frame is grounded by the three-wire, three-prong power cord or a separate ground strap before operating. If not grounded the RCS-4B frame and exterior panel could be at a potentially dangerous voltage level.

a. Make sure that BATT switch is OFF. The only time that the BATT switch should be on is when the receiver is on and synchronized with a transmitter. Also, the BATT switch must be ON during receiver test.

b. Make sure AC line voltage select switch and fuse on 4028 unit are matched to the local AC line power.

c. Set INPUT ATTEN (dB) switch to 0.

d. Set ANTENNA SELECT thumbwheel switches to the appropriate antenna input jack number (1, 2 or 3) for each path. Each transmitter received by the RCS-4B is assigned a path number (1, 2 or 3). Each path may have a separate receive antenna or different paths may share an antenna. Assignment of path to receiver antenna inputs may be done in any order or in any combination. For example, path 1 may use antenna 1(J1); paths 2 and 3 may use antenna 2(J2), and antenna 3(J3) may not be used at all; or all paths may use the same antenna. If all paths require the same antenna, input J1 is normally used, but inputs J2 and J 3 will work equally well. Make sure antenna(s) are connected to the 6043 power divider or directly to the 4028 as required.

e. Place FREQ switch in either 2-16 or 2-30 position depending on the selected frequency sweep limit that corresponds with the transmitter setting. One switch determines the sweep limit for all three paths.

3-8. START UP PROCEDURE. The pre-operative start-up procedure for the receiver is performed as follows:

a. Press POWER switch to on (lighted) position. Timer and sweep may start immediately.

b. Check that indicator lamps are good by pressing LAMP TEST switch. With switch depressed indicators and digital display should light.

c. With MODE switch to MAN, press RESET pushbutton to set sweep to 02.00 MHz.

d. Turn MODE switch to SET 1 and press RESET. Then press START and RESET again. Repeat for SET 2 and SET 3. All path clocks are now at 00:00 system time.

e. Press CURSOR ERASE and " " switches simultaneously until CRT screen is cleared of cursors. If cursor(s) persist, cycle power off-on, and repeat steps 1 thru 5.

f. Adjust CRT BRIGHT control (screwdriver adjustment) as desired. Do not overdrive brightness adjustment to point where the white raster is visible as this may damage the CRT.

g. Perform a receiver self test. Turn MODE switch to MAN and press START switch. The BATT switch should be placed in ON position prior to initiating the test. Press the TEST switch and hold it depressed for an entire sweep. After not more than five seconds after pressing TEST, the following results should be observed:

(1) The green BATT lamp lights. For a complete description of the battery test as applicable to either the rechargeable or non-rechargeable supply, refer to paragraph 5-15.

(2) A fixed tone (1050 Hz) is heard on the speaker. Check that the AUDIO GAIN control is adjusted properly.

(3) The green RCVR lamp lights. If the red RCVR lamp lights, refer to paragraph 5-9 for troubleshooting procedures.

(4) A horizontal line is displayed approximately in the middle of the CRT, or approximately 3/4 inch (2 cm) below the bottom of the AGC bargraph. The AGC bargraph should indicate a signal amplitude of approximately 30% of the receiver AGC range or about 4 mm above the AGC baseline.

h. Allow a twenty-minute warm-up period for the frequency standard to stabilize.

i. Synchronize the receiver to the transmitters by performing the procedures of paragraphs 3-11 thru 3-19, after which the RCS-4B is ready for normal operation.

3-9. NORMAL OPERATION. After synchronization is achieved with the transmitters and PATH PROGRAMMER times selected, the receiver can be operated using only the DISPLAY and CURSOR controls. Since specific procedures are dependent on particular field conditions and frequency management requirements, only some typical applications of operating controls are provided as examples. Refer to Section 7 for a discussion of HF circuit management procedures.

a. In the programmer mode of operation, the PATH PROGRAMMER MINUTES switches select the path to be received for any five minute period. The PATH digit display reads out the path being received and the instantaneous receiver frequency. The PATH 1 clock time is also displayed whenever the MODE switch is in PROG position. If the MODE switch is placed in a SET position (either SET 1, SET 2, or SET 3), the time readout on the MIN SEC display is for the corresponding path 1, 2, or 3. If the MODE switch is in SET 2 or SET 3 position, and the DISPLAY TIME PATH 1 pushbutton is pressed, the LED display shows path 1 time as long as the push-button is held down. However, all other controls, such as START, RESET, AUTO SYNC, and SLIP RATE will operate on the circuits of the selected path. Whenever the MODE switch is in any of the three set positions the PATH digit on the LED

display will flash and indicate the position of the MODE switch and not necessarily the actual path being received at that instant in time. For example, if a path 2 sweep was started in the program mode, the PATH digit would show a steady 2. If however, during this sweep, the MODE switch was changed to the SET 3 position, the RCS-4B would continue to receive path 2, but the PATH digit would display a flashing 3. This serves to remind the operator that controls such as START, RESET, and ADVANCE TIMER which affect the program timers are active and will control the path 3 clocks even though a path 2 sweep is in progress. This feature allows the operator to initialize another path program timer while a sounding sweep is in progress without disturbing the RF sweep. The frequency MHz display indicates the RF frequency of the path being received regardless of the position of the MODE switch.

b. During normal operation the INPUT AT TEN switch should be in the “O” dB position. Occasionally conditions of an unusually high background noise strength will drive the CRT bargraph display of received signal strength (AGC level) off scale and make interpretation of the received signal strength difficult. This condition can be remedied by selecting 10, 20, or 30 dB attenuation of the received signal by turning the INPUT ATTEN switch to the respective “10”, “20”, or “30” position.

c. The last received Chirpsounder records, one for each path, are stored in three separate display memories. The DISPLAY switches select which of these records will be shown on the CRT. The display memories are automatically updated, independent of the settings of the DISPLAY switches. Thus, programmed soundings (receiver sweeps) are independent of CRT display operation. Receiver sweeps are determined by the path programmer only. Sweep activity is indicated by the LED numeric display (MHz and path) and the CRT load line cursor which indicates the instantaneous receiver frequency on the CRT display. The CRT DISPLAY controls may be operated at any time with no effect on the receiver’s sweep operation.

d. Up to six fixed cursors can be stored and displayed on the CRT. The movable cursor is controlled with the CURSOR (left) and (right) switches. The frequency setting of the movable (blinking) cursor is displayed on the digital MHz readout when the CURSOR FREQ pushbutton switch is pressed. A fixed cursor is positioned on the CRT by placing the movable cursor (using the CURSOR , switches) at the particular frequency of interest and pressing the CURSOR STORE switch. The fixed cursors remain stored and displayed for all sweeps and for all path displays until erased. A fixed cursor is removed by placing the movable cursor over the fixed cursor and pressing CURSOR ERASE switch.

e. Due to slight differences in the absolute frequency of the sounder transmitter and receiver frequency standards, the Chirp sounder records will slowly drift up or down on the receiver CRT. This drift requires an occasional manual slip adjustment of the receiver synchronization to recenter the Chirp sounder record on the CRT. If however, this manual slip adjustment is required more than once every eight hours, the frequency standard should be adjusted (paragraph 5- 21) . The slip adjustment is made with the receiver MANUAL SYNC controls as follows:

(1) Wait until the RCS-4B starts a sweep for the path to be recentered.

(2) Select the CRT display for the path to be recentered.

(3) Turn the MODE switch to the SET positon corresponding to the path to be recentered, and set the SLIP RATE to 1 ms/sec.

(4) When the receiver starts showing Chirp traces on the CRT, place the MANUAL SYNC switch either to ADV position to raise the traces on the CRT or to RET position to lower the trace. The traces move as the receiver changes synchronization by 1 ms for every second the ADV/RET switch is activated. The total CRT display range is 5 ms for the 2-30 MHz sweep (or 10 ms for the 2-16 MHz sweep). Thus, activating the MANUAL SYNC switch for 1 second (at the 1 ms/sec slip rate) moves the CRT display by 20% of its range when operating on a 2-30 MHz sweep.

(5) After recentering, place MODE switch in PROG position.

The receiver synchronization may be changed at any time, even when not sweeping. However, the change in synchronization is only immediately visible at the CRT load line cursor while sweeping. If the receiver synchronization is changed when the sweep is stopped or during a portion of the sweep where there are no chirp traces, there will be no immediate indication on the CRT that the synchronization has changed. The result of the change will be visible only when the sweep advances to the propagating band where the change in trace position will be visible.

NOTE

Do not change the synchronization of a path while the receiver is sweeping a different path (i.e. do not slip PATH 1 while sweeping PATH 2).

3-10. SYNCHRONIZATION

3-11. The RF sweeps of the RCS-4B and TCS-4B must be synchronized in time to an accuracy of about one millisecond for proper operation. Because it would be extremely difficult to directly synchronize the receiver and transmitter program timers to this accuracy, a four-step procedure is used that makes synchronization relatively easy. This four-step procedure, summarized in steps a thru d below, is described in paragraphs 3-12 thru 3-19:

a. Establish the TCS-4 sweep program and determine which 5 minute segments of the hour a particular transmitter is transmitting and set the receiver PATH PROGRAMMER to the same segments. For example, path 1 sweep may be set for 00, 15, 30 and 45 minutes; path 2 set for 05, 20, 35 and 50 minutes; and path 3 set for 10, 25, 40 and 55 minutes.

b. Establish the transmitter clock timing relative to real time. For example, the clock could be started 1 minute and 14 seconds after the 00 minute and 00 second of the real time hour. When operating a multiple (2 or more paths) sounding network it is recommended that the transmitter clock start times be offset from one another by a minimum of two seconds (even when the individual path sweeps are programmed for different 5 minute segments of the hour) to avoid any possibility of accidently synchronizing the receiver on the wrong transmitter. For example, path 1 start time mav be four seconds after the time reference (e.g. WWV); path 2 at seven seconds after; and path 3 at 15 seconds after. To insure reception of all three paths without loss of data, the path start time offsets should be within a 20-second “window”.

c. Manually start one of the RCS-4B receiver path clocks to match the desired transmitter start time from step b. The receiver path clock must be started with a ±1 second accuracy.

d. When the next regularly programmed sweep of the RCS-4B starts for that transmitter, fine adjust the RCS-4B sweep and time synchronization by means of the AUTO SYNC and/or MANUAL SLIP procedure until the receiver detects the transmitted signal and the received signal is properly displayed on the RCS-4B CRT display.

Because in the normal programmer mode, the RCS-4B displays path 1 time only, care should be used in setting the path 1 clock as the basic clock for all transmitters. All transmitter start times should be set relative to the path 1 clock. It is recommended that, if only one or two transmitters are to be received, they be synchronized with the path 2 and/or path 3 clocks using the path 1 clock as a baseline time reference. In general, the path 1 clock is set as ±x seconds relative to some external source. International time standards (e.g. WWV) time reports given every minute or by international shortwave broadcast stations (e.g. BBC) or synchronized wrist watches (preferably electronic digital watches) can be used. Then, the path 2 and path 3 clocks are set relative to path 1 time. Another method is by voice contact between the transmitter and receiver operators via telephone or on a prearranged frequency using HF radio.

3-12. STARTING PROGRAM CLOCKS. To set the RCS-4B path programmer and associated clock timers follow steps a through i below. To set the clocks with large time offsets, refer to paragraph 3-13. To set path clocks 2 and 3 relative to path 1 timing refer to paragraph 3-14 for additional information.

Place MODE switch in MAN and press RESET. Receiver frequency is set to 2.00 MHz

b. Place MODE switch in the SET 1 position or for the path clock that is to be synchronized. Press RESET. Time is set at 00:00.

c. Turn all PATH PROGRAMMER thumbwheel switches to the appropriate path number(s) for each 5 minute segment of the hour.

d. Set the ANTENNA SELECT thumbwheel switches for the appropriate antennas connected to the receiver (refer to 3-7, step d) .

e. Set the FREQ range switch to appropriate 2-16 or 2-30 MHz position.

f. Establish clock start time relative to an external time reference (or to path 1 clock) to within ±1 second accuracy. (Path 1 time can be made to appear on the digital display by pressing the DISPLAY TIME PATH 1 pushbutton when the MODE switch is in SET 2 or SET 3 position.)

g. At appropriate start time press START. The path clock starts and, if the 00 MINUTE-PATH PROGRAMMER thumbwheel switch has been set to the same path number, the receiver sweep starts.

h. Check the accuracy of receiver clocks to time reference by observing LED clock timer display. It is desirable for the receiver clock to be set to the time reference with less than ±0.5 second error (±1.0 second maximum). If the time error is greater than 0.5 seconds, place the MANUAL SYNC-SLIP RATE control to 50 ms/see and momentarily push the MANUAL SYNC toggle switch to ADV to speed up the receiver clock, or to RET to slow down the receiver clock relative to the time reference. Pressing the ADV/RET toggle one way for 10 seconds will change the receiver clock by 0.5 seconds from its previous timing.

i. Turn BATT switch ON.

3-13. SETTING THE PROGRAM CLOCK WITH TIME OFFSETS. The ADV TIMER button is used to preset the receiver clocks to real time (as determined from time standard WWV or similar source). It can also be used to preset the receiver with a start time offset. Each time the ADV TIMER button is pressed, the receiver program clock timer will advance by one minute from its previous setting. This is done so that individual transmitters can be distinguished from each other by different start time offsets. The ADV TIMER button operates only on the particular path program timer selected by the MODE switch in one of the three SET positions; i.e. if the MODE switch is in SET 1, only the path one timer is affected by the ADV TIMER button. Note that timing offsets are defined as the time that a sweep starts after an integer 5 minute interval of a real time standard. For example, if the start time offset is 2 minutes and 20 seconds, the sweep programmed for the 00 minute segment will start at 02:20 real time, and the 05 minute program sweep will start at 07:20 real time, etc. Follow these steps to begin a sweep with a timing offset:

a. Place the MODE switch in the SET position for the path timer desired (for example SET 1) , and press RESET.

b. Determine how much time the start of the sweep is to be offset. For example, assume the offset will be 2 minutes and 20 seconds.

c. Establish accurate real time by tuning to a time standard (WWV) or using digital watches to note the minute and second.

d. Carefully note when the watch or standard reaches 00 seconds of a minute, Note what the minute is, for example, 16 minutes past the hour.

e. Count 20 seconds (for this example) after the 00 second on the watch. When it reaches 20 seconds, press the START button. The clock time will now start counting on the 6025 LED display.

f. Press the ADV TIMER button to set the minute counter on the display to the real time (from digital watch or WWV) minus two minutes (for this example). Thus, if it was 16 minutes past the hour the ADV TIMER button must be pressed to read 14 minutes on the display.

g. The clock is now offset 2 minutes and 20 seconds from real time. You can check this by comparing the 6025 timer display with WWV or a digital watch when the display reaches a minute mark.

3-14. SETTING PATH 2 OR 3 CLOCK RELATIVE TO PATH 1. It is often convenient to coordinate path clock timing with path 1 as the master reference and path 2 and 3 set with a defined delay offset relative to path 1. For example, path 2 clock starts four seconds after path 1, and path 3 clock starts 10 seconds after path 1. To set path clocks 2 or 3 timing relative to path 1 follow these steps.

a. Make sure path 1 clock is running and properly synchronized as the master reference.

b. Place the MODE switch in SET 2 position, and then press RESET. Clock time display will read 00:00 and path number will show a flashing 2.

c. Press and hold down the DISPLAY TIME-PATH 1 button. The LED clock display will show path 1 timing while path 2 indicator continues to flash.

d. When the (PATH 1) clock display advances to the desired delay offset (for example 4 seconds), press START. This will start the PATH 2 clock.

e. Release the DISPLAY TIME PATH 1 button and note the PATH 2 clock has just started. To check the delay offset between path 1 and path 2 timing, alternately press and release the DISPLAY TIME-PATH 1 button and the clock display will alternate between path 1 and path 2 timing so that a comparison can easily be made.

f. Set MODE switch to SET 3 and repeat above procedure to set PATH 3 clock relative to PATH 1.

g. Place MODE switch to PROG position when finished.

3-15. SYNCHRONIZATION WITHOUT PREDETERMINED SWEEP TIMING. The following method can be used if there is no opportunity for prearranged timing or operator contact.

a. The TCS-4 transmitter sweep is started at maximum power at any arbitrary time and is set to sweep every 5 minutes at a prearranged sweep rate.

b. The RCS-4B receiver operator, using a standard sideband HF receiver, monitors a clear voice bandwidth channel on a frequency that typically propagates for the time of day. (For paths less than 1000 km, 2-6 MHz at night and 4-10 MHz during daytime should be satisfactory; for longer paths, frequencies 1.5 to 2.0 times higher can be used.) The operator listens for the characteristic “chirp” sound resulting when the transmitter signal passes through the received bandwidth. For a 100 kHz/second sweep, the chirp sounder signal remains in a 3 kHz channel only 30 milliseconds and sounds like a very brief whistle or sliding pitch tune. For 50 kHz/second sweep, the sliding tone can be heard for at least 60 ms and the monitoring process is easier.

c. When the receiver operator believes he has heard a chirp signal pass through his channel, he notes the time and monitored frequency and then tunes to another clear channel 1 MHz higher. For a 100 kHz/second sweep, the chirp will be heard exactly ten seconds later; for a 50 kHz/second sweep, a 20 second period is required. If the chirp is heard again, the second frequency and time are noted.

d. If no chirp is heard, the operator retunes to the original clear channel and waits to see if the same chirp-like signal is heard exactly 5 minutes later. If the chirp signal is heard at the appropriate time, it is recommended that the operator tune to another channel 1 MHz higher and listen again for the signal, repeating the process until no signal is heard. This helps to approximately establish the expected propagating frequency range.

e. If the operator believes he heard a chirp signal, he should retune his monitor receiver to the frequency where it was best heard and wait to see if the signal is heard again exactly 5 minutes after the first recorded observation.

f. The monitored chirp sweep start time can then be determined relative to the baseline time reference by computing the difference between the monitored frequencies and 2 MHz, dividing that difference by the observed sweep rate, and subtracting the resulting number of seconds from the recorded times. All observations should result in the same start time within a one-second tolerance or additional observations are necessary.

3-16. SWEEP SYNCHRONIZATION. The final step in synchronizing the receiver with a transmitter is the fine adjustment of the receiver timing and sweep synchronization to exactly match that of the transmitter. This is accomplished by using the automatic synchronization procedure, paragraph 3-17, or by manual synchronization, paragraph 3-18.

NOTE

When the path clock start time is known relative to the PATH 1 clock or to an external time reference, this information should be carefully noted as it will facilitate the synchronization process should there be difficulty later.

3-17. AUTOMATIC SYNCHRONIZATION PROCEDURE. After the receiver programmer and clocks have been set as described in paragraphs 3-12 thru 3-15, the AUTO SYNC circuit is used to acquire and lock the receiver onto the transmitter signal.

a. Check the following:

(1) FREQ range switch is set to the appropriate 2-16 or 2-30 MHz position.

(2) ANTENNA SELECT thumbwheel switch is set appropriately.

(3) INPUT ATTEN is set to 0 dB, or 10 dB in high noise areas or when heavy interference is expected.

(4) PATH PROGRAMMER switches are set correctly.

(5) Path clocks are set and running.

(6) BATT switch is ON.

b. When the next programmed sweep starts for the path to be synchronized, perform the following:

(1) Place the MODE switch in the SET position corresponding to the path to be synchronized.

(2) Press AUTO SYNC pushbutton to initiate automatic synchronization process. The AUTO SYNC button should be pressed just before the sweep reaches the expected propagating band for the path, if known. For example, if it is known that the propagating frequencies for the path are 10 to 20 MHz, the AUTO SYNC button should be pressed when the sweep reaches approximately 9 MHz. If the propagating band is not known, press the AUTO SYNC button just after the sweep starts, around 2.5 MHz. The AUTO SYNC indicator lamp flashes while synchronization is underway, and the CRT load line indicator moves at a faster rate than the digital frequency readout indicates.

(3) The AUTO SYNC switch-indicator stops flashing and remains lit when internal criteria for probable signal acquisition are met. If no signal acquisition occurs, the AUTO SYNC feature terminates just before the upper frequency limit is reached.

(4) Verify that proper signal acquisition and synchronization has occurred by listening for an audio tone from the speaker and looking for a Chirpsounder record to appear on the CRT. Make sure to select CRT display path number that is the same as path being synchronized.

(5) If no tone is heard and no Chirpsounder record is displayed, the signal acquisition circuit has been falsely triggered. After a false sync the path clock may have to be reset. Check the receiver clock timing relative to reference and correct if necessary. Refer to paragraph 3-12 h. If the clock timing is correct, the auto sync process can be restarted by pressing the AUTO SYNC button again. The auto sync process can be repeated (or restarted) as many times as necessary to achieve synchronization as long as the receiver path clock timing is correct, and the receiver is making a programmed sweep for the path to be synchronized when the AUTO SYNC button is pushed. On rare occasions, the AUTO SYNC circuit will be falsely triggered repeatedly in the same frequency range by the presence of a large number of interference signals. To avoid this situation, try turning the INPUT ATTEN to 10 dB .

(6) When signal acquisition ocurs, the Chirpsounder record may be moved to the desired position on the CRT screen bv setting the MANUAL SYNC-SLIP RATE switch to the 1 millisecond per second position and pushing the ADV/RET switch to move the display up or down. (Refer to paragraph 3-18 g).

NOTE

The Chirpsounder record obtained immediately after auto synchronization will not be registered correctly with the frequency calibration on the CRT. Do not use this first record for frequency management data. The next complete Chirpsounder record will be registered correctly.

(7) Occasionally the AUTO SYNC circuit will lock onto the chirp signal and the chirp tone will be heard in the receiver audio, but no traces will be visible on the CRT display. When this happens the signal traces are just above the top of the CRT display area and can be brought back down on screen as follows:

(a) Set Controls:

Mode = SET (of path synchronized)

SLIP RATE = 1 ms/sec

CRT DISPLAY = Path being synchronized

(b) Listen for chirp audio tone and depress MANUAL SYNC toggle to RETard while watching CRT.

(C) Tone should drop in pitch and chirp trace should slowly move down from top of the CRT.

(d) Release RETard switch when traces are approximately centered or slightly below center of CRT. Audio tones should be approximately 1000 Hz in pitch.

(8) Place MODE switch in PROG position.

3-18. MANUAL SYNCHRONIZATION PROCEDURE

a. Perform all steps (1 thru 6) of paragraph 3-17 a above, and then place the MODE switch in the SET position corresponding to the path to be synchronized.

b. Place MANUAL SYNC-SLIP RATE switch in the 50 millisecond per second position. Adjust AUDIO GAIN to hear signal when acquired.

c. Search for the transmitted signal by pushing ADV/RET (advance-retard) switch to ADV position for 20 seconds, then RET position for 40 seconds, then alternate to ADV and RET positions for 40 seconds each until signal is acquired.

NOTE

At the 50 millisecond per second slip rate, the procedure of step c causes the receiver sweep timing to advance and retard over a plus or minus 1-second window relative to the original start time. The original start position is reached by holding the last sweep advance or retard action for 20 seconds. If the receiver operator is convinced his start time is matched to the transmitter start time within a smaller window, he may reduce the time he holds the ADV/RET switch in each position. In any event, interruption of the advance/retard routine may cause loss of the original start point. If this occurs, recovery is best achieved by checking the clock timing and repeating step c at the start of the next sweep.

d. While advancing or retarding the receiver sweep, listen carefully for any chirp tone sliding in pitch, as opposed to the popping sounds making up the background noise. The received chirpsounder signal is in the receiver passband 100-200 milliseconds (depending on the sweep rate) 20 times longer than any background interference.

e. When any chirp tone is heard, immediately release the ADV/RET switch.

f. If the switch is released quickly enough in step e, the tone should remain audible. If not, rotate MANUAL SYNC-SLIP RATE switch to the 10 position and continue the search by pressing the ADV/RET switch to the opposite position from that last used in the 50 position. Hold the switch for 5 seconds, then alternate advance and retard actions for 10 second periods until the chirp tone is acquired, or until the operator is convinced that a legitimate chirp tone was not heard. If no tone is heard, hold last switch position for 5 seconds to return timing to original point; then return MANUAL SYNC-SLIP RATE switch to 50 and pick up search where it was interrupted at step e above.

g. When the tone remains in audio passband, the transmitter signal is acquired. Rotate MANUAL SYNC-SLIP RATE switch to 1 position. Momentarily place ADV/RET switch in ADV position. The pitch of the tone should increase, and the Chirpsounder

record line on CRT should move up. If this occurs, signal is properly acquired; if not, (the trace moves down) the audible tone is the opposite mixer product of the receiver baseband output, and the receiver timing must be advanced at the 1 milli-second /second slip rate until the Chirp sounder record trace drops to the bottom of the CRT and folds over about the baseline of the CRT and starts moving up the CRT screen. When the tone is between 700 and 1200 Hz pitch, the signal should be visible on the CRT display and in proper sync.

h. Use manual slip at 1 ms/see rate to position Chirpsounder record in center or slightly below center of the display area on the CRT display.

i. If the Chirp signal is not acquired during the sweep, repeat entire procedure during next programmed 5-minute period for the path.

3-19. Following the automatic or manual synchronization of a path (paragraph 3-17 or 3- 18) , the next programmed chirp record display for that path may appear vertically displaced from its original position and may even be slightly off screen. Should this occur, a minor manual synchronization adjustment may be made, while the sounding is in progress. Follow these steps:

a. Place the MODE switch to SET 1, 2, 3 (as appropriate).

b. Place the SLIP RATE switch to 1 ms/sec.

Advance or retard the MANUAL SYNC until the sounder display is properly positioned on the CRT.

d. When the display is properly positioned, return the MODE switch to PROG position. All further soundings will be in sync.

3-20. STANDBY POWER. In the event of primary power loss, all displays will turn off. If battery power is on, the internal clock will continue to function until primary power is restored or the batteries discharge. The duration of the battery pack life is dependent on ambient temperature. At 23°C, life of a fully charged battery will exceed 24 hours. At 0°C, battery life may be no longer than eight hours. When primary power is restored after an interruption, the receiver may generate a random, out-of-sequence frequency sweep. When this sweep is completed, normal operation will commence on the next programmed 5-minute interval.

3-21. SHUTTING DOWN THE RECEIVER

3-22. If all receiver power is to be shut down, but time synchronization (temporarily) maintained, make sure that the BATT switch on the 6025 is ON.

3-23. [f receiver is to be shut down with loss of time synchronization, turn BATT switch OFF . Then, turn off power switch on the 4028 unit.

3-24. For shutdown of more than two days, the following steps should be performed:

a. For receivers with the non-rechargeable standby battery supply (P/N 6025-1008), turn BATT switch OFF, and then turn off the 4028 power switch.

b. For receivers with the rechargeable standby battery supply (P/N 6025-1018), perform these steps:

(1) Operate equipment from normal AC line power for 24 hours (minimum) to fully charge batteries. (Batteries must not be stored if discharged.)

(2) Turn BATT switch ON at 6025 front panel.

(3) Turn off AC line power to RCS-4B.

(4) Press TEST switch on 6025 front panel and verify green BATT test indication.

(5) Remove battery supply from 6025 and momentarily press battery cutout pushbutton (S1) through hole in battery box top cover.

(6) Reinstall battery supply in 6025 with AC line power off.

(7) Press TEST switch on 6025 front panel with AC line power off and BATT switch ON. Verify that BATT test lamps on front panel do NOT light.

(8) Turn BATT switch OFF.

(9) Secure equipment for shipping or storage.

CAUTION

Do not turn on AC line power to instrument at any time after the batteries are disconnected with battery box cutout pushbutton until equipment is ready for normal use. Applying AC line power to unit automatically re-connects batteries to battery charger circuit (even with front panel BATT switch off) and slowly discharges batteries when AC line power is removed. If AC line power is accidentally applied prior to storage, repeat procedure starting at step b above.

3-25. For long term storage (more than six months) of receivers with the non-rechargeable standby battery supply, remove and store separately the D-cell batteries. For receivers with the rechargeable battery supply, first, perform the procedures of paragraph 3-24 b above, then remove the complete battery drawer assembly from the 6025, and store separately to avoid damage from any possible battery cell leakage.

NOTE

Early versions of the rechargeable battery supply - part number 6025-1018, Revision A - did not include a battery cutout pushbutton switch (S1). Later versions - Revision B and on - include the cut-out switch (S1) and a deep-discharge battery protection circuit that prevents battery damage if the battery supply is accidentally left on and allowed to discharge. The Revision A version of the battery supply may suffer permanent damage, and cannot be recharged, if it is allowed to completely discharge or if it is stored for long periods without first being fully charged. Operating procedures for the Revision A version of the rechargeable battery supply are the same as for the non-rechargeable battery supply. However, the Revision A rechargeable battery supply should be stored only after it is fully charged. If difficulties or poor performance are encountered with the Revision A battery supply, contact BR Communications for assistance or repair.

SECTION 4

THEORY OF OPERATION

4-1. INTRODUCTION

4-2. This section of the manual contains descriptions of the circuits which comprise the RCS-4B receiver. System and functional block diagrams are included to aid in understanding operation of circuits and subsystems. Detailed schematic diagrams are included as foldouts.

4-3. FUNCTIONAL DESCRIPTION

4-4. The RCS-4B receiver consists of three rack- mounted units as shown in figure 4-1. The 6025 control/display (unit 1) contains the circuit modules that perform timing and control functions and process the baseband signal and AGC voltage (from the 4028 receiver) to produce an ionospheric sounding record with an AGC bargraph on the 6025 CRT display. Also on the 6025 is a numeric display of system time, receiver tuned frequency and path in progress. The 4028 receiver (unit 2) is a synthesized heterodyne HF receiver that receives the chirp signals on one of three antenna inputs via power dividers in the 6043 unit. The triple conversion receiver produces a baseband signal suitable for spectrum analysis. All local oscillator mixer injections are derived from a phase-locked loop synthesizer. The 6043 power divider (unit 3) uses three separate four-way power dividers to provide the 4028 receiver with three antenna connections and to furnish up to three additional antenna connections for use with communications receivers. The functional elements and interconnections of receiver units and assemblies are shown in the block diagrams of figures FO-1 and FO-2.

4-5. 6025 CONTROL/DISPLAY UNIT (UNIT 1)

4-6. The 6025 unit comprises five major functional sections as shown in figure 4-1. Also, included are voltage regulators, a standby battery supply, front panel controls, and the receiver self-test circuit. The frequency standard function is provided by assembly 1A6 which contains two circuit cards and an oven-enclosed crystal oscillator. As another functional section, the spectrum analyzer circuits are in a single module (1A1) containing two circuit card assemblies. The receiver control section includes the 3-path controller module (1A 4) and the auto/sync circuits which are part of assembly 1A5. The 3-path controller module contains two circuit card assemblies. Considered part of the CRT display section are the circuits of the display logic module 1A2, display memory module 1A3, and CRT display module 1A7. Both the 1A2 and 1A3 modules contain two circuit card assemblies while 1A7 module contains one circuit card assembly.

The numeric display module 1A9 contains two circuit cards. The 6025 Control/Display provides all control and timing signals for the 4028 Receiver. The 6025 analyzes the received signal for display of real time ionospheric conditions. These signals are displayed on a front panel CRT, producing an easily interpreted Chirpsounder record, or ionogram. The descriptions that follow for the 6025 circuits are grouped by functional section.

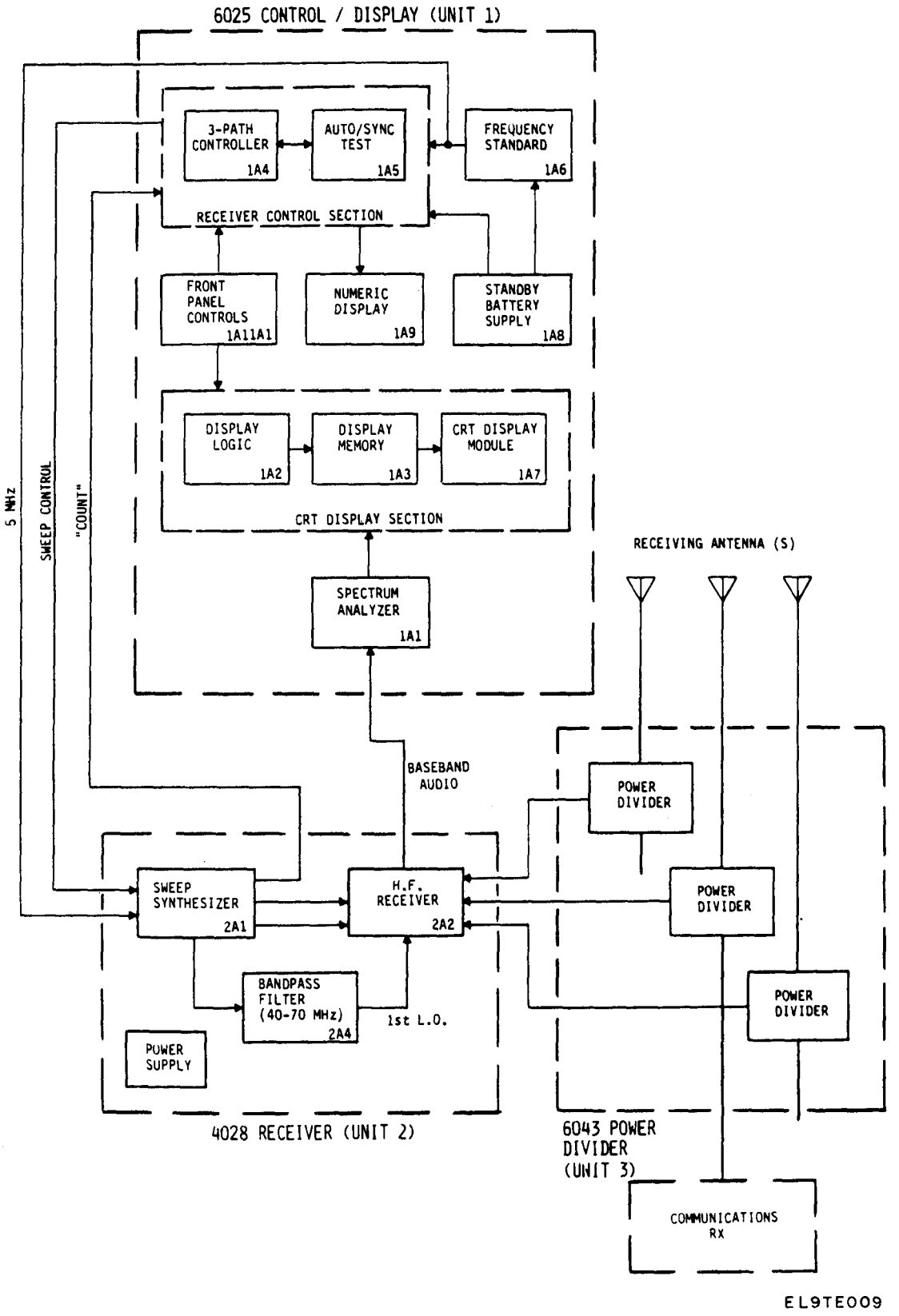


FIGURE 4-1. Receiver System Block Diagram.

4-7. FREQUENCY STANDARD SECTION

4-8. FREQUENCY STANDARD 1A6 (figures FO-7 and FO-8) (S/N 400101 and on). This module provides highly accurate 5 MHz outputs for use by the synthesizer and timing clocks and also provides +5 volts DC (referred to as +5VB)power to the clock circuits. The +5VB supply is generated by a switching regulator (within the 1A6 module) that has a battery backup (1A8) so that time clock synchronization can be maintained during an AC line power failure. The frequency standard has three subassemblies Al, A2, and A3. Assembly 1A6A1 is a high stability, low noise, oven-enclosed, 5-MHz crystal oscillator. It is constructed in a dewar flask to reduce heat loss and thereby minimize oven power consumption. The oscillator has an internal voltage regulator whose output (8 volts) appears at A1J1-2 (figure FO-7). This voltage is used to trim the frequency (coarse and fine) by applying an adjustable DC bias to A1J1-1. On figure FO-7, Q1, Q2, and CR3 comprise a voltage regulator to power the unit during normal operation. In the event of primary power failure, the battery supply on E15 is switched in by CR1. Diode CR2 prevents the battery voltage from appearing on K1 during a primary power failure. This allows K1 to close after a few milliseconds delay and bypass CR1 eliminating CR1 power loss .

4-9. The switching regulator 1A6A3 (figure FO-8) provides +5VDC power (+5VB) for all critical timing circuits involved with receiver synchronization. Regulation is controlled by regulator U1. Switching transistor Q1 and clamping diode CR1 provide variable width drive pulses into storage inductor L1. L1-C2 provides the phase shift necessary for oscillation and determines the switching frequency. L2 and C3 form a ripple reduction smoothing filter. The switching regulator has a 1.5 amp fuse on its input to prevent serious damage in case of a long-term short. Circuit damage from momentary shorts is protected by internal current limiting (R2).

4-10. SPECTRUM ANALYZER SECTION

4-11. SPECTRUM ANALYZER 1A1. The spectrum analyzer circuits process baseband audio (0-500 Hz) analog input (from the 4028 HF receiver section) and supply the resulting spectrum to the CRT display section. Sounder signals are received by the 4028 receiver via different ionospheric modes and are separated into tones of frequency proportional to their relative time delay. The resulting receiver multitone output is transformed into a multi-mode sounder display (for the CRT) by the spectrum analyzer, each tone representing a mode. The basic concept of the spectrum analyzer is to provide high resolution spectral analysis of the incoming baseband signal from the receiver. That is, the spectrum analyzer resolves the composite analog waveform into a group of distinct spectral lines (or tones) which make up the received analog chirp signal. However, the analyzer must also perform this spectral analysis rapidly to keep up with the continuously changing analog chirp signal. Thus, the analyzer operates in “real time” to process the spectrum as quickly as the spectrum changes. The rate of change of the spectrum is determined by the nature of the chirp signal and the analysis bandwidth. In normal operation, the spectrum analyzer is capable of processing the spectrum over six times faster than the “real time” limit. To do so, the analyzer operates with a hybrid digital/analog technique. The analog input signal is A-to-D converted and loaded into a continuously updating and continuously recirculating high-speed memory. The output of the

high-speed recirculating memory is D-to-A converted and the resulting analog waveform is a "time-compressed- frequency expanded" replica of the sampled input waveform which repeats every memory recirculation time. The D-to-A output is then fed to a heterodyne mixer whose local oscillator injection is a frequency sweep (from a linear VCO) covering the entire bandwidth of the frequency-expanded signal every 60 milliseconds. The output of the mixer is applied to a single, amplitude-sampled filter that is synchronized to the 60-millisecond VCO frequency sweep and the 300 microsecond memory recirculation. (The filter is sampled every 300 micro-seconds.) The output of this filter is a series of voltage samples which represent the amplitudes of the spectral components of the analyzed waveform. The resolution of the analyzer is "200 lines", (200 memory recirculation every 60 milliseconds) which is equivalent to dividing the analyzer input bandwidth (e.g. 500 Hz) in 200 parallel, frequency analysis filters. It is this high resolution spectral analysis which gives the chirp sounding technique the ability to make clearly defined, highly sensi-tive soundings with good "mode" or time delay, resolution. Functionally, the spectrum analyzer consists of an input section, dealing with the digital processing (time com-pression speedup) of the input signal, and an output section, covering the analog swept filter analyzer.

4-12. ANALYZER INPUT SECTION (figures 4-2 and FO-9). The incoming signal is first amplified and then sent to a sample-and-hold circuit whose sampling rate is selected relative to the analysis range of interest. The analysis frequency range is programmed by changing TTL programming lines and controlling the selection (U15) of the sample rate divider. The two analysis ranges normally used by the sounder are 500 Hz and 5000 Hz, which require sample rates of 1500 and 15000 samples per second, respectively. The sampling rate is always three times the highest input frequency of interest. The normal analysis range for the receiver (except during auto sync) is 500 Hz. Analog samples of the input waveform taken by the sample and hold circuit Q1 at the selected sampling frequency, are entered into an A-to-D converter (figure FO-9/3) and translated into six-bit digital words. Flip-flops U1 and U3 are used to latch the parallel output of the A/D converter before entering the data into the memory load buffers. The clocking pulse for these flip-flops is the end-of-con-version pulse (TP5) derived from the sampling circuit. The memory load buffers are eight-bit shift registers whose digital bits are clocked forward by the buffer control circuit (figure FO-9/4). The new data is clocked into the load buffers at the sampling rate. The transfer of data from the buffer to the memory is keyed by the 2-MHz memory clock but is also dependent on the status of the buffer control anti-coinci-dence circuits. These circuits prevent coincidence problems between the loading and unloading of the load buffer registers and insures that the contents of the buffer are only clocked out following the "tail" of the circulating memory.

4-13. The memory (figure FO-9/5) is a 600 word, 6-bit per word, MOS shift register loop operating at a two megaword per second rate (300 microseconds per memory revolution). Two 2-MHz clock signals of different phase, derived from the 12-MHz oscillator (figure FO-9/1) continuously clock each of six parallel storage registers which collectively circulate data words at a 2-MHz rate. Each of the six parallel registers consists of three, serially connected, 200-bit long, MOS shift registers to produce the required 600 word long memory. Each time a new input sample is available from the load buffer, it is loaded in place of the oldest memory sample following the "memory tail" (figure FO-9/4). This is achieved using a divide-by-600 counter (U6, U7, and U8) which interfaces with shift register U29 to move

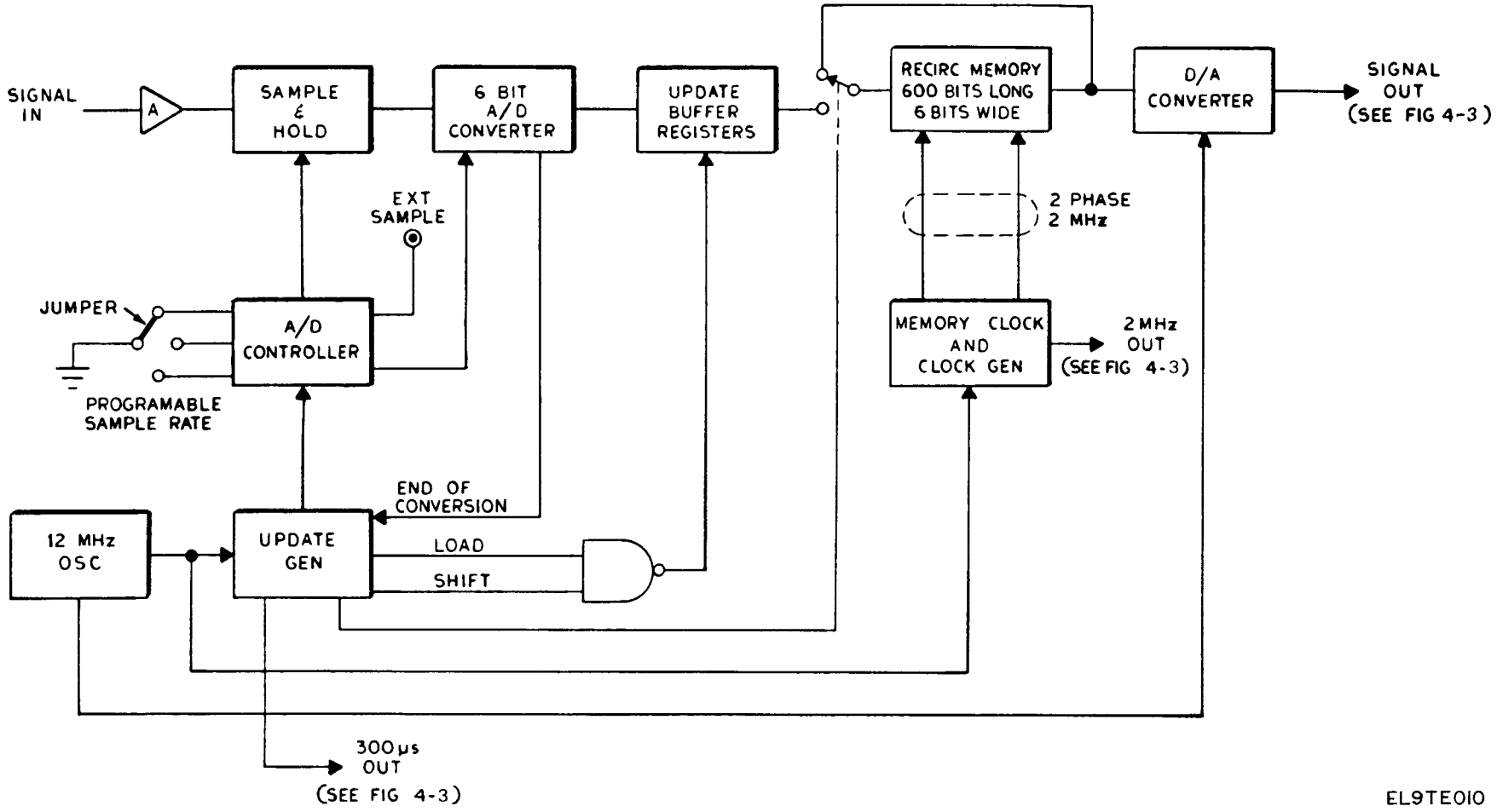


FIGURE 4-2. Spectrum Analyzer Block Diagram - Input Section.

the memory tail by the same number of words entered. The six-bit words circulating in the memory are continuously clocked out at the same 2-MHz into a six-bit, digital-to-analog converter. This output constitutes a reconstructed analog replica of the input signal over the last 600 samples received by the memory. The frequency expansion, or time compression, achieved by the analyzer memory is equal to the ratio of the rate that data is read out of the memory (two megawords per second) to the rate that data is written into the memory. (2M ÷ 1.5K = 1333.3 compression factor). Thus, the frequencies are spread between 0 and 666 kHz, i.e., the 0 to 500 Hz is now translated into 0 to 666 kHz, (0 to 500) x 1333.3 = 0 to 666 kHz.

4-14. ANALYZER OUTPUT SECTION . (figures 4-3 and FO-10). The output section of the spectrum analyzer processes the analog frequency-expanded signal and provides a spectrum output of 0 to 5 volts amplitude, 200-line frequency resolution, and 60-millisecond scan time. The 0 to 666 kHz signal from the digital-to-analog converter is low-pass filtered to remove transition spurs caused by the conversion process. Following the filter is a heterodyne mixer (U25-U26, figure FO-10/1). The mixer local oscillator (2.250-2.916 MHz) is derived from a VCO (QI, figure FO-10/6) driven by a 60-millisecond ramp generator (U 12, figure FO-10/5). The VCO ramp is essentially equivalent to the CRT display vertical sweep. The output of the mixer is applied to a fixed bandpass filter with an effective bandwidth of 3.33 kHz centered at 2.250 MHz. By sweeping the mixer local oscillator between 2.250 and 2.916 MHz, the 0-666 kHz signal is translated to the filter center frequency. This operation is equivalent to sweeping a 3.33 kHz wide filter over the 0 to 666 kHz range of the frequency expanded input data.

4-15. The mixer output is fed to the 2.25 MHz IF processor (figure FO-10/2) and is mixed with 2 MHz. The resulting 250 kHz difference is fed to the gain weighter circuit. The gain weighter (Q7, figure FO-10/3) reduces spurious sidebands on the analyzed signal caused by the data discontinuity at the memory tail (the point where the oldest and newest samples in the memory meet). The sampling filter is a high Q active bandpass filter (C60, L3, Q1O, figure FO-10/3) centered about 250 kHz and having an effective bandwidth of 3.33 kHz. This circuit linearly integrates energy at 250 kHz within its bandwidth over the 300 microsecond memory recirculation time. At the end of the 300 microsecond memory recirculation, a small sample is taken at the positive peak of the 250 kHz waveform. It is the voltage amplitude of this sample, which represents the energy in the filter over the last 300 microseconds, that is used to measure spectral amplitude. At the end of the 300 microsecond period the resonant circuit is quenched (Q11) and the process is repeated.

4-16. The output sample and hold circuit works in conjunction with the sampling filter and supplies the peak voltage data. The output of the sampler (Q16, figure FO-10/3), consisting of stepped samples of the signal waveform, is fed to a low pass spectrum filter for final smoothing before being sent to the CRT display logic circuits.

4-17. RECEIVER CONTROL SECTION

4-18. AUTO SYNC 1A5 (figure FO-11). The auto sync circuit performs the logic functions for automatic time synchronization of the receiver system. Also, a part of the assembly contains the logic circuits to perform the receiver test which is described in paragraph 4-22. The function of the auto sync is to relieve the operator of the task of critical initial synchronization between the receiver and TSC-4B transmitter. In practice, the operator is required only to time the units to within ±1 - second of each other after which the auto sync circuit searches for, and locks onto the chirp signal. Then, it fine adjusts the timing to synchronize the chirp signal within the receiver analysis window.

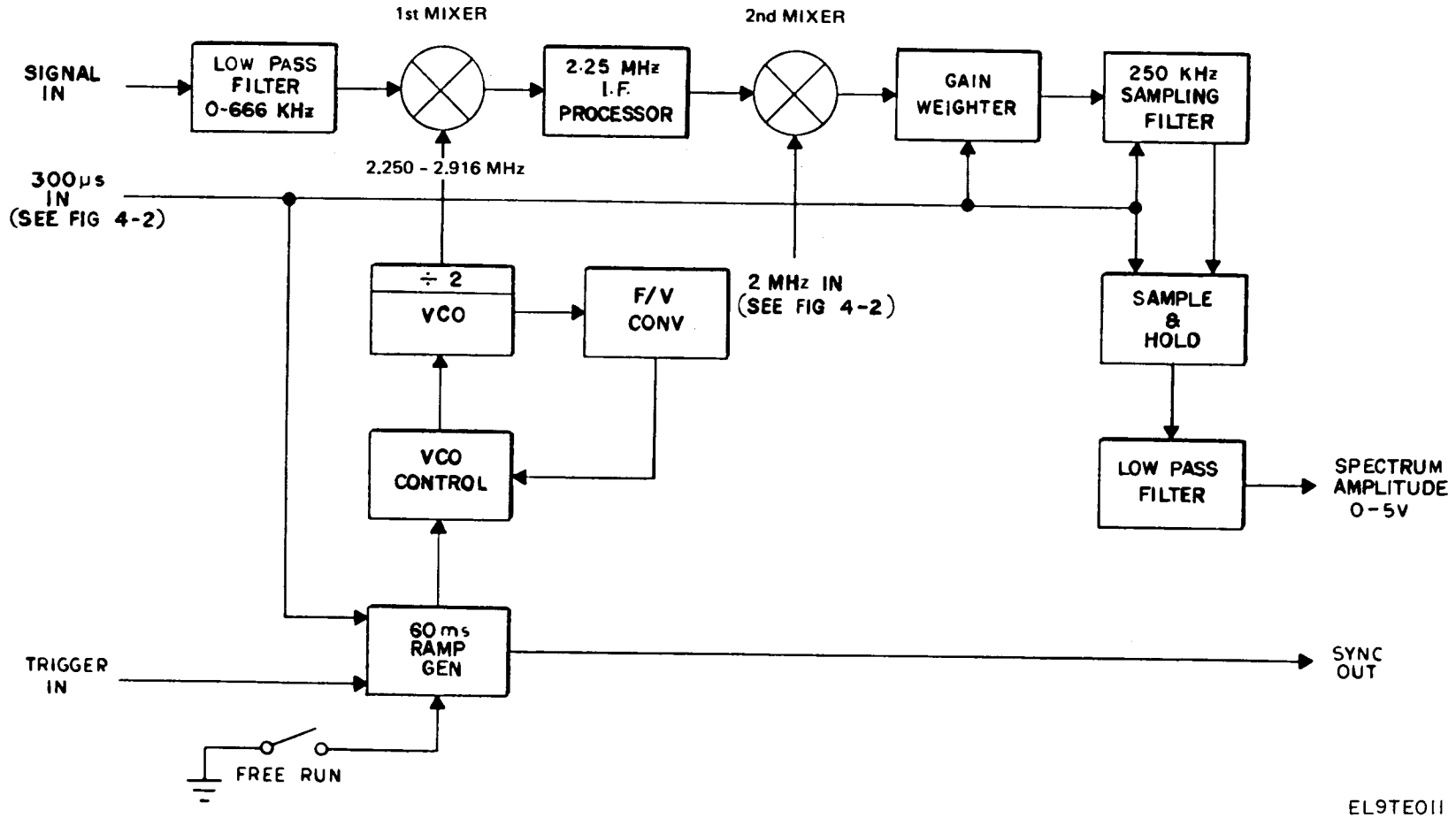


FIGURE 4-3. Spectrum Analyzer Block Diagram - Output Section.

4-19. On activation of the AUTO SYNC front panel switch, the AUTO SYNC lamp flashes (U20, figure FO-11/1), and a signal is sent to the receiver and spectrum analyzer to increase the bandwidth to 5 kHz (from 500 Hz). In addition, another signal (BSL) is sent to the advance control circuits (figure FO-11/2). This (BSL) signal sets in motion the following sequence:

a. A burst of extra clock pulses producing a very rapid timing advance (E63, FO-11/2) moves the 3-path programmer timing clock and synthesizer sweep one-second ahead of the nominal time.

b. A series of short clock interruptions (E66, FO-11/2) to the basic 100 kHz clocks of the 3-path timer and synthesizer which effectively steps or retards the receive system back in time to a point one-second before the nominal start time. Between each retard- step the chirp sweep and timer clocks are allowed to proceed normally for brief periods varying from 90 to 210 milliseconds.

c. During these periods the output of the spectrum analyzer is examined by the auto sync circuitry to determine if a coherent (i.e., same sweep parameters) chirp signal is present:

d. A burst of extra clock pulses that again places the system one-second ahead of the nominal start time; and

e. Retard timing slips as in b above. This sequence is repeated until a coherent chirp signal is detected.

NOTE

The transmitter that the receiver is searching for must be within the ±1-second window if the auto sync is to work properly.

To detect the presence of a coherent chirp signal, the output of the spectrum analyzer is sampled by the data level detector circuit (U62, figure FO-11/3). If the sampled spectrum crosses an adaptive threshold level (indicating the presence of a chirp signal), then logic "1's" are loaded into a 1024-bit MOS memory (U54). The position of the "1's" in the memory indicate the location of the coherent tone in the spectrum analyzer output scan. If this occurs, a second sample is taken to check that the "1's" are still in the same positions to verify that the first detection is not noise. If this checks out, a third (and final test) is run to determine the presence of at least one recurring "1" to verify the coherency of the detected signal. If all three tests prove positive, the receiver is left in the time frame in which the test occurred, a fine adjustment timing slip is made, and the auto sync circuit is disabled.

4-20. If the signal "1's" are not detected and verified during the first test (which is usually the case), then the receiver is retarded (moved) to the next time period. These time periods correspond to every 4 kHz band in the ±1-second window of the chirp sweep (50 bands of 40 milliseconds each for 100 kHz/second sweep rate; 25 bands of 80 milliseconds each at 50 kHz/second). A 2-second burst advance takes place at the end of 25 (50) of these periods if no synchronization occurs, and the test sequence starts over. Each test spectrum is looking for a fixed tone within the receiver baseband. Since the receiver is sweeping through the HF band and crossing many non-sweeping signals, the only fixed tone that should be seen by the

spectrum analyzer would be a signal moving (sweeping) through the HF band at the same rate as the receiver. An occasional strong interfering signal resulting in momentary spectrum analyzer overloads may falsely trigger an auto sync detection. Therefore, up to three tests are made at each of the 25 (50) steps, to insure positive chirp signal identification and interference rejection. Once a conclusive test has been achieved (three consecutive tests with "1" in the same position), the position of the last "1" recorded in the memory is transferred to an up-down counter (U50, U57, figure FO-11/3) where it is used to fine slip the receiver by a proportional amount required to place the detected chirp tone within the normal 500 Hz receiver bandwidth, instead of the auto sync 4000 Hz search bandwidth.

An in-sync (INS) signal is then generated to restore the normal 500 Hz bandwidth to the receiver and spectrum analyzer. If the tests continue to near the upper limit of the sweep (i.e., 256 seconds after the start of sweep) without achieving synchronization, a restoration circuit (U32, figure FO-11/2) resets the slip-burst cycle to the original start time.

4-21. Each path in the receiver is designed to be individually, automatically synchronized using the AUTO SYNC switch in conjunction with the SET positions of the MODE control switch. If the MODE switch is changed from a SET position while performing an auto sync search, the auto sync function is shut down (U31, figure FO-11/1). This prevents loss of sync in other paths.

4-22. RECEIVER TEST CIRCUIT . The test circuit performs a rapid check of receiver sensitivity and power supply parameters. The test circuit is activated by the front panel TEST switch. When initiated, the test includes a check of standby battery status, an overall DC power supply check, and an overall receiver check. The receiver check uses an RF generator to simulate an incoming signal, then checks to see that the signal appears at the correct frequency and at the proper amplitude. The DC power supply check is made using two, 8-input NAND gates (U1 and U2, figure FO-11/4). The voltages checked (+5, -12, +12, and +29/+35) come from various points in the 6025, and the test is intended only to indicate whether a malfunction is the result of a wiring or power supply fault. The power supply test fails when the measured voltages are approximately 50% in error. The inputs are combined and applied to test gate U8-5. Indication of battery condition is made by transistors Q3 and Q4 (figure FO-11/4). These transistors are activated by the TEST switch and are indirectly biased by R 25, R26, and R27 according to the voltage present. Q3 drives the battery green indicator and is on for all voltages above 18 volts. Q4 drives the battery red indicator and is on for voltages below 23 volts. Since there is an overlap between the 18 and 23 triggering voltages, this middle condition (indicating satisfactory but marginal batteries) lights both lamps.

4-23. For receiver sensitivity y test, activation of the TEST switch changes the 4028 receiver input from the antenna to a calibrated, sweeping, RF signal that results in a fixed, 350 Hz tone at the baseband output of the "receiver. Since the bandwidth of the spectrum analyzer (which corresponds to the vertical CRT trace) is 500 Hz, the resulting test output tone (350 Hz) is displayed 7/10ths up the CRT screen, or .7 x 60 = 42 milliseconds along each sync clock period. One shots U10 and U3 position a 5 millisecond wide test window, centered 42 milliseconds after the start of the spectrum analyzer scan (or CRT sync clock period). If the signal is detected in this 5-millisecond wide window, U4-7 goes

low which turns on the green test lamp by means of Q2 and U8. If the test tone is detected outside the window (either before or after), U4 goes high and Q1 turns on the red test lamp. The 2-millisecond pulse at U10-10 delays the start of the test tone detection sequence to skip over spurious noise signals that are occasionally produced by the spectrum analyzer at the very beginning of its scan. If the receiver is not sweeping when the TEST switch is pressed, U8-12 is low, and the receiver sensitivity test is bypassed so that only the power supplies are tested. The results of the receiver sensitivity test and the power supply test are ANDed at U8-6 such that both tests must pass (when receiver is sweeping) before the green test light turns on.

4-24. 3-PATH CONTROLLER 1A4 (S/N 400101 and on). The 3-path controller module consists of the 3-path programmer circuit 1A4A2 and the receiver control circuit 1A4A1. Its function is to control the synchronized timing of the chirp receiver relative to the transmitter for automatic time-programmed sounder operation.

4-25. 3-PATH PROGRAMMER (figure 4-4 and FO-12) (S/N 400101 and on). This circuit uses three 60-minute timers and associated five-minute interval decoders to perform the auto program starts. The 100-kHz clocks for the three timers are obtained from the receiver control circuit (1A4A1). The clock for timer 1 is applied to U67-5 (figure FO-12/2), the first of five cascaded decade counters. The output appearing on U52-7 is one pulse/second. U27 (divide by 10) is the “seconds” counter. U26, programmed to divide by six, is the “ 10's of seconds” counter. U25 and U33 work similarly for the minutes and ten’s of minutes. The other two timers are identical to timer 1. The clock circuits are powered from the +5VB supply generated by the swtiching regulator (1A6A3). This supply has a battery backup so timing synchronization is maintained during primary line power failures. The timers are controlled by run /reset latches, formed by U45, U43 and U34 (figure FO-12/1). U47-10 provides a momentary reset pulse to the minutes and 10’s of minutes counters when the front panel RESET push-button is pressed. Actuation of the ADV TIMER pushbutton increments the minutes counter by the addition of an advance timer pulse from U47-6. U16 through U23 (figure FO-12/3) form four, four-pole triple throw switches that switch the BCD outputs of timer 1, timer 2, and timer 3 to the LED display. The “minutes” outputs of each timer are decoded by 5-minute interval decoders U13, U8 and U9 (figure FO-12/4). These decoders trigger one shots U68 and U7 at the beginning of each 5-minute segment of the hour of their respective timer. When the start of a 5-minute segment is decoded, four-pole, double-throw switches U 12 and U 10 route the BCD outputs of the appropriate timer to U1. U1 converts the four line, BDC, 5-minute segment time code, to a 1 out of 12 code.

4-26. The 12-output lines of U1 (figure FO- 12/4) are connected to the common terminals of 12, single-pole, 4-throw switches on the front panel. U 1 provides a low-going pulse output for approximately 50 microseconds (the period of the one shots U68 and U7) on the line corresponding to the start of the particular decoded 5-minute segment. The front panel switches select which path is initiated for each 5-minute segment of the hour: 0 = no sweep, 1 = Path 1, 2 = Path 2, 3 = Path 3. The three possible path lines (on J5- 16, -2, -15 respectively) are gated by U4 with their respective timer pulse to produce an auto start pulse at U5-6. U2 latches the path code for the 5-minute segment for use by other circuits in the receiver.

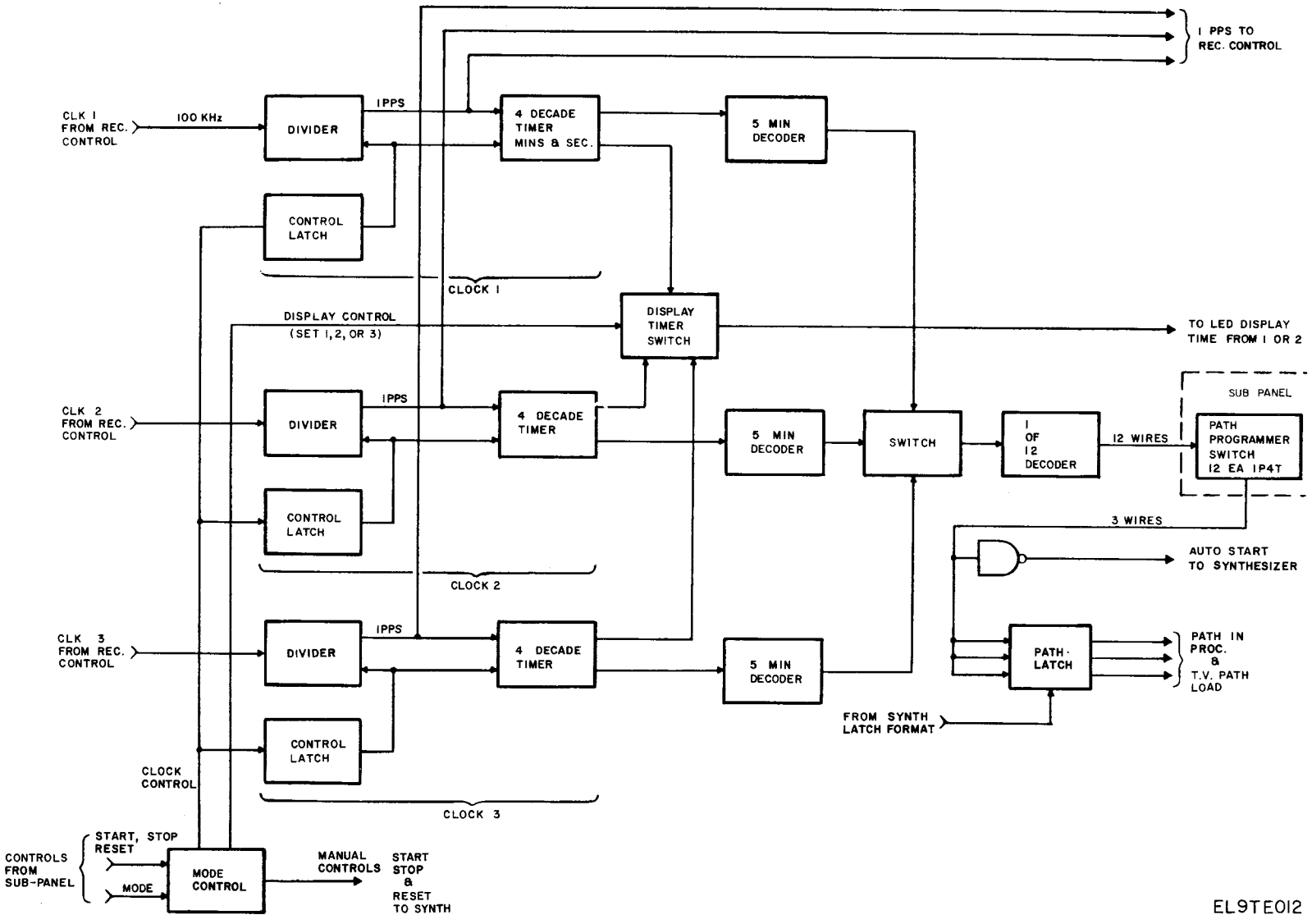


FIGURE 4-4. Block Diagram, 3-Path Programmer CCA.

4-27. RECEIVER CONTROL (figure 4-5 and FO-13) (S/N 400101 and on). This circuit performs various logic functions associated with the operation and control of the RCS-4B. One, it provides a 100-kHz clock for each of the timers of the 3-path programmer with provision for slip synchronization; second, it counts the VCO prescaled "count" signal from the synthesizer to drive the LED display with the receive frequency of the receiver; third, it interfaces with the CRT display logic to put the CRT cursor frequency on the LED display, when requested; and last, it generates commands to automatically select the appropriate preselector filters as the sweep progresses. The preselect filters are located in the 4028 unit.

4-28. The 5-MHz standard enters on J1 and is connected to U51 and U52 (figure FO-13/2) which forms a divide-by-50 yielding a 100 kHz square wave on U52-5. U47, U46 and U39 are decade dividers which divide the 100 kHz to 5, 1, and 0.1 kHz. These three additional rates are used to modify, or "slip" the 100 kHz clocks sent to the timers by 5, 1, or 0.1 percent (fast, medium or slow). The rates are identical to, and controlled by, the same means as the slip rate dividers in the synthesizer. Speeding up or slowing down the basic 100 kHz clock allows the synchronization timing to be advanced or retarded. Add pulses at U35-6 and delete pulses at U35-8 are summed with the 100-kHz clock only when the front panel MODE switch is in Set 1, Set 2, or Set 3 position, and the ADV/RET switch is depressed to add/delete pulses to the selected timer only. All the circuits that provide the 100-kHz clocks to the timers are powered from the +5VB supply from the switching regulator 1A6A3. This supply has a battery backup so timing synchronization is maintained during primary power failure. Auto sync control pulses from the auto sync module are applied to U35-4 and U35-10 to adjust the receiver timing during the auto sync timing search.

4-29. The count signal (f_o) that is input on J3 (figure FO-13/3) is related to the receive frequency 1st L.O. as follows:

$$f_o = \frac{\text{1st L.O. Frequency}}{20}$$

The first L. O. frequency is related to the tune or receive frequency as follows:

$$\text{L.O. Frequency} = \text{tune FREQ} + 40.2 \text{ MHz}$$

The count signal is processed by receiver control circuits to give an instantaneous readout of the receiver sweep frequency. This signal (f. = 2.11 MHz to 3.51 MHz) is buffered by U31-10 and is fed to U40-6. U40 is a digital counter programmed to divide-by-5. A gating control on U40-13 enables the divider for 10-millisecond count intervals. The output of U 40 is sent to a four-decade divide string, U29, U30, U32, and U33. At the conclusion of the 10-millisecond period, the count in the counters is latched in output latches U15 through U8 whose outputs drive the LED display. Counter gating is provided by a 100-HZ signal from the slip rate divider U39-12, which drives U19-1, a divide-by- 2 circuit. The five inverters (U34, figure FO-13/4), which drive U19-13, cause the 10-millisecond on, 10-millisecond off, gate output at U19-7 to be slightly asymetical in time to avoid counter indecision when the synthesizer is set to an integer frequency such as 2 MHz. (The 10-millisecond gate is on approximately 20 nanoseconds longer than the 10-millisecond gate off time.)

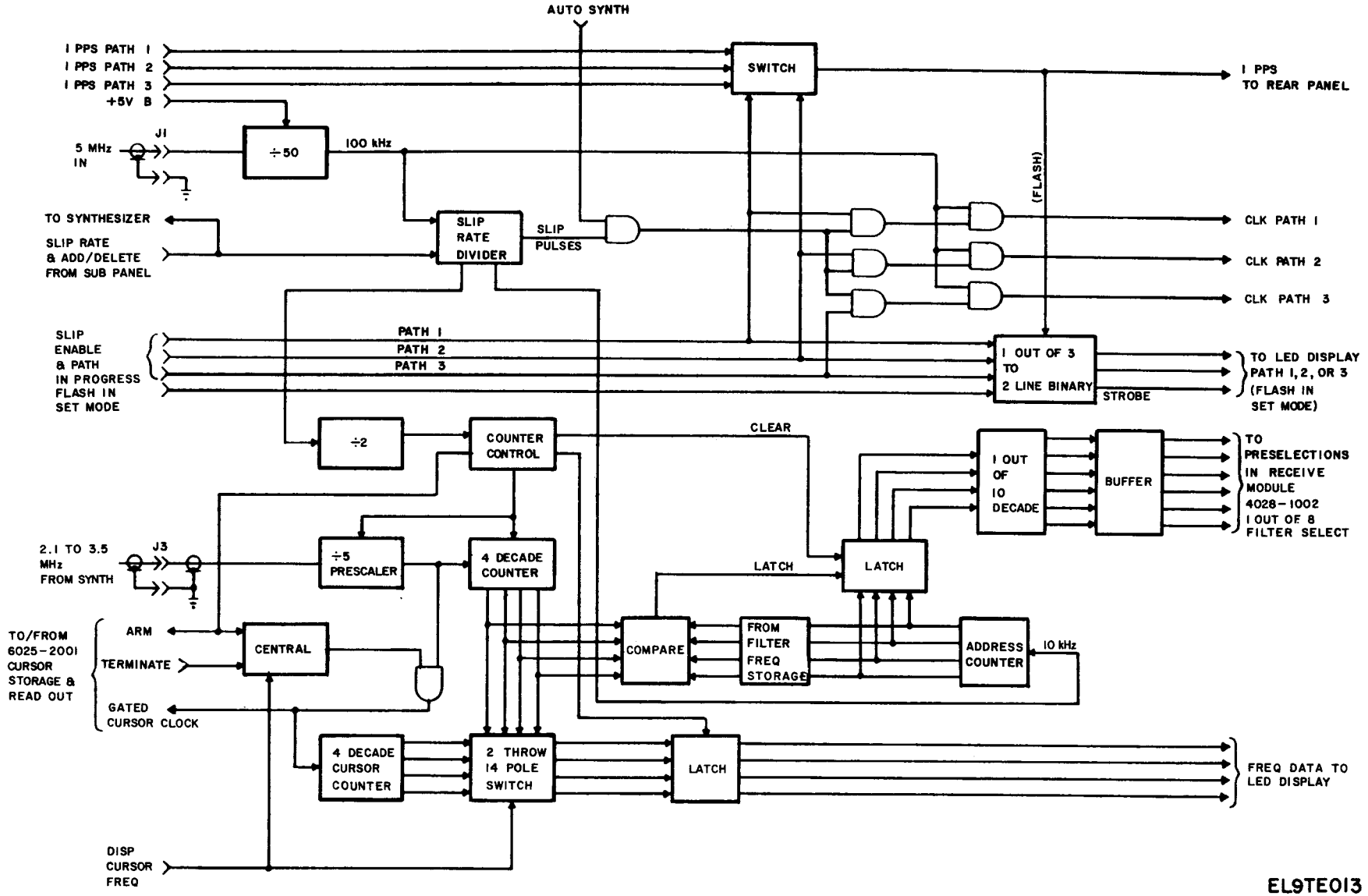
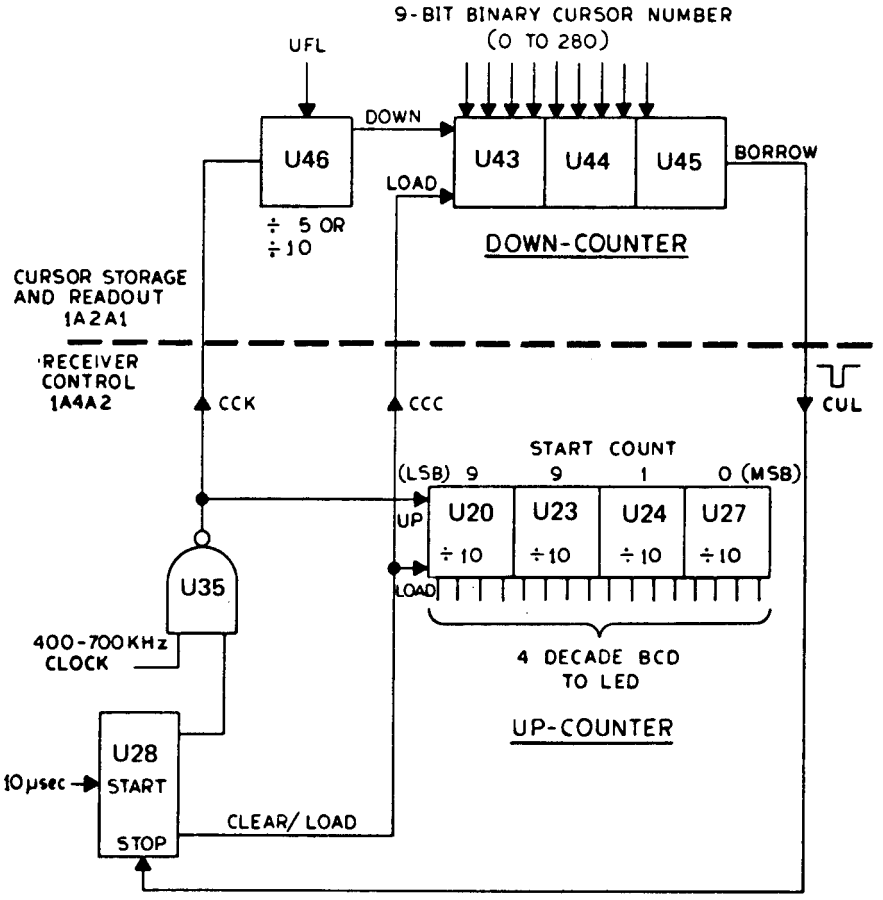


FIGURE 4-5. Block Diagram, Receiver Control CCA.

4-30. The logic for the cursor to frequency conversion is represented in the diagram of figure 4-6. This function is performed by cursor storage and readout (1A2A1) and receiver control (1A4A1) circuits. Every 10-milliseconds, the start/stop flip-flop U28 (figure FO-13/3) gates a clock derived from count divider U40 into BCD up-counters U20, U23, U24, and U27, which are started from count 0199. Each clock pulse advances the counter (U20) by one count of the "10 kHz" decade of the LED display. This clock is also fed simultaneously to binary down-counters (U43, U44, U45) on the cursor storage and readout circuit (1A2A1) which contain a binary number representing the position (along the frequency axis) of the cursor on the CRT display. The number ranges from zero (equivalent to 2.0 MHz) to 280 (equivalent to 30.0 MHz) corresponding to the 280 vertical raster lines of the CRT frequency axis. Each raster line represents a 10 kHz wide segment of the receiver sweep. The binary down counter counts down from the cursor location raster line number to zero while the BCD up counter simultaneously counts up from 0199 (i.e. 1.99 MHz); each clock pulse advancing the count by 10 kHz. When U45 "under-flows", a pulse (CUL) is generated which clears U28, thereby stopping the up-down count sequence. Since the number of clock pulses for the BCD up-counter is the same as for the binary down-counter, the total count added to the BCD preset of 0199 provides the BCD equivalent of cursor frequency. Note that there will always be at least one clock pulse to advance the BCD counter from 0199 to 0200 even when the cursor is at line number "0" (at 2.00 MHz) because the U45 borrow pulse (CUL) does not appear until the binary down counter actually down counts past zero to minus one (- 1). At the end of ten milliseconds the two counters are cleared, the load enable activated, and the count process repeated. The frequency of the moving cursor appears at the outputs of BCD upcounters U20, U23, U24, and U27 every ten milliseconds. Actuating the CURSOR FREQ switch connects the cursor BCD counters to the LED display via the 16-pole switch (U21, U22, U25, U26) and latches U15 thru U18,

4-31. The preselector filter select circuit begins with three, 4-bit magnitude comparators U10, U12, and U13, which compare the count frequency from the frequency counter to the stored upper frequency limit of the filter passband (figure FO-13/4). The filter cut-off frequencies are stored in a programmable-read-only-memory, U11. U6, a 4-bit counter, is used to shift the PROM, U11, through its address codes; each address corresponding to a preselector 1 thru 8. The PROM is shifted through all 16 address codes (only 8 are used) each time the counter is updated, every 10 milliseconds. The PROM frequencies are arranged from lowest frequency to highest. When a "less than flat" emerges from comparator U13-7, U7-9 goes high latching the corresponding filter address code into U5. U2 performs 1 out of 8 decoding. U9 and U4 are high voltage buffers, one of whose outputs goes low (zero volts) when selecting the decoded preselector. The eight preselector filters are selected as follows:

FILTER #	FREQUENCY RANGE
1	2.0- 2.9 MHz
2	3.0 - 4.3 MHz
3	4.4- 5.9 MHZ
4	6.0- 8.3 MHz
5	8.4 - 11.9 MHz
6	12.0 - 16.9 MHz
7	17.0 - 23.9 MHz
8	24.0 - 30.0 MHz



NOTE

Reference designations, as shown, apply to units serial numbered 400101 and on. For units S/N 400100 and before, convert reference designations as follow:

S/N 400101 and on	S/N 400100 and before
U20	U28
U23	U27
U24	U26
U27	U25
U28	U29
U35	U23

EL9TE014

FIGURE 4-6. Simplified Cursor to Frequency Converter Circuit.

NOTE

Decoder truncates (does not round off) frequencies at the 100 kHz decade.

4-32. CRT DISPLAY SECTION

4-33. DISPLAY SECTION DESCRIPTION. The CRT display section contains the circuits that provide the RCS-4B with a bright, high resolution, digitally-refreshed CRT display of chirp sounder record and receiver AGC voltage data. This functional section contains three separate digital memories capable of storing three complete chirp sounder records; one for each path of the 3-path receiver system. Each memory is organized to display 128 points for each vertical CRT raster scan by 280 raster scan lines across the CRT. The CRT employs a high-speed vertical raster (15 kHz) which requires 19.732 milliseconds to complete one full picture of 280 lines plus 16 lines for the horizontal retrace. Timing control within the CRT display circuits divides each memory into 280 segments, corresponding to the 280 second sounder RF frequency sweep. Thus, each raster line represents the data collected over one second of the receiver sweep. The data acquired during one second of the RF sweep is processed by the spectrum analyzer to provide propagation time delay information. Upon command of the CRT display circuits, the spectrum analyzer outputs one spectral scan every second, which corresponds to one vertical raster scan on the CRT display. The spectrum analyzer outputs 200 data points during each spectrum scan which is compressed to 100 points in the CRT display circuits. Thus, the CRT display provides a 100 cell resolution of relative time delay data. In addition, the CRT provides 28 points at the top of the vertical scan for receiver AGC bargraph information. The total stored data displayed on the CRT is 128 x 280 = 35,840 bits. All data is binary (on/off) with no gray scale information. The CRT digital memories are continuously recirculated at high speeds (effective rate of 2.4 megabits/second) to provide a flicker free display with an approximate 50-Hz refresh rate. Due to timing limitations of the dynamic MOS shift registers used for the memory, two parallel half size memories (called odd and even) are used. Thus adjacent points along the 128-bit CRT vertical raster are stored alternately in the even/odd memories (i. e. , bit positions 0, 2, 4, 6. . . in the even memory and bits 1,3, 5,7... in the odd memory). These two memories are time multiplexed such that the individual memories may be clocked at 1.2 MHz instead of 2.4 MHz. All timing functions of the CRT display section are based on this 1.2 MHz memory clock. Since the spectrum analyzer requires 60 milliseconds for its output scan, temporary buffer registers are used which load the 100 bits (cells) of time delay information from the spectrum analyzer (over a 60 millisecond period) and then transfer this data at a 1.2 megabit rate into the main memories. Thus, while each CRT raster line is equivalent to one spectrum analyzer output scan as far as data content is concerned, the actual data rates are very different. The CRT display system also provides six storable cursors which may be displayed over any of the 280 CRT lines for ionogram reference information. The CRT is annotated with frequency tick marks and numerical characters along the horizontal axis which are generated by logic within the CRT display system.

4-34. The display system comprises four circuit card assemblies housed in two modules, and the CRT display assembly in a third module, as shown in the overall block diagram, figure 4-7. The basic timing signals are developed by the timing control circuits (1A2A2). (Refer to block diagrams, figures FO-3 and FO-4.) A 12-MHz clock is divided into two 1.2 MHz timing signals ($\phi 1$ and $\phi 2$) which control the CRT memory readout and display. Clock $\phi 1$ is also used to synchronize the CRT display with the memory loading in assembly 1A3. The CRT scans from the bottom to the top of the display 280 times before making a horizontal retrace (figure 4-8). Each vertical scan displays 128 bits of spectrum and AGC data, stored 64 bits each in the odd and even memories. A vertical trace continues until 64 $\phi 2$ clock pulses have been counted, at which time a flip-flop stops the memory until 16 clock pulses have been counted for the vertical retrace interval. When 280 vertical traces have been counted by the vertical line counter, another flip- flop, establishing horizontal synchronization, inhibits every other clock pulse. Thus, as the horizontal retrace takes place, the "memory timing clocks drop to half speed for 16 vertical traces until the horizontal retrace counter resets the horizontal sync flip-flop. In this period, 1024 bits ((128 divided by 2) x 16) of memory are circulated but not used. Assembly 1A 2A 2 also controls the interface timing with the spectrum analyzer 1A1 which provides the signal input for display. A 1.5 kHz clock from the spectrum analyzer is used to establish a 1-second triggering of the spectrum analyzer output scan. The spectrum analyzer generates a 200-point scan of the spectrum. The display unit loads every second point until 100 bits have been stored in memory. The 100 bits are stored in alternate cells of a buffer memory in Assembly 1A3A2. (Refer to block diagram, figure FO-5.) After 100 bits from the spectrum analyzer have been stored, a switch on 1A2A2 triggers an amplitude-to-time conversion of the AGC level from the receiver. A total of 28 bits can be clocked in for display of up to 60 dB of AGC variation. Circuit 1A2A2 (figure FO-4) also generates the numerals (with a digital character generator) and marks used to display the horizontal frequency axis independent of the data present in the circulating memory.

4-35. The cursor storage and readout circuit 1A2A1 (figure FO-6) provides the memory address pointer establishing which of the 280 memory lines is being loaded by the current spectrum analyzer scan. This spectrum analyzer load line counter is one of eight counters available on a 9-pole 8-position switch which is scanned with each vertical retrace. The other seven positions of the switch are used for display of cursors on the CRT display. The 9-bit spectrum analyzer load line counter in 1A2A1 is compared with the display vertical line counter in assembly 1A2A2. When the two counts are equal, a vertical load-line cursor appears on the CRT display, and the CRT memory (1A3A1) is loaded with the current memory line data from assembly 1A3A2.

4-36. The memory load logic circuit 1A3A2 (figure FO-5) provides the logic for the loading of the CRT display memory 1A 3A 1 and supplies the on-off video signal to the CRT display. The memory load logic provides two static 64-bit buffer memories which temporarily store alternate bits for a line of CRT memory. When the two memories are filled with data from a spectrum analyzer scan and AGC scan, the contents are burst-loaded into the circulating CRT memory at the appropriate point determined by the line counter comparison of assemblies 1A2A1 and 1A2A2. The on-off video data consists of numerals from the character generator in assembly 1A2A2, frequency marks from 1A3A2, or data from

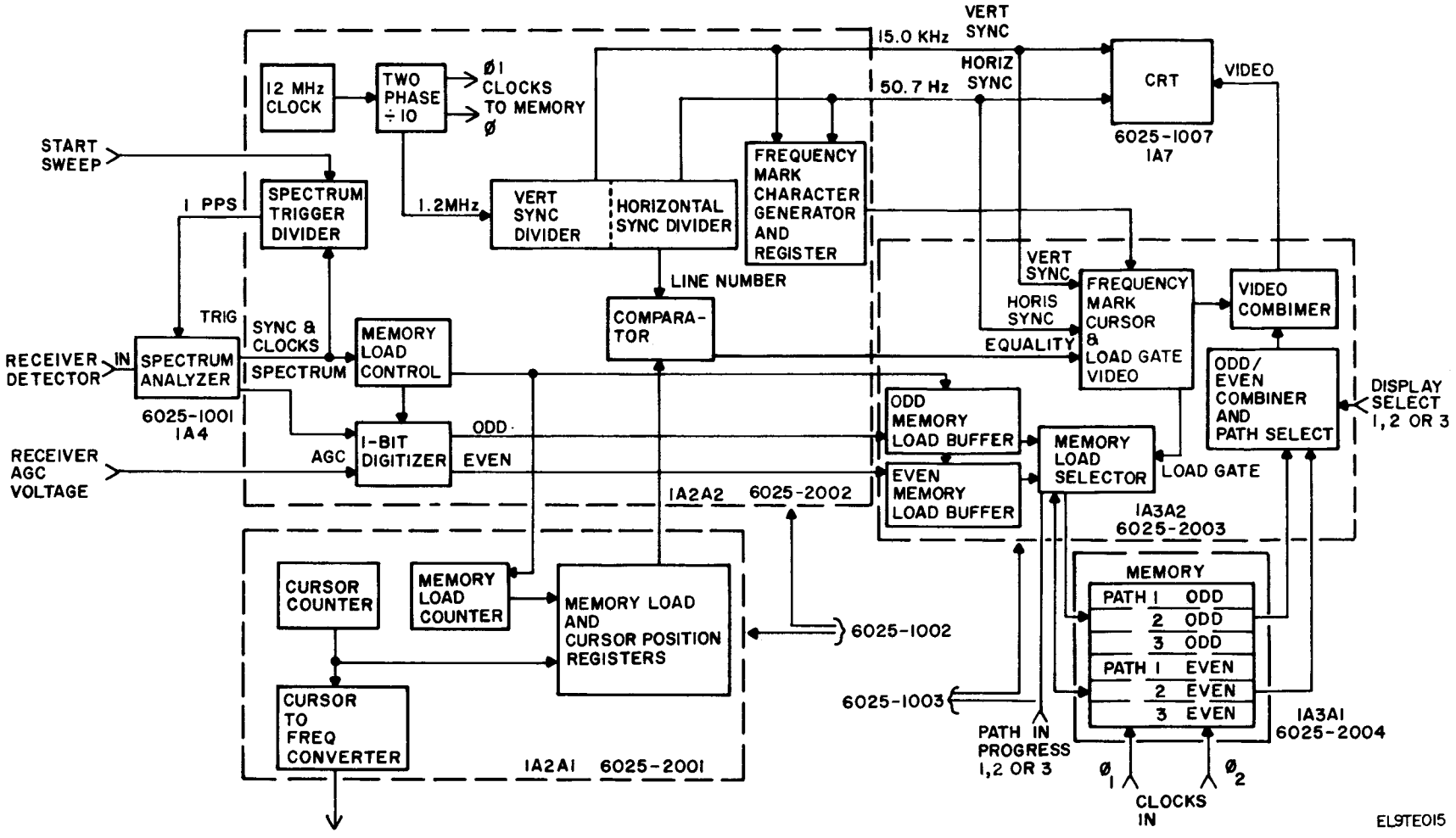


FIGURE 4-7. CRT Display Section Block Diagram.

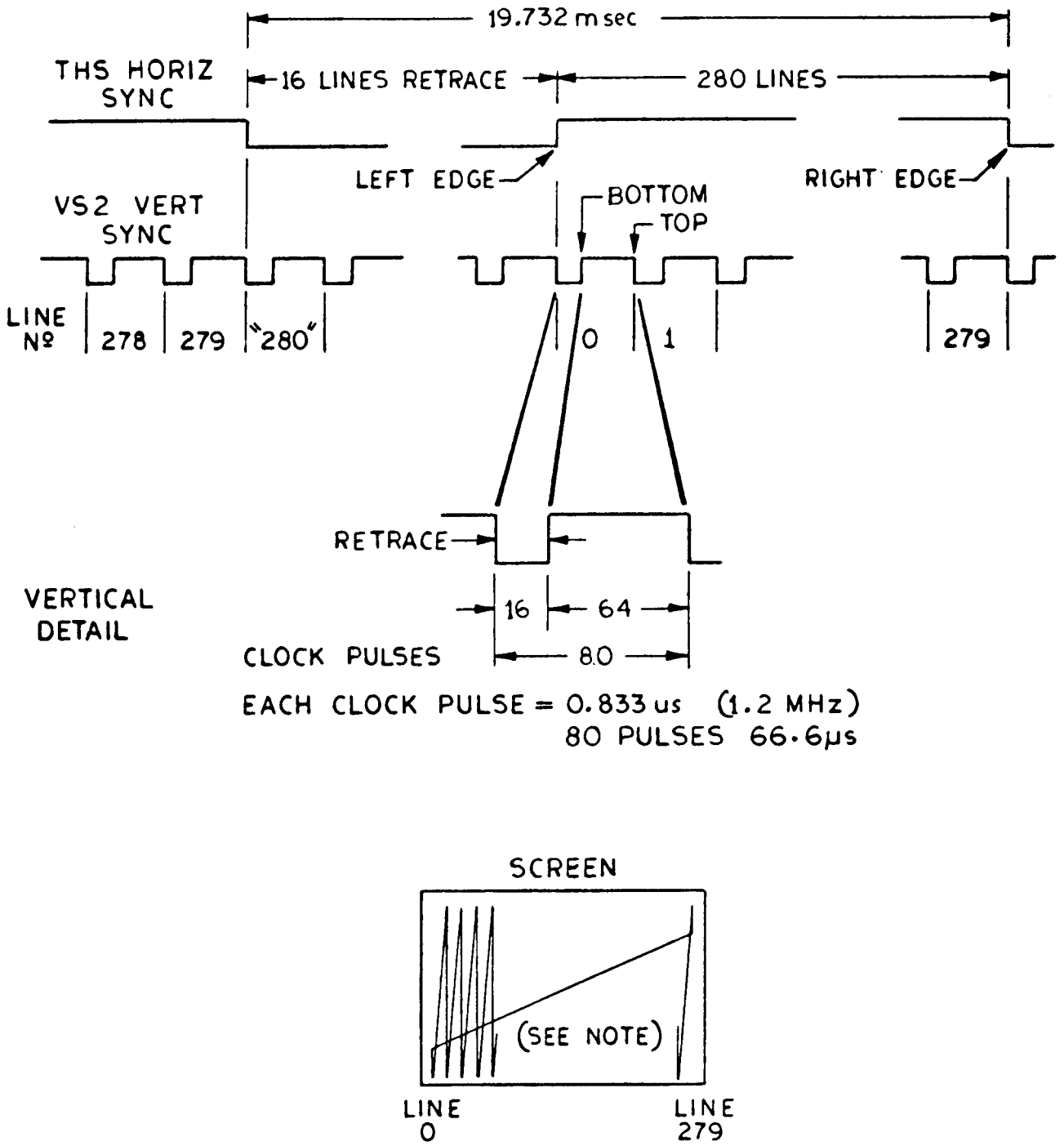


FIGURE 4-8. CRT Display Timing Relationships.

the circulating memory in assembly 1A3A1. Logic is provided so that, if the memory output is high at the point in display where a frequency mark is to appear, the video output goes off and the frequency mark is displayed as a dark line.

4-37. The CRT memory circuit 1A3A1 (figure 4-7) consists of three sets of dual 18432-bit dynamic memory shift registers which circulate the odd and even bits of the display. Each dual memory is capable of storing one complete display picture (sounder data + AGC).

4-38. The CRT assembly 1A7 contains the cathode ray tube and the driver electronics which are located on a circuit card 1A7A 2 within the module (figure FO-18). The circuit card is the interface between the video signal and the CRT. It also provides various CRT controls (e.g., brightness, focus, width) which can be manually adjusted to counter effects of tube and component aging.

4-39. TIMING AND CONTROL ASSEMBLY 1A2A2 (figures FO-4 and FO-15). This circuit performs five major functions:

a. Controls the timing of the CRT memory loading.

b. Controls the timing of the CRT raster.

c. Provides the interface with the spectrum analyzer (1A1) and the 4028 receiver (2A2) which provide the input for display.

d. Provides a count of the vertical line being displayed to synchronize any line update.

e. Generates the numerics for the CRT frequency axis.

All timing is provided by a 12-MHz oscillator (figure FO-15/1). This signal is divided by 10 at two different points. The divide-by-10 U44 provides a continuously operating 1.2 MHz master cIock while divider U28 provides a 2-phase 1.2 MHz slave clock (ϕ1 and ϕ2) for driving the memory circuits. U28 is stopped totally during vertical retraces and runs at half speed during the horizontal retrace to keep the dynamic memory circuits operating and yet conserving unused memory bits. The dynamic MOS shift register memories require a two phase clock drive; ϕ1, the read out clock and ϕ2, the read in clock. These clocks are derived from the slave clock divider U28 and gates U8, U39, and U40. The CRT vertical sync (VS1) available at U40-8 is generated by counting 64, ϕ2, clocks in U48 and U51 and setting flip-flop U40-8. This starts the CRT vertical retrace (Q3-E23) which lasts for 16, ϕ2 clock periods when U40-8 is reset by U42. When U 52-U53-U54 have counted 280 vertical scans, flip-flop U55-11 is set, and the horizontal retrace starts. Because the time for a horizontal retrace is too long to stop the dynamic memories completely, a half speed (600 kHz) clock is generated (by U29-U28) to keep the memory alive and yet conserve bit storage. This enables U49, U52, U50 which counts 512 of the half speed ϕ2 clocks before clearing flip-flop U55-11 and ending the horizontal retrace. U60-12 buffers the CRT horizontal sync pulse (TVS).

4-40. Timing and control circuits (1A2A2) also provide the interface with the spectrum analyzer used as the signal source for the display. Spectrum analyzer triggering is controlled by a divider circuit consisting of U8, U9, and U10 (figure FO-15/4). This divider circuit provides the trigger pulses to the spectrum analyzer at the rate of one per second. Timing is derived from an available 1.5 kHz signal in the spectrum analyzer which is gated to the divider train (U8, U9, and U10) by the RS latch, U1 and U3. When an ionogram start signal appears on U64-3, the output of U1-3 goes high gating the 1.5 kHz signal to U8 where it is divided by 15 to provide a 1OO-HZ clock to programmable dividers U9 and U 10. U9 and U10 are programmed to divide the 1OO-HZ signal by 100, providing 1 pulse per second, stretched by the one-shot U24, to trigger the spectrum analyzer. The spectrum analyzer returns a sync signal to pins 9 and 10 of U1 (figure FO-15/4) when it actually starts an analysis scan. Spectrum analyzer scan start pulses pass through U2-8 to line LC2. This scan start pulse on line LC2 causes the load buffer gate U1 and U3 (figure FO-15/3) to enable two counter trains (a divide-by-128 formed by U34, U35, and U36 and a divide-by-100 formed by U46 and U47) and to set line (SLB) enabling memory load buffers in memory load logic 1A3A2 for inputting new data in the CRT display memory.

4-41. The recirculating CRT display memory is synchronized with the CRT video. To load data into the display memory, two temporary memory buffers are provided in the memory load logic 1A3A2. The loading of the temporary buffers is synchronized with the spectrum analysis scan by a 3.3 kHz clock signal (SAM) derived from the spectrum analyzer. Clock signal (SAM) (figure FO-15/3), is divided by 2 in U33 to provide a clock to count the number of bits stored in temporary buffers. Each display memory is split into an odd and even memory, and each has a separate memory buffer for data input. U33 pins 9 and 8 alternately enable the output of U33-5 to drive the clocks for the two corresponding memory buffers (SRE and SRO). Each buffer on 1A3A2 holds 64 bits, making a total of 128 bits for each CRT display line. The first 100 bits are associated with the spectrum analyzer data input, while the last 28 bits are associated with the AGC information provided by the receiver. The counter U34, U35, and U36 divides the spectrum analyzer clock by 128, while the second counter, U46 and U47, divides the same clock by 100. Both of these counters are held reset at zero until the synchronizing pulse from the spectrum analyzer (LC2) causes them to be enabled. At the same instant, the RS latch made up of U62 and U26 enables digitized data from the spectrum analyzer to pass through U62-3 into the memory buffers (SSD). When counters U46 and U47 reach the count of 100, the spectrum data is shut off and the AGC data is allowed to pass through U62-8 into the memory buffers. When the divide-by-128 counter overflows, the load buffer gate resets, stopping the load buffer action until another pulse appears on LC2.

4-42. The analog spectrum data is converted into digital data by a 1-bit analog-to-digital converter consisting of U43 and U65 (figure FO-15/3). U43 is a standard voltage comparator with an adjustable threshold level. All analog data above the threshold of 3/4 volt causes the output of U43 to be high, while the data below this level causes a low output. Because of the nature of sample timing in the two 64-bit memory buffers, a small narrow spike coming out of the spectrum analyzer could be lost because it would not remain high long enough to be sampled. Thus, U65 is provided as a pulse stretcher to ensure that all spectrum threshold-crossing pulses are long enough to remain within 1 clock

pulse of the memory buffers. The second input to the memory, the AGC information, is converted into a digital form by a voltage-to-time converter. The voltage from the AGC is buffered and adjusted in level by U63 from a zero-volt level with no signal in the receiver to approximately -5 volts with a maximum interest signal in the receiver. This is fed to comparator U 45. The other input of U45 starts at zero volts at the end of the 100 clock pulses counted by U 46 and U47 (i.e., the end of the analog spectrum analyzer data period) and ramps downward to -5 volts in 28 clock pulses. At the time this ramp crosses the voltage present on U45-3, the output (U45-7) goes low; thus the width of the high going pulse at TP5 is proportional to'the amplitude of the AGC voltage. The result on the CRT is a vertical bar proportional in height to the AGC voltage.

4-43. Every other frequency mark on the CRT display is labeled by an electronically generated character at the bottom of the screen starting with “2“ and ending with either "14” or “ 28”, depending on the upper frequency limit. These characters are generated by U21, (figure FO-15/5) which provides a 5 x 7 dot matrix from standard ASCII code. A parallel-in/serial-out shift register memory, composed of U12 through U20, stores the successive digits to be displayed and presents them one after the other to the inputs of the character generator. Each number displayed on the screen consists of two characters (the numbers 2, 4, 6, and 8 are followed by a blank). Depending on what upper limit has been selected (16 or 30 MHz), U12-U20 are correspondently loaded with two different sets of numbers controlled by U7-12 and U27-12. The character generator circuit is synchronized to the TV raster. The whole shift register buffer train and counting circuit is started by a pulse (CGS) which comes from the horizontal synchronizing circuit (U60-10, figure FO-15/2). This pulse occurs at the left edge of the screen at the beginning of the first line of data. This clears flip- flop U23-14 and loads the character shift register (U12- U201). At the second frequency mark occurring after the CGS load pulse, U23 toggles causing the RS latch U26-6 to be enabled. This, in turn, allows a timing pulse (SNG, coming from a vertical retrace interval counter in assembly 1A3A2) to reach the parallel-in /serial-out buffer U22 to load it with the data presented by U21. This loading occurs slightly below the edge of the normal data portion of the CRT vertical trace. Then, a 2.4 MHz clock (from U44-2) strobes U22 to clock out the 7 bits of the first line of the first character. The next CRT trace causes the character generator U21 to output the second vertical line of 7 bits into U22. After the five vertical lines making up each character are completed plus two blank lines for spacing, U21-11 goes high triggering the one-shot U24 to shift the nine register memory one position over presenting the second character to U21. At the end of this shift, flip-flop U23-5 (via the clock on pin 1) goes high. When the second character is completed, U23-5 goes low which resets U26-6 and disables SNG pulses from reaching U22. This condition remains until U23-7 toggles low on every second frequency mark pulse (FMK).

4-44. CURSOR STORAGE AND READOUT (1A2A1). This circuit assembly generates a moving vertical line (spectrum analyzer load line) that corresponds to the current frequency of the receiver sweep. Also, a manually-controlled moving (blinking) cursor is generated that may be positioned anywhere on the CRT by the operator. The moving (blinking) cursor may be replaced by a fixed stored cursor at up to six locations on the CRT. A 9-bit counter (U49-51, figure FO-14/1), limited to counts of 0-279, generates the address of the next line to

be loaded into the CRT memory (1A3A1) . The counter advances one position every time new data is loaded into the CRT memory, typically once per second. Another 9-bit counter, the moving cursor register (up /down counter U 40, U 41, U 48, figure FO- 14/2) , provides the 9-bit address of the moving (blinking) cursor, which may be changed by front panel pushbuttons. Six 9-bit fixed cursor registers (figure FO- 14/4 and FO- 14/5) store the address of the moving cursor when the STORE switch is actuated. U21 through U 38 provide storage for the six fixed cursors. The status of a cursor is determined by the busy register, U23- 8, U26-8, U29-8, U32-8, U35-8, U38-8, one flip flop per cursor.

The busy register shows whether the register is already being used to store a cursor location or is available for a new location to be stored. Control for cursor storage is provided by U 54 and U 55 (figure FO- 14/ 3). When a cursor is to be stored, the RS flip-flop formed by U 54-3 and U54- 6 is set. This allows logic 1's to be clocked into U 55. These logic l's activate CL1 (cursor load 1) to CL6 one at a time until an unused register is found. Then the moving cursor address is clocked into this register, the busy register is set, and a pulse is generated through CLF to clear the RS flip-flop.

4-45. To erase any one cursor, the moving cursor must be positioned on top of the cursor to be erased. To monitor this condition, the locations are checked line by line during each vertical retrace of the CRT display by shift register U 8 (figure FO-14/3). When the ERASE switch is actuated, U8, U52, and U53 compare the address of the moving cursor to those addresses stored in the six fixed cursor registers. If any of these registers contain the same address as the moving cursor address, one (or more) of the lines CE 1 through CE 6 goes low erasing the address from the corresponding register and clearing the corresponding busy register flag.

4-46. A 9-bit, 8-position multiplexer switch (U12-U20, figure FO-14/6) is used to sequentially cycle between the 9-bit outputs of the moving cursor register (U40, U41) , the six fixed cursor registers (figure FO-14/4 and FO-14/5), and the spectrum analyzer load line counter (U50, U51) . During each raster vertical retrace interval, U 12-U 20 is cycled through all eight of its positions by control lines CSB2, CSC2, and CSD2. The 9-bit output of the switch is fed to the 9-bit comparator on assembly 1A2A2 which compares the output of the raster vertical line counter to the output of the 9-bit multiplexer. As the multiplexer cycles through the addresses of the moving cursor (position O) , the six stored cursors (positions 1-6) and the spectrum analyzer load line (position 7) , the comparator on 1A2A2 yeilds a true output if the raster vertical line number equals the stored address of one of the eight display lines. If this happens, an EQT pulse is generated by the comparator which indicates that the raster is now at the same address location as one of the cursors. The EQT pulse is then used to initiate one (or more) of three actions: (1) it causes a cursor line to be drawn on the CRT by logic in 1A3A2, (2) it erases a cursor (1A2A1, figure FO-14/3), or (3) it initiates a memory loading sequence (on 1A 3A 2) to load new spectrum data into the main CRT memory. Description of the cursor to frequency converter circuit (U43-U45, figure FO-14/2) is provided in paragraph 4-30.

4-47. MEMORY LOAD LOGIC (1A3A2) . This circuit provides the logic for loading the CRT recirculating memory and outputs the video signal to the CRT.

Much of the logic activity is established during the vertical retrace interval. The vertical retrace interval takes 16 clock pulses. The three most significant bits of counter U42 in assembly 1A2A2 (FO-15/1) are fed to Ul (figure FO-16/4) on lines CSB1, CSC1, and CSD1.

U 1 is used as a one-out-of-eight decoder which provides individual pulse outputs in synchronism with the one-out-of-eight multiplexer switch (U 12-U 20) in assembly 1A2A1. If new spectrum data is to be loaded into the memory, an EQT pulse is generated by timing and control circuit 1A 2A 2 indicating when the raster line (and therefore, the memory) has arrived at the address location corresponding to the new data to be loaded. The EQT pulse is applied to latch U 3-2. When U 1 reaches " 7", the output on U 1-9 goes low enabling a strobe pulse coming from U8-9 to clock U3. The strobe occurs in the middle of the EQT pulse. The output on U3-5 is fed via U12-6 and U14-12 to a cursor gate at U17-1 to draw the load line on the CRT. The output on U 3-5 also becomes the spectrum analyzer load control line, SAL. The SAL signal remains high for the one CRT vertical line having the same address number as the spectrum analyzer load line register. This is used to synchronize the loading of the data from the buffer memory into the high speed circulating memory.

4-48. The dual 64-bit memory buffers (figure FO- 16/2) consisting of eight, 16-bit shift registers, U 26 through U 33, are loaded at a slow clock rate controlled by the spectrum analyzer sync gate, SLB. When this signal is high, meaning that a spectrum analyzer scan is in progress, alternate odd and even clocks are gated into the clock lines of each of the corresponding odd or even memory buffers by switch U 25. The data from the spectrum analyzer and the AGC data from the HF receiver are presented on the serial data line SSD to both 64-bit shift register buffers. The clocks appear alternately on U 26 through U 29 and U30 through U33. After 128 pulses (or 64 alternate pulses to each group) are completed, the SLB line falls clocking the outputs of U21- 5 high and U21- 6 low . The next time that the SAL signal goes high, indicating the CRT vertical raster line equals the spectrum analyzer load line, U22 is clocked and U22- 9 goes high. This causes the load /recirculate gates (figure FO- 16/3) to switch the main memory from the recirculate mode to the load mode. (For example, U44- 11 and U51- 6 are disabled, while U40- 6 and U 49-6 are enabled.) Note that there are three memory pairs (odd and even): path 1, Ml and M2; path 2, M3 and M4; and path 3, M5 and M6. (This description follows only path 1 for simplicity.) At the same time, U24- 11 applies 1.2 MHz $\phi 1$ clock pulses to the eight memory buffers to shift their contents out into the circulating memory (via U 40-4 and U49-4) . At the conclusion of the load period, the SAL signal falls clocking U21- 13 which clears U22- 14 shutting off the load sequence and restoring normal memory recirculation.

4-49. A 2.4 MHz clock is derived by applying $\phi 1$ and $\phi 2$ to an RS flip-flop (U24) and using pins 6 and 3 to control a switch which alternately feeds the outputs of the odd memory and even memory to the video line for one-half of the normal 1.2 MHz clock. The memories are read out alternately. The rising clock edge of U43- 11 causes the odd data present at U 43-12 to be transferred to U 47-13. At the falling edge of the clock, U 43 is cleared at pin 13. As the clock at U 43-3 rises, even data at U 43-2 is transferred to U 47-1 and U 47-2. The falling edge of the clock at U 43-1 clears this flip-flop. Thus, in 1.2 MHz memory clock

period, one memory is read in and presented for half of the clock period, and then the other memory is read for the other half of the clock period, producing an effective 2.4 MHz bit rate at U 47-12 to be presented to the memory video circuit.

4-50. Frequency marks are generated for every 20 vertical TV lines which is equivalent to each MHz in the 2-16 MHz format or each 2 MHz in the 2-30 MHz format. A counter formed by U 5 and U 11 (figure FO- 16/4) divides by 20 the vertical sync pulses (VS 1) , which occur for every vertical line, enabling a frequency mark flip-flop U20 to be set every 20 lines. The frequency mark information is available for the full vertical scan at U 20-6. This in turn is gated into the video of the CRT at U17- 11. At the start of each CRT raster line, a 2-microsecond gate signal provided at U 9-7 enables the lower frequency mark to appear on the screen. A second one- shot output on U 9-10 enables the frequency marks to appear at the top of the screen after 63 microseconds of vertical scan time. The frequency mark data causes U15- 8 to go high, resulting in a white output on the screen. The screen could also be white as a result of noise or AGC data thus obliterating the frequency marks. However, U 15 and U 16 comprise an exclusive-or circuit to ensure that the frequency marks appear as white-on-black or black-on-white depending on the other signal inputs to the CRT video combiner (U15 and U16) . Characters appear at the bottom of the CRT display as a result of any input to U17- 10 on line PNG from assembly 1A2A2. All cursors, moving, fixed, or load, are combined at, and then gated to, the CRT by U 17-3. The video information from the CRT memory comes from line MVO which contains the combined circulating CRT memory data. This data is gated onto the screen from U 17-6.

4-51. CRT DISPLAY MEMORY (1A3A1) . This circuit contains three, 36k-bit memories consisting of 36, 1024-bit MOS shift registers each and associated clock drivers. The complete circuit is repeated three times, one for each path.

NOTE

The circuit for only one path is shown in the schematic diagram, figure FO-17.

The memory for each path is divided into two banks of 18 x 1024 bits. Both banks are loaded at the same time. The data enters at odd and even inputs MI 1 and MI 2, respectively, and is clocked into the memory by $\phi 2$ at 1.2 MHz. Memory clock $\phi 1$ which clocks the data out (MO1 and MO2) operates 180° out of phase with $\phi 2$ as depicted by the inset waveform (figure FO-17). Normally, the three banks of memory, each containing one complete CRT path display, continually circulate via the gating logic from the memory load logic circuit (1A 3A2) . When new data comes in, it is gated in place of that path's circulating memory. Therefore, as long as primary power to the receiver remains on, the most recently received path data is always available for display. (The standby battery supply does not refresh the memory in the event of primary line failure.) The 2-phase memory clock is buffered by transistor clock drivers to provide an approximate +10 to -6 volt clock swing required by the MOS shift register memory.

4-52. CRT DISPLAY (1A7) . The CRT display is a standard raster TV monitor consisting of a cathode ray tube and drive electronics in a replaceable module. The CRT is sealed to protect it from shock and vibration and to minimize possibility of arcing for airborne operation. The CRT display drive circuit provides video input amplification, raster trace waveform shaping, and yoke drive current. In addition, the circuit provides adjustments whereby various parameters (e. g. , brightness, width) can be manually controlled to counter effects of tube and component aging. The timing relationships for the CRT display are depicted in figure 4-6. Note that the raster is turned 90° from what is normally expected on a display tube. The CRT operates from a single +12 VDC supply and generates all other required supplies (+26V, - 120V, +340V, and +9kV) from its own transformer (T 1) .

4-53. STANDBY BATTERY SUPPLY , 1A8

4-54. Either one of two different types of standby battery supply assembly is used in the RC S-4B. Some receivers have a non-rechargeable battery supply (P/N 6025- 1008) that uses standard D-cell batteries. Other receivers have a rechargeable supply (P/N 6025- 1018) that includes an integral charging circuit and uses sealed lead acid cells. Different checkout procedures are used for the supplies and are described in paragraph 5-15.

4-55. NON-RECHARGEABLE SUPPLY (P/N 6025- 1008). The non-rechargeable battery consists of 18, 1. 5-volt batteries. The supply (approx. 29 to 15 volts depending on battery condition) is used to drive the swtiching regulator and the crystal oscillator located in the frequency standard module 1A 3 if the main power is interrupted. A test circuit, located on the programmer circuit card 1A 2A 1, measures the output voltage of the battery supply and yields the results necessary to drive the front panel indicators. A 5-amp fuse, located within the supply, provides protection for inadvertent shorts.

4-56. RECHARGEABLE SUPPLY (P/N 6025-1018) . The rechargeable battery supply (figure FO- 22) is used to maintain timing synchronization, blanker frequency memory and the 5 MHz frequency standard in the event of power cut-off. The supply consists of 12 sealed lead/acid batteries, rated 2-volts each, and a voltage regulator circuit card. The supply is contained in a sliding drawer. Standby power of 28-volts DC is supplied to the 5 MHz frequency standard and to a switching regulator which provides +5 volts DC to the programmer timers.

4-57. The regulator card, mounted in the battery box, receives unregulated +35 VDC input from the 4028 power supply. Voltage regulator U 1 (figure FO- 22) is set to output exactly 28.9 VDC by potentiometer R 3. The resulting 28.9 volts at TP1 provides a precise terminal voltage (28.2 volts) for the batteries at the manufacturers recommended trickle charge rate of approximately five milliamps. The 6.8 ohm resistor, R4, limits the charging current to a safe value (400 mA max.) when the batteries are discharged. The 2-amp fuse, F2, prevents severe physical damage to the system wiring harness or battery box if an inadvertent short occurs on the 28 volt line. Fuse FI protects the 4028 power supply from shorts in the battery charging circuit. Permanent damage to the batteries may occur if they are allowed to completely discharge to 0 volts. Relay coil (K 1) and zener diode (VR 1) sense the battery voltage. If the voltage drops below 17 volts, relay K 1 drops

out (opens) removing the battery load. Turning the AC line power to the 4028 back on automatically resets (closes) the relay and activates the battery charger circuit to recharge the batteries. Depressing switch S1 forces the relay to drop out when the batteries have normal charge and the AC line power is off. This allows the batteries to be disconnected from any load for long term storage.

4-58. NUMERIC DISPLAY, 1A9

4-59. The numeric display is a 9-digit, 7-segment LED display consisting of two groups of four digits (frequency and time) and one path digit. The first group (LED 1 thru 4) displays program time elapsed in minutes and seconds and has a fixed colon (CR1 and CR2, figure FO- 19) separating the minutes from the seconds. The second block (LED 5 thru 8) displays frequency in megacycles to 10 kHz resolution. The decimal point is permanent and is placed at the start of the third digit (activated by R65 to ground). The path digit (LED 9) displays the actual path being received, and is independent of the path selected for CRT display by the CRT (memory) control pushbutton. When the mode select switch is in one of the SET positions (i.e. , a path timer under manual control) , the path digit flashes. The LED display is driven by nine BCD-to-7 segment decoder drivers (figure FO-19/2). The two blocks of four drivers accept positive true BCD time and frequency information from the 3-path programmer (1A 4A 1) and receiver control circuit (1A 4A2) , respectively, and translate it to 7-segment negative true outputs for the common anode LED readouts. The lamp test line causes all LED display segments to illuminate.

4-60. SUB PANEL CONTROL, 1A10

4-61. This assembly includes most of the control switches for the 6025 unit. Operation of the switches is described in section 3. This module may be removed from the chassis for troubleshooting bv first removing the five casting modules from the unit. Mounting screws for the sub-panel are on the bottom of the unit with additional nuts on both sides. Once removed from the chassis it is then possible to remove the four socket-head screws on the front to access the switches.

4-62. ENCLOSURE ASSEMBLY, 1A11

4-63. The enclosure consists of a chassis, front panel and rear panel assemblies. Internal wiring and cabling are part of the front and rear panel assemblies. The rear panel mounts the voltage regulators, (three terminal IC'S in T03 cases), a cooling fan, and the input/output connectors. Interconnections of the unit are defined in Section 2. Front panel controls are explained in Section 3. A schematic diagram for the regulators and fan circuit is provided (figure FO-21). The DC voltages required by the 6025 (unit 1) are generated in the 4028 (unit 2) . Voltages as input to the 6025 are unregulated. U1 through U5 are 5-volt, 3-amp regulators. U6 through U10 are +12-volt, 1-amp regulators. U11 and U12 are - 12-volt, 1-amp regulators.

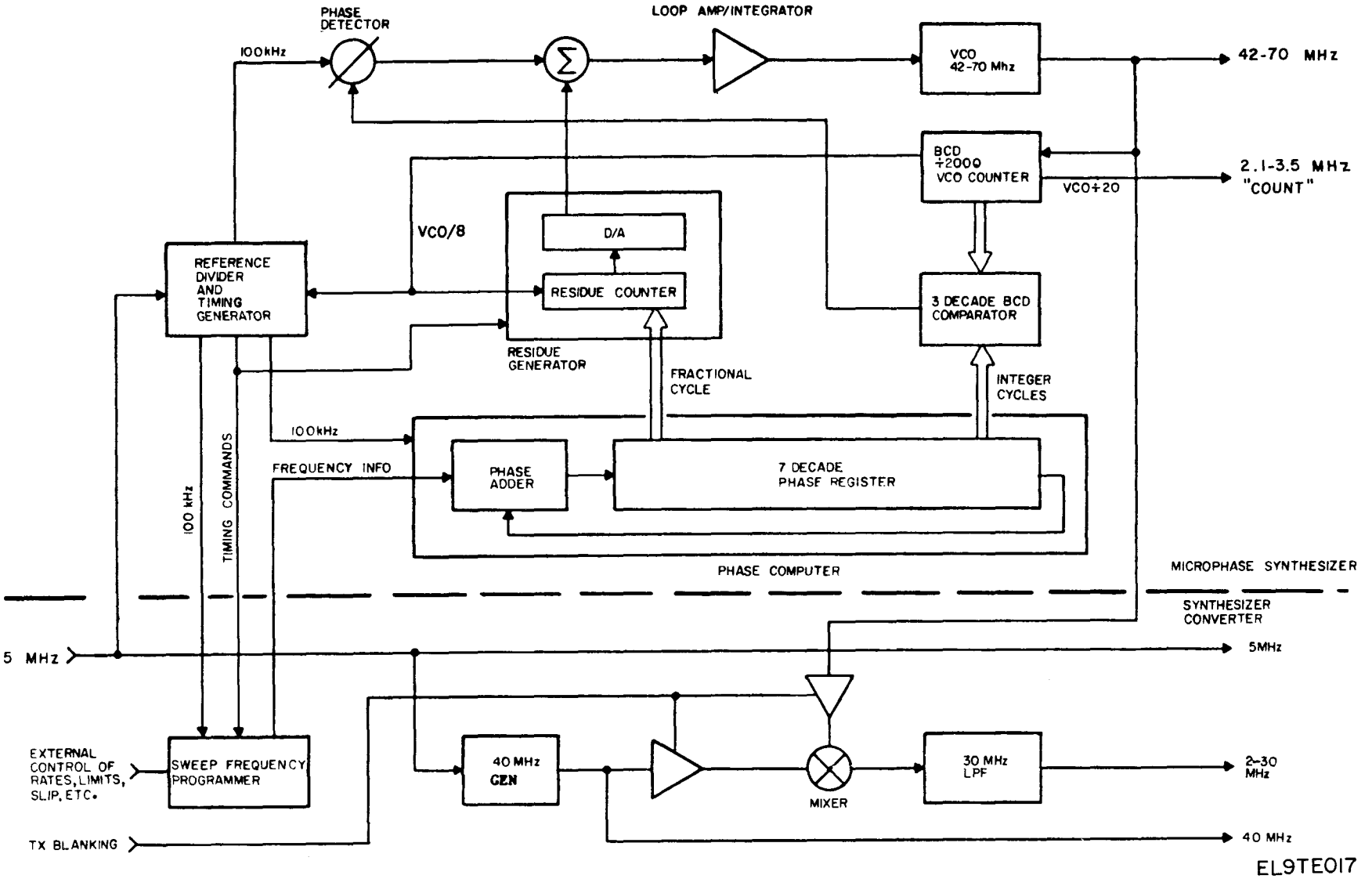
4-64. 4028 HF RECEIVER - Unit 2

4-65. The HF receiver unit consists of three principal assemblies: the sweep synthesizer, receiver, and power supply. The receive antenna (figure 4-1) is selected by the antenna switch and applied to one of eight preselector bandpass filters. The filtered RF is then amplified, filtered and translated to baseband and audio signals. The receiver has bandwidths of 500 Hz and 5 kHz. The baseband signal is sent to the spectrum analyzer in the 6025 unit. Additionally, the receiver translates the same baseband information to an audio band starting at 700 Hz which is applied to a speaker for operator monitoring. The receiver frequency tuning is determined by the sweep synthesizer. Ranging from 42.2 to 70.2 MHz, the local oscillator is 40.2 MHz higher than the tuned frequency. The first LO is filtered by a bandpass filter before going to the receiver. The synthesizer receives a 5 MHz reference and the start, stop, reset, sweep rate, and frequency-limit programming from the 6025 unit.

4-66. SWEEP SYNTHESIZER (2A1) (P/N 5030-1001 Only) (figures 4-9, FO-23, and FO-24). The sweep synthesizer consists of two circuit card assemblies: the microphage synthesizer, operating between 42 and 70 MHz, and the synthesizer converter, which offsets the microphage output by 40 MHz to produce the 2-30 MHz sweep. In addition, the synthesizer module has two fixed frequency outputs, 5 and 40 MHz, used in the receiver, and a 2.1- 3.5 MHz count output used by the frequency counter logic. Logic to control the frequency programming of the synthesizer RF sweep is contained on the converter assembly. This logic digitally increments the synthesizer frequency program every 20 microseconds to produce a linear frequency sweep. External control inputs to the synthesizer converter logic provide means to start, stop, reset, and blank the sweep and to select sweep limits and rates. Transmit blanking of the 2-30 MHz output is implemented by disabling the 40 MHz mixer conversion of the 42-70 MHz signal. All synthesis operations are based on an externally supplied 5 MHz standard.

4-67. The synthesizer module may be used without modification in either the receiver or transmitter. For TCS-4B applications the 2-30 MHz output is used directly to drive the 5018 RF amplifier. For RCS-4B applications, the basic RF sweep is offset 200 kHz higher to produce a 42.2-70.2 MHz receiver 1st L.O. from the microphage synthesizer and a 2.2-30.2 MHz receiver calibration signal from the synthesizer converter. Selection of transmit or receive frequency formats is provided by a digital programming line in the unit wiring harness connecting to the sweep synthesizer assembly.

4-68. The sweep synthesizer uses a single digital phase-lock loop (PLL) design employing a fractional phase computation technique that provides a phase-continuous (coherent) output sweep with 2 Hz frequency resolution. The fractional phase computation technique is a hybrid approach that combines the operation of a conventional phase coherent, high frequency, low resolution, PLL synthesizer and a digitally controlled, low frequency, high resolution, direct phase computation waveform generator. The result is a PLL synthesizer capable of locking properly with a continuously changing programmed phase error within the loop. The programmed phase error capability of this hybrid loop extends the frequency resolution of the basic PLL by almost five decades.



4-9. Synthesizer Block Diagram.

4-69. The basic microphage synthesizer phase-lock loop (figure 4-9) consists of a voltage controlled oscillator (VCO) having a frequency range of 42 to 70 MHz, a loop amplifier/integrator, a phase detector, and a counter/divider/comparator string. This basic synthesis loop is capable of synthesizing any frequency between 42 and 70 MHz in 100 kHz steps as determined by the effective divide ratio in the divider between the VCO and the phase detector. That is, for the VCO to operate at 45.1 MHz, the divider must divide by 451 to achieve the required 100 kHz output for the phase detector. (The phase detector reference is 100 kHz.) Another way of considering this loop is to note that during the 10 microsecond period of the phase detector reference, the VCO must advance exactly 451 cycles (zero crossings) if the loop is to lock properly. To synthesize 45.15 MHz with this loop would imply 451 1/2 cycles of phase every 10 microseconds. By adding additional logic to the basic loop, the snythesizer can operate properly by processing for the integer (451) and fractional (1/2) cycle of phase information. For example, for the synthesizer to operate continuously at 42.123000 MHz, the phase (i. e., VCO zero crossings) must advance 421 whole cycles plus 23/100 fractional cycles every 10 microseconds. A phase computer computes both the exact whole number and fractional number of phase cycles of the programmed frequency occurring in a 10 microsecond period. The result of this phase computation is then added to the stored phase value from the previous 10 microsecond frame. For example, assume a continuous frequency of 42.123 MHz, and a phase register initially at zero. During the first 10 microsecond frame, the phase computer calculates 421.23 cycles of phase. For the second 1.0 microsecond frame, the VCO advances another 421.23 + 421.23 = 842.46 total cycles by the end of the second frame. Similarly, for the third frame, The phase is advanced to 842.46 + 421.23 = 1263.69, and so on.

4-70. The synthesis loop operates by comparing and changing the VCO output phase to equal that of the phase computer for both integer and fractional cycles. Integer cycles (e.g., 421) of VCO phase are controlled by conventional phase-lock loop techniques employing a high speed BCD counter and digital phase detector. The fractional remainder of VCO phase (e.g., 0.23) is handled by the residue generator. The residue generator is a digitally programmed waveform generator, controlled by the phase computer, that corrects the output of the loop phase detector for the remaining fractional cycle phase error occurring every 10 microseconds. It is this programmed, fractional cycle, phase error correction capability that allows the loop to operate to a much finer frequency resolution than can normally be expected from a conventional (integer cycle) phase-lock loop . Thus, in this example, while the integer cycle BCD counter accumulates an additional 421 cycles every 10 microseconds, the residue generator corrects the phase detector by O, .23, .46, .69, etc. cycles every 10 microseconds to produce a VCO output frequency of 42.123 MHz or 23 kHz offset from an integer 100 kHz point. The ability of the residue generator to correct the loop is limited only by the accuracy of the residue correction waveform. In the sweep synthesizer assembly, this correction is made with sufficient accuracy to provide 2 Hz frequency resolution with spurious signals typically greater than 50 dB below the fundamental.

4-71. SWEEP SYNTHESIZER (Part Number 5030-1101) (Refer to figures 4-10 and 4-11). The sweep synthesizer 2A1 is a modular, digitally controlled, phase-locked-loop synthesizer that generates the linear RF sweep.

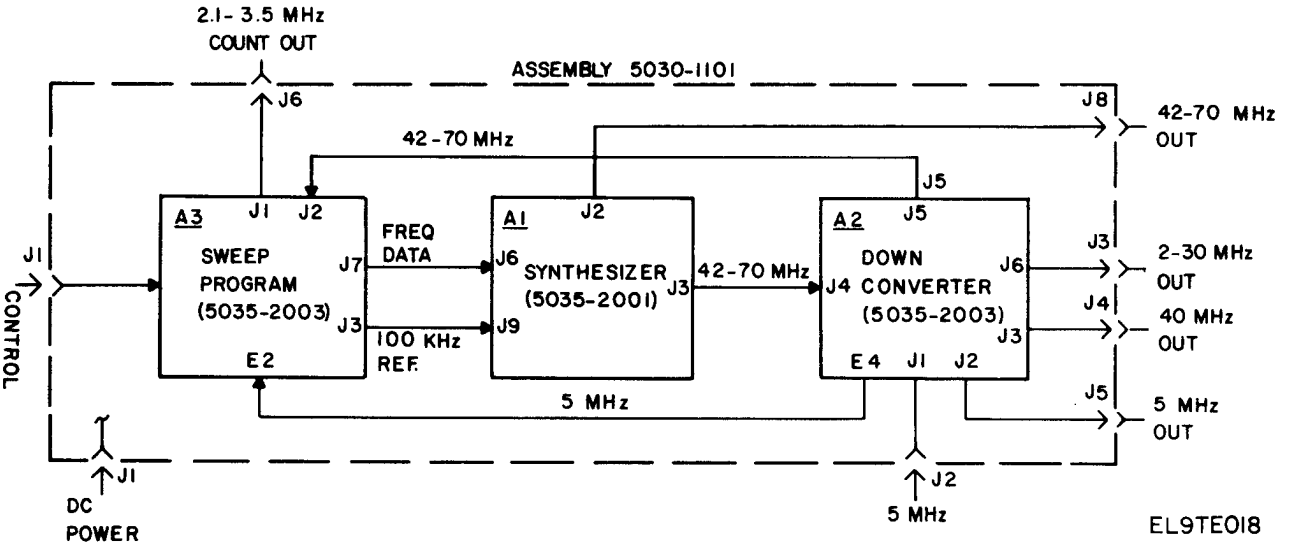


FIGURE 4-10. Sweep Synthesizer (2A1) Functional Block Diagram (Part Number 5030-1101).

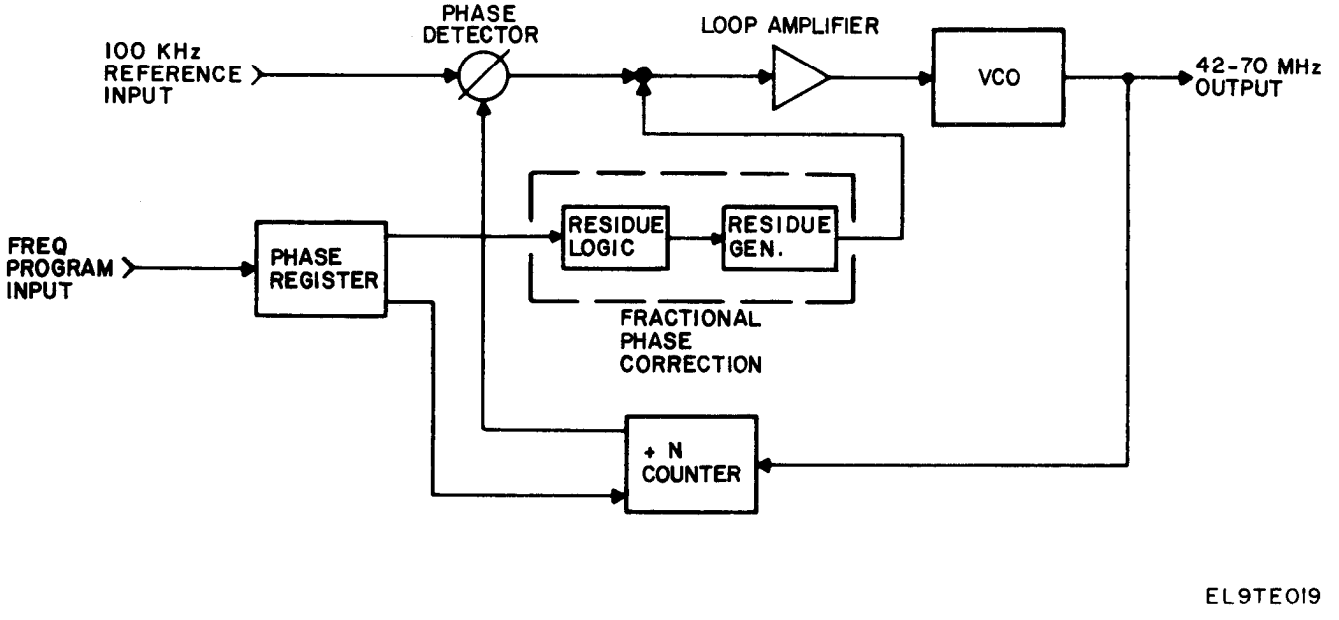


FIGURE 4-11. Simplified Block Diagram of Synthesizer CCA 2A1A1 (P/N 5035-2001).

NOTE

The synthesizer module is used interchangeably in both transmit (TCS-4B) and receive (RCS-4B) applications. A programming line in the instrument wire harness determines whether the synthesizer operates in the transmit or the receive mode.

The sweep synthesizer module has five RF outputs: (1) the 42-70 MHz first mixer L.O. injection for the receiver; (2) the 40 MHz second L.O. receiver injection; (3) a buffered 5 MHz from which the receiver third mixer L.O. injection is derived; (4) the 2.1- 3.5 MHz count output which is used by the frequency counter in the TCS-4B transmit logic, or RCS-4B receiver control logic to drive the front panel LED frequency display; and (5) the 2-30 MHz transmit sweep output which drives the TCS-4B RF power amplifier or the RCS-4B receiver calibrator circuits. The one RF input to the sweep synthesizer is the 5 MHz frequency standard signal from which all RF outputs are derived. The synthesizer digital inputs select parameters such as: sweep rate and limits; sweep start, stop and reset; RF blanking; slip; auto sync and RF output power level. The module consists of three circuit card assemblies: synthesizer 2A1A1, down converter 2A1A2, and sweep programmer 2A1A3.

4-72. SYNTHESIZER (figures FO-25 and FO-26). The 5035-2001 synthesizer circuit (2A1A1) is a digitally programmed, phase-locked-loop synthesizer capable of generating any frequency between 42 and 70 MHz to 1 Hz resolution. It consists of a 42-70 MHz VCO, a programmable divider (divide-by-N), a phase detector and loop amplifier, and control logic (phase register and timing generator). Figure 4-11 is a simplified diagram of the circuit. A detailed functional block diagram is in figure FO-25.

a. The output frequency of the VCO (and the synthesizer) is determined by electrically tuning the VCO with a control voltage from the loop amplifier. The loop amplifier produces this control voltage by integrating (smoothing) the phase-error signals generated by the phase detector. If there is no phase error, the output of the phase detector is zero and the loop amplifier will hold the VCO at its existing frequency. If there is a phase error the phase detector will drive the loop amplifier to change the VCO frequency until the error is corrected. The synthesizer uses the phase detector to compare the output of the divide-by-N counter with a fixed 100 kHz reference signal. If the phase or frequencies of these two signals do not match, the phase detector will drive the loop amplifier to adjust the VCO frequency until the divide-by-N output exactly matches the 100 kHz reference, thereby achieving phase lock. The VCO output frequency is always N times 100 kHz. There are N cycles of the VCO output for every one cycle of the 100 kHz reference. If N is an integer number, the VCO frequency will be an exact multiple of 100 kHz. However, if N is a number consisting of both integer and fractional components, intermediate frequencies between 100 kHz points may be synthesized. For example, to produce a 43.5 MHz output the divide-by-N counter must divide by 435. If an output of 43.501 MHz is desired, the required divide ratio is 435.01. The divide-by-N counter, however , is a 3 decade counter only capable of dividing by integer numbers between 400 and 700. To divide by 435.01 the phase register circuitry programs the divide-by-N to divide by 435 for 99% of the time and divide by 436 for the remaining 1%. The resulting average divide number is

$$\frac{(99+ 435) + (1 + 436)}{100} = 435.01$$

b. Because the synthesizer basic timing reference is 100 kHz, the divide-by-N counter completes a count sequence (frame) every 10µs. In the above example the divide-by-N will count 435 VCO cycles (zero crossings) for ninety-nine 10µs frames and 436 cycles for one frame. The phase detector and loop amplifier will then try to drive the VCO to operate at 43.50 MHz for 990µs and at 43.60 MHz for 10µs. The resulting VCO output is a phase modulated signal with an average center frequency of 43.501 MHz with 1 kHz sidebands. The 1 kHz sidebands result from the jumps in VCO frequency occurring every one millisecond (990µs + 10µs = 1 ms). The amplitude of the sidebands can be reduced by smoothing the jumps in frequency such that the VCO remains steady at the average frequency and does not follow the loop back and forth between the two programmed frequencies. However, to reduce the sidebands to an acceptable level (-50dBc) would require smoothing (slowing) the loop response to such an extent that the synthesizer would no longer be suitable for sweeps used in Chirp sounder applications. These sidebands may be cancelled however, using a fast loop and a fractional phase correction circuit operating in conjunction with the divide-by-N.

c. Since the average frequency of the VCO is correct, the average value (or DC component) of the VCO control voltage from the loop amplifier is correct. The undesired 1 kHz sidebands are produced by the sudden phase errors generated when the divide-by-N counter jumps between the two programmed integer divide numbers. This produces a small momentary change in the VCO control voltage which modulates the VCO frequency resulting in sidebands. The fractional phase correction circuit cancels the VCO modulation by injecting a compensating phase error correction signal into the loop amplifier to counteract the effect of the phase error jump when the divide-by-N skips from one divide ratio to another. The phase register keeps track of when to skip the divide-by-N from one divide-ratio to the next and simultaneously programs the residue logic of the fractional phase correction circuits. The residue logic, in turn, drives the residue generator, which produces the residue fractional phase error correction signal. By careful alignment of the residue generator the synthesizer sidebands can be suppressed better than 50 dB below the fundamental output level. The divide-by-N counter consists of a VCO prescaler which typically divides the VCO output frequency by 2. The prescaler also contains a pulse skipper circuit that makes the divide-by-2 circuit skip one extra VCO clock pulse each time a skip command is given. This effectively turns the prescaler into a divide-by-3 circuit during a skip command. The output of the VCO prescaler drives the VCO divider. The combination of the VCO divider and the VCO prescaler is capable of dividing by any integer number between 400 and 700. For example, to divide by 437, the VCO counter down counts 430 times and the VCO prescaler skips 7 extra VCO clocks during the count sequence, yielding a total count of 437. The phase register accepts binary-coded-decimal (BCD) frequency program data from the sweep programmer card. All 7 decades of BCD data are transferred serially on a decade by decade basis every 10µs. All timing signals needed by the synthesizer are produced by the timing generator circuit. The timing generator controls the timing of the transfer of frequency data input to the phase register and divide-by-N counter, and controls the timing of the fractional phase correction (residue) circuitry.

4-73. DOWN CONVERTER (figure FO-27). The 5035-2002 down converter circuit 2A1A2 generates additional synthesized signals derived from the 5 MHz frequency standard and the 40-70 MHz synthesizer output which are required for receiver (or

transmitter) use. The primary function is to translate the 42-70 MHz output of the synthesizer to a 2-30 MHz output for the transmitter sweep. The 5 MHz input from the frequency standard is buffered by the down converter circuit and frequency multiplied to 40 MHz by the harmonic generator and 40 MHz bandpass filter. The 40 MHz is then mixed with an amplified 40-70 MHz signal from the synthesizer. The output product of the mixer is the 2-30 MHz receiver sweep which is further amplified and filtered to produce a 0 dBm (one milliwatt) sine wave output. The down converter also featues a gating circuit which turns off the 2-30 MHz output when it is not needed. Gating is used for blanking of the TCS-4B transmit sweep at selected frequencies and to gate off the unused 2-30 MHz output for RCS-4B application.

4-74. SWEEP PROGRAMMER (figure FO-29). The 5035-2003 sweep programmer circuit 2A1A 3 controls the frequency sweep by digitally programming the synthesizer to advance its output frequency in 1 Hz steps every 10 microseconds. The sweep programmer contains an 8 decade BCD counter that stores the programmed frequency data of the synthesizer. This is preset with the sweep starting frequency (low limit) of 2 MHz. When the sweep START command (from the sounder control logic) is received, a 100 kHz clock from the synthesizer is gated on to the 8 decade counter. The counter increments by one count on every pulse of the 100 kHz clock . This advances the preset count by one Hz every 10 μs resulting in a linear increase in the programmed frequency corresponding to a 100 kHz per second sweep rate. The sweep continues until it reaches 30 MHz when the upper limit detect circuit interrupts the 100 kHz clock thereby stopping the sweep and resetting the 8 decade counter back to the 2 MHz low limit. If a 2-16 MHz sweep is" selected the sweep programmer operates as described above except the upper limit detector is set to 16 MHz and the sweep clock is divided by 2 to 50 kHz.

a. The sweep programmer also contains slip circuits and clock gating circuits which increase or decrease the basic 100 kHz (or 50 kHz) sweep clock by O. 1, 1.0, or 5.0%. The resulting slight change in sweep rate allows the RCS-4B receiver sweep to be advanced or retarded relative to the TCS-4B transmit sweep for synchronization purposes. This slip circuitry is not used in TCS-4B applications. The blanking control circuit drives RF gating circuits in the synthesizer down converter for TCS-4B transmitter RF blanking, but this circuit is not used in RCS-4B application.

b. The sweep programmer also contains two digital dividers; the 100 kHz reference generator, and the VCO divide-by-20 counter. The input to the 100 kHz reference generator is the 5 MHz standard, which is digitally divided by 50 to produce 50 nanosecond wide pulses at 100 kHz rate. These pulses drive the synthesizer phase detector reference input. The VCO divide-by-20 counter takes the 42-70 MHz synthesizer output and divides it to the 2. 1-3.5 MHz count output for use by the frequency counter logic that, in turn, drives the LED displays.

4-75. RECEIVER (2A2) (figures 4-12, FO-32, and FO-33). The 4028 receiver consists of two major circuit sections: the receiver front end section and the output section. The functional circuits of the receiver are diagramed in figure 4-12.

4-76. RECEIVER FRONT END. Antenna selection is accomplished by two relays, K 1 and K 2, which connects one of three antennas to the receiver (figure FO-32). Relay K 3 selects either an antenna or the internal calibrator. The calibrator

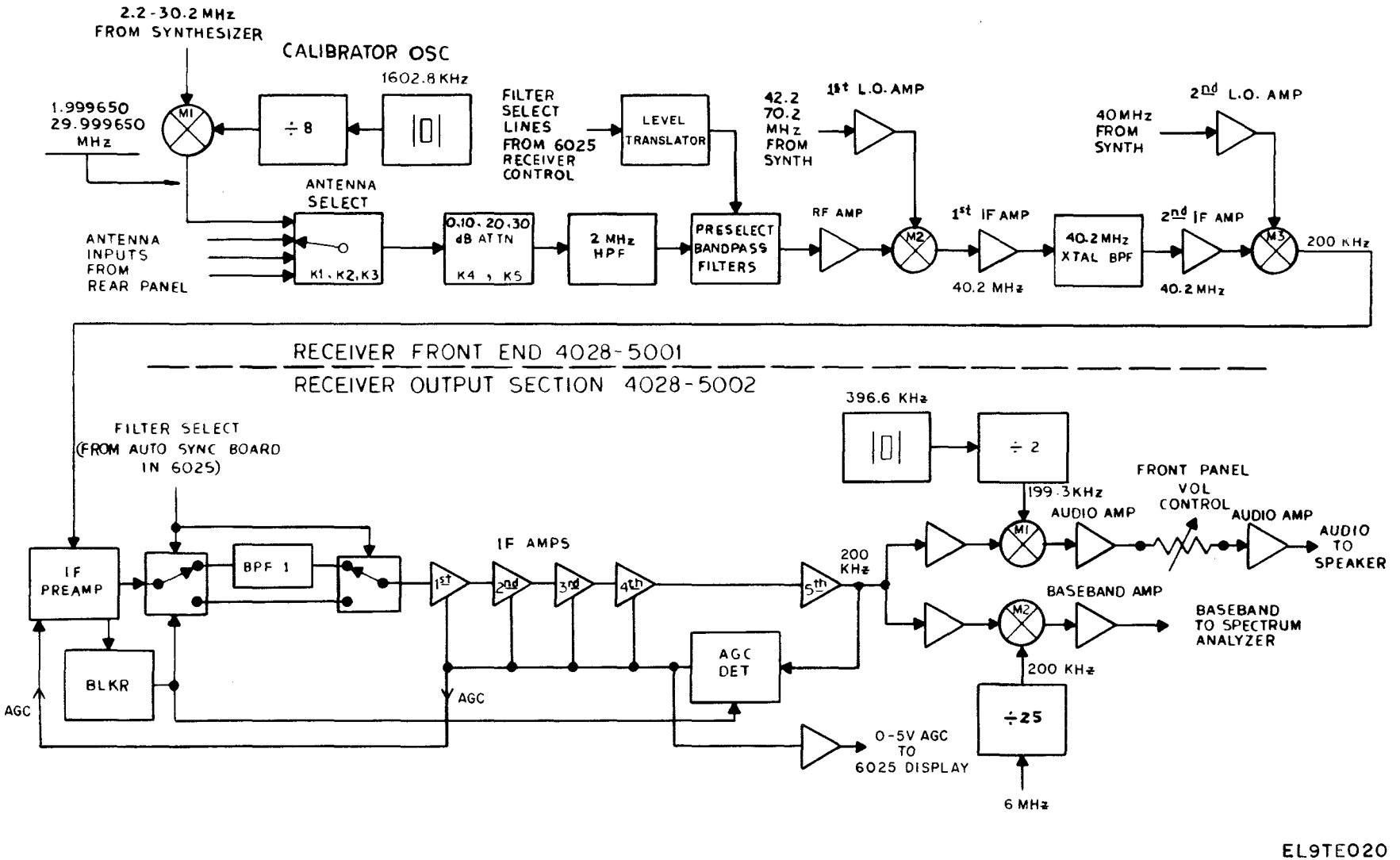


FIGURE 4-12. Receiver Block Diagram.

provides an in-band sweeping signal of approximately -107 dBm at the receiver tuned frequency over the range of 2 to 30 MHz. The 42.2 to 70.2 MHz LO frequency from the sweep synthesizer is mixed with 40 MHz in the synthesizer converter to produce a 2.2 to 30.2 MHz output which is 200 kHz above the receiver tuned frequency. This signal is fed to the receiver calibrator where it drives mixer M1. A 1602.8 kHz crystal oscillator Y1-U1 is frequency divided by 8 to produce a 200.350 kHz low level signal that is also fed to mixer M1. The output of Ml is a double sideband suppressed carrier sweeping signal with 200.350 kHz sidebands. The lower sideband is, therefore, 350 Hz below the receiver tuned frequency and falls in-band; resulting in a 350 Hz baseband output tone. Following mixer M1 a double π section attenuator sets the calibration tone level at -107 dBm before it is applied to relay K 3 of the antenna switch. From the calibrator relay K 3, the RF input is passed through two relay switchable attenuators K 4 and K 5, 10 dB and 20 dB respectively, to provide 30 dB of front end attenuation in 10 dB steps, as selected by the 6025 unit. When the calibrator is enabled, the attenuators are set to 0 dB.

4-77. Following the attenuator stage the signal passes through a 2 MHz high pass filter to remove all signals below the frequency range of interest. The preselector which follows provides bandpass filtering for the half-octave band of interest. In practice, the eight half-octave filter stages (figure FO-32/2) operate in a sequential manner as the sweep progresses, starting with filter #1 and ending with filter #8 (2-30 MHz). The filter select lines are driven from the preselector decode circuit on the 6025 receiver control board and are level translated by Q1 through Q8. The switched ±12V level translator output provides forward biasing (+12V) on the selected filter while maintaining reverse biasing (-12V) on the other filters. Only one filter at a time is enabled. Preselector decide is described in paragraph 4-31.

4-78. Following preelection, the signal is amplified by a 10 dB linear class A push-pull RF amplifier and enters the first mixer (M2). Mixer M2 combines the 2-30 MHz RF signal with the 42.2-70.2 MHz output of the sweep synthesizer to produce a first intermediate frequency of 40.2 MHz. The first mixer LO injection from the synthesizer is amplified from 0 dBm to +13 dB m and is then converted to a square wave drive by U4. The square wave LO signal is then further amplified by U6 to +27 dBm to drive the first mixer. This 1/2 watt square wave LO provides superior first mixer intermodulation distortion performance for the receiver. The 40.2 MHz IF mixer output is amplified in a 10 dB amplifier, identical to the one used at the mixer input. After this initial IF amplification (figure FO- 32/4), the signal is filtered by a 40.2 MHz crystal filter. This 10 kHz bandwidth filter provides selectivity to eliminate unwanted signals and noise in the early stages of the receiver before the signal enters the high gain stages. The filtered signal is then amplified by a third 10 dB RF amplifier before entering the second mixer (M3) (FO-32/5). The second mixer converts the 40.2 MHz signal to the 200 kHz second IF. The 40 MHz local oscillator injection signal for this stage is generated in the synthesizer. The 40 MHz output from the synthesizer is amplified and passed through a series of gates to develop complementary square wave LO inputs to the mixer.

4-79. RECEIVER OUTPUT SECTION. The receiver output section input is the low-level 200 kHz IF from the receiver second mixer. The output section generates two output signals: the baseband (0-500 Hz, or 0-5 kHz) signal (which goes to

the spectrum analyzer), and the audio, which is the same bandwidth as the base-band but offset by 700 Hz to make it easier for an operator to hear when presented to a loudspeaker. The 200 kHz IF signal is first terminated by R1 (figure FO-33/1) and then impedance transformed (upward) by T1. Resistor R2, R7 and Q1 form a variable attenuator which is controlled by the AGC circuit. Q1 acts as a variable resistance to ground - resistance increases as the gate voltage becomes more negative and decreases as the gate-to-source voltage goes to zero volts. Q2 and the drain-resonating components L1 and C10, form a tuned amplifier at 200 kHz, while Q3 is a source-follower circuit providing minimum impedance loading to the preceding tuned circuit and a controlled source impedance to the following crystal filters. The receiver has two bandwidths, 500 Hz , and 5000 Hz, controlled by the 6025 system logic. U1-U3 are electronic switches which place the appropriate filter into the IF circuit. The 500 Hz (BPF #1) crystal filter is mounted inside the receiver module, and the 5000 Hz bandpass is determined by the LC tuned circuits in the 200 kHz IF amplifiers. After such filtering, the 200 kHz IF is amplified by several similar amplifier/variable-attenuator circuits. Q5-7 (figure FO-33/2) form a typical circuit. Q5 is a voltage-variable resistance which, with R30, forms a voltage-variable attenuator to control the amplitude of the signal at the input of the tuned amplifier Q6. Q7 is a source-follower circuit that presents a high impedance load to the tuned drain circuit of Q6 and a low-impedance drive to R39, the first element of the next similar circuit. These amplifiers and attenuators comprise a tuned IF amplifier whose gain can be changed by the AGC circuit, such that the 200 kHz IF is maintained at approximately 50 mVrms at Q17. The 200 kHz is converted to baseband by M2 (figure FO-33/3) which mixes the IF with a locally generated 200 kHz LO. This LO is generated from the 5 MHz supplied by the sweep synthesizer to J8 of this board. U10-11 divide the 5 MHz by 25 to yield 200 kHz which drives U12 to modulate M2 through R105 and R106. The baseband output of M2 is amplified by U 14-15 to approximately 1 Vrms which becomes the baseband output of the sounder receiver.

4-80. The 200 kHz IF is also converted to Ml to audio with a 700 Hz offset. Y1 and U7 form a 398.6 kHz oscillator whose frequency is divided by 2 in U4 to 199.3 kHz. When mixed with the incoming 200 kHz IF, this signal yields the receiver bandwidth offset converted to 700 Hz. U5 is an audio amplifier and low-pass filter which drives the audio volume control mounted on the 4028 front panel. U 6 further amplifies the audio to power the loudspeaker, also on the front panel.

4-81. To control the gain of the IF amplifiers, the 200 kHz IF output is detected in an AGC circuit. The 200 kHz IF, approximately 50 mVrms, is buffered in unity-gain amplifier U16 and detected in a half-wave rectifier circuit of U17 (figure FO-33/4). This half- wave- rectified signal is further amplified by U 18 and smoothed by R134 and C101. The resulting voltage is amplified by U19 and presented through Q22 to an RC circuit, R151-152, C107 and CR5. This circuit determines the AGC time constant which is made to be asymmetrical; that is, CR5 allows C107 to be charged negative more rapidly than positive. (Note that voltage on C107 is negative.) This provides an AGC loop with a slow attack-fast decay time constant necessary for chirp sounding. Relay K1 can switch in another resistor in parallel with R152 to change the AGC time constant. A shorter time constant is needed during auto sync to maintain optimum receiver gain and minimize the change of missing the received chirp signal. The voltage on C107 is buffered by the unity-gain amplifier U21 and becomes the AGC control

voltage for the IF amplifier. The voltage also goes to an AGC output amplifier, U20, which is used to drive the AGC bargraph on the 6025 display.

4-82. The receiver is generally sweep-tuned through the HF band. Occasionally, the receiver sweeps through a strong signal which may cause the narrow-band filters to ring for a long period of time, thereby desensitizing the receiver immediately afterwards. To reduce this effect, a blanker circuit is used to detect the presence of an approaching large signal and to momentarily turn off the input to the IF amplifiers, Transistors Q24-32 (figure FO-33/5) form a separate IF amplifier with a bandwidth wider than that of the main IF amplifier, such that, as the receiver is sweeping, it will detect a large signal approaching the main IF bandwidth before it appears in the main IF passband. When such a signal is detected, a one-shot, U22, is triggered which, for approximately 10 milliseconds: (1) disconnects the IF input to the crystal filter in U1 and terminates the filter input by U2, and (2) holds the prior AGC level by opening Q22 in the AGC detector. The blanking sensitivity control is normally set to blank the IF amplifier if the approaching signal is 25 dB or greater above the currently received signal or noise.

4-83. RECEIVER POWER SUPPLY (figure FO-34). The receiver power supply provides all the DC voltages used in both the 6025 and 4028 units. Regulated voltages supplied to the 4028 unit are +-5V, +12V, and -24 VDC. The remaining unregulated supplies are routed to the 6025 unit and are regulated there. (See paragraph 4-63.) In the 4028 unit, the +12V, -12V, and +24 VDC outputs supply both the synthesizer and receiver modules while the +5V outputs supply only the synthesizer. The duplication of some DC supplies is provided to assure separation of noise signals between unrelated inputs. An internally mounted toggle switch (S2) is provided for selecting 115 or 230 VAC inputs. In addition, some compensation for small increments of input voltage variations may be made by altering terminal board (TB1) connection adjacent to the transformer. (Refer to paragraph 5-14 for adjustment of these connections.)

4-84. 6043 POWER DIVIDER UNIT 3

4-85. The receiver uses three separate fourway power dividers to interface with receiving antennas. AU connections should be of 50 ohms impedance. The power divider results in an output on each port approximately 6 dB below the input. Each divider provides minimum isolation of 30 dB over the entire 2-30 range.

4-86. FREQUENCY STANDARD SECTION (S/N 400100 and before)

4-87. FREQUENCY STANDARD (1A6) (figures FO-35 and FO-36) (S/N 400100 and before). The receiver timing circuits are based on a 5 MHz standard derived from a 10 MHz temperature-controlled quartz crystal oscillator. Both the oscillator-amplifier and the oven controller portions of the oscillator require a stable 10 VDC input. This is provided by regulator U3 from the battery or Q02 regulated primary power source. An LC circuit comprising L1 and C10 further isolates the oscillator portion from switching transients. On the return side of the oven circuit, Q101 provides current limiting to safeguard against current surges during the initial oven heater warm-up period (approximately 5 minutes), The 10 MHz output of the oscillator is divided by flip-flop U2 down to 5 MHz (internal standard) and fanned out to buffer gates U1 for use by the timing circuits as independent 5 MHz, 50 ohm sources.

4-88. The switching regulator circuit 1A6A3 (figure FO-36) regulates the +5-volt power input to the primary timing circuits of the receiver. The circuit is basically intended for regulation of the battery supply during a power failure. However, in normal operation, a line power derived source of 29 VDC (from CR4+) is routed through the same circuit allowing unbroken interruption of power should a supply failure occur. The high efficiency (65%) circuit contained on this board uses a low current drain voltage regulator connected as an oscillator (U1) in which an inductor (L2) is used in the feedback loop as an energy storage device. By controlling oscillation, the inductor effects" internal conduction of the regulator/ oscillator, thereby cent rolling volt age. A 1.6A current limiter (Q4, Q5, and Q6) and a 6 volt, 5 watt, overvoltage protector, (CR6 and CR10) are included as an integral part of the circuit. A related circuit senses the input line to determine if the battery voltage is less than 16.3 volts. This is achieved at U2 by comparing the received voltage to two zener diodes, the difference voltage thereby controlling Q7, which in turn controls turn-on of oscillator U1.

4-89. 3-PATH CONTROLLER 1A4 (S/N 400100 and before)

4-90. 3-PATH PROGRAMMER 1A4A1 (figure FO-37). The 3-path programmer circuit performs three basic functions: it provides precision five minute timing, using a count down of the 5 MHz frequency standard; it generates advance and retard pulses to slip each path in time to synchronize it with the related transmitter; and it provides a LED display decode for either path 1 or any other switch-selected path time.

4-91. The incoming 5 MHz is initially divided down to 100 kHz by U17 and U10 (figure FO-37/1) and routed to the three separate path timer inputs (MCK). Each path timer then divides the 100 kHz down, first to one pulse per second for external sampling, and then into seconds and minutes for the LED display logic switch. The LED display logic switch is a 16-pole, 3-throw logic circuit switched electronically by three SET positions of the MODE select switch. When the MODE select switch is not in a SET position, path 1 is automatically selected since only one path time can be displayed. The selected path is routed directly to the LED display driver circuit for display of the time segments. In addition to the basic five-minute count, each path timer sends a sequential five-minute pulse to each of the PATH PROGRAMMER switches (0-MINUTE position, 5-MINUTE position, 10-MINUTE position, etc.), The pulse is negative-going for one millisecond. If the switch for that path is active at any of these times, it is routed to the auto start circuit for activation of the CRT memory and synthesizer start functions.

4-92. The slip generator (figure FO-37/1) uses a timing and gating technique to add or delete pulses from the 100 kHz input frequency of any path. A pulse train, whose frequency is selected by the front panel SLIP RATE MS /SEC switch, is gated to the two one-shots, U18. The positive (MSP), or advance, output produces narrow pulses which are added into the 100 kHz stream to slip the path position forward in time. The negative (MSN), or retard, output develops a negative- going pulse of identical duration and position (i.e. in sync) as the 100 kHz stream which, when gated into the select paths input, effectively cancels existing synchronous pulses, thereby retarding the clock time.

4-93. RECEIVER CONTROL 1A4A2 (figure FO-38). The receiver control assembly can be divided into five functional circuits: front panel select, preselector decode, frequency counter, cursor-to-frequency converter, and auto start.

4-94. FRONT PANEL SELECT (figure FO-38/1). This circuit interfaces all subpanel switches with related parts of the receiver control circuits. All pushbutton switches are debounced and rotary switch positions routed to relevant circuitry at the proper time.

4-95. PRESELECTOR DECODE (figure FO-38/2). Binary-coded-decimal (BCD) frequency data is routed from the local oscillator (LO) frequency counter (paragraph 4-96) to the preselector decode circuit, for translation to frequency range data for the receiver preselect filters. The frequency information is decoded to provide a 1 of 8 selection (negative true output) to drive the preselector switches as follows :

OUTPUT (LOW)	FREQUENCY RANGE
PRE 1	2.0- 3.0 MHz
PRE 2	3.0- 4.4
PRE 3	4.4- 6.0
PRE 4	6.0- 8.4
PRE 5	8.4- 12.0
PRE 6	12.0 - 17.0
PRE 7	17.0- 24.0
PRE 8	24.0- 30.0

4-96. FREQUENCY COUNTER (figure FO-38/3). This circuit counts the 2-3.5 MHz frequency from the synthesizer and provides BCD frequency information to the LED display and preselector decode. The 2-3.5 MHz input is gated into U13 for two milliseconds. Counters U9-U13 are preset with the number 5980. During the two millisecond gate interval, U9-U13 count up from 5980. At the end of the two-millisecond period, the number contained in the counters is the actual received frequency (disregarding the carry digit) . For example, at 2 MHz, the receiver synthesizer frequency is 42.2 MHz. The frequency counter counts every 20th cycle, or 2,110 counts/millisecond. Thus, 4,220 counts are gated for two milliseconds:

```
Gate for 2 milliseconds = 4220
add counter preset      = 5980
                          10200
Disregard carry
For                       02.00 MHz (receiver frequency)
```

The BCD frequency information is routed through U17-U20 which form a 16-pole, double-throw switch. This switch is in turn activated by the front panel Cursor/ RCVR pushbutton, which in the normal (RCVR) position switches the BCD information into the LED display.

4-97. CURSOR TO FREQUENCY CONVERTER (figure FO-38/3). The cursor storage and readout assemblv (1A2A1) sends information (signal CUL) to the cursor to frequency converter logic indicating the frequency on which the movable cursor

is set. Pushing the CURSOR FREQ pushbutton switch (CFS) routes the BCD cursor information (CCK) to the LED display.

4-98. The logic for the cursor to frequency conversion is represented in the block diagram of figure 4-4 and this function is performed bv the circuits on the cursor storage and readout (1A2A1) and receiver control (1A4A2). Every ten milliseconds the start/stop flip-flops U9 gate the 400 - 700 kHz clock (the exact rate is arbitrary) into the up-and down-counters, a borrow (end-of-count) pulse is issued which stops the clock. Since the count rate for the BCD up-counter was the same as for the binary down-counter, the total count added to the pre-load of 0199 provides the BCD equivalent of cursor frequency in megahertz. At the end of ten milliseconds, the two counters are cleared, the load enable activated, and the count process repeated. Assuming the moving cursor to be stationary, the frequency of the moving cursor appears at the outputs of BCD up-counters U25-28 every ten milliseconds and remains latched at U1-U4 (figure FO-38/3) for the same period. Hence, actuation of the CURSOR FREQ switch throws the 16-pole switch (U17-20) between the BCD counters and the LED display via the latches, making a current cursor readout available at a refresh rate of two milli-seconds.

4-99. AUTO START (figure FO-38/4). The purpose of the auto start circuit is to receive start time information for the PATH PROGRAMMER switches, start the synthesizer, and start loading the appropriate CRT memory. Each pair of flip-flops (U45, U53, or U61) are for a single path. The two inputs necessary to trigger the CRT memory load function (TVL1) are: 1) a pulse through the (PS1) path programmer #1 bus (signifying any #1 PATH PROGRAMMER switch selected) and 2) a pulse through 1 CLK input (signifying that a new 5-minute interval is starting) from the path programmer circuit (paragraph 4-91). The two hex inverters (U52) provide a slight time delay so the second half of the flip-flop re-sets (gets armed) before active toggling on the new pulse. Each of the path flip-flops operate in the same way; however, a gating circuit (U44) prevents active switching of the other two paths once a legitimate output is detected. The active TVL line is routed to the memory load logic for display and memory load. Simul-taneously, the synthesizer is enabled (AST - for any path) for sweep start. After the sweep is completed, a return pulse from the synthesizer (EOS) clears the output flip-flops ready for the new selection.

SECTION 5

MAINTENANCE

5-1. INTRODUCTION

5-2. This section provides maintenance and service information for the RCS-4B receiver. Included are tables of recommended test equipment, a preventive maintenance schedule, corrective maintenance procedures, and performance verification data. An understanding of the theory of operation from Section 4 is required for troubleshooting and repairing the receiver.

5-3. TEST EQUIPMENT

5-4. Recommended test equipment for performance checking and troubleshooting is listed in table 5-1. Other test instruments may be used if their performance is equivalent to those listed. If a test measurement is made which is outside the acceptable range, operation of the test equipment should first be verified before assuming malfunction of the equipment under test.

5-5. PREVENTIVE MAINTENANCE

5-6. Table 5-2 provides a list of recommended preventive maintenance procedures. To assist in obtaining long-term trouble-free operation of the receiver, the maintenance schedule as recommended should be adhered to as closely as possible. Marginal operation of any unit checked should be noted and carefully re-examined at the next maintenance period.

WARNING

In the performance of some maintenance procedures, it is necessary to have the equipment energized and dust covers removed. Extreme care must be exercised in making internal measurements or adjustments since potentially lethal voltages are present.

5-7. CORRECTIVE MAINTENANCE

5-8. The corrective maintenance data provided in this section consists of troubleshooting procedures and adjustment procedures. Parts requiring removal during relevant adjustment operations are described and illustrated as necessary. The recommended maintenance approach for the RCS-4B receiver is repair by replacement of assemblies. Faulty assemblies are returned to the depot for repair to a part level.

5-9. TROUBLESHOOTING PROCEDURES. Table 5-3 provides a basic guide to troubleshooting the receiver. The table is not intended to be all inclusive, but rather to provide indications of what unit or assembly is defective. One approach to fault isolation is to derive all possible information from the function or malfunction of operating controls and indicators and then, through systematic analysis of test and measurement data, along with the troubleshooting guides, localize a fault to a module or assembly. The malfunction is verified and corrected

Table 5-1. Test Equipment Required

Item	Recommended manufacturer and type
Oscilloscope	Tektronix 455 (or 465)
Frequency Counter	Hewlett Packard 5300B
Multimeter	Simpson 460 (or Beckman 3020)
Termination, 2 watts	Microlab FXR TA-5MN
Attenuator, 20 dB	Tektronix 011-0059-02
Spectrum Analyzer	Hewlett Packard 141T
with IF Section	Hewlett Packard 8552B
RF Section	Hewlett Packard 8553B
Sweep Generator	TCS-4B/1024 Unit (BR Communications)
Audio Oscillator	Hewlett Packard 651A
Mixer	Watkins Johnson MIC
Attenuator (Variable)	Kay Model 432D
Power Supply (35 VDC Lab Type)	Lambda LL-903-OV, or LP-552-FM or HP 6200B

by replacing the faulty assembly with a known good assembly. The performance test of paragraph 5-29, figures 5-2, 5-3, 5-4, 5-6, 5-7 and 5-8, and schematics of Section 7 provide the measurement data that can be used for fault isolation.

5-10. OVERVOLTAGE PROTECTION. The 4028 power supply incorporates an overvoltage protection device, U9 (figure FO-34/1. The overvoltage device accomplishes circuit protection by effectively short circuiting the output terminals of the power transformer when the trip voltage limit is exceeded. The overvoltage device is connected across the 11 volt terminals and trips at 17 volts. When the trip voltage is exceeded, the input power fuse is normally blown. This condition should be noted when troubleshooting and line voltage checked before trying to turn on the receiver.

5-11. ADJUSTMENT PROCEDURES

5-12. GENERAL. All initial adjustments to the receiver were made at the factory before shipment. The following procedures are provided for use following a repair or as required during the performance verification test.

Table 5-2. Preventive Maintenance Schedule

Procedure	Schedule
1. Perform self-test to check receiver operation and condition of standby battery. For receiver operation, the main power and standby battery must be on and the receiver must be sweeping. See paragraph 5-15 for standby battery test.	Daily (at beginning of each shift).
2. Check receiver synchronization by actuating DISPLAY CYCLE switch. To adjust the display synchronization, sequence MODE switch to the three SET positions and, in each position, adjust display using the ADV/RET switch. Also check for evidence of sounder record display dropout. A recurring indistinct or broken path display could indicate a faulty antenna connection, defective power divider, or defective receiver preselector filter.	Daily (at beginning of each shift). NOTE Adjust only while selected path sweep is in progress.
3. Check operation of 6025 and 4028 exhaust fan efficiency. Fan suction should be sufficient to hold paper placed over intake filter (rear panel of 6025 and front panel of 4028). If necessary, remove and clean filter by submerging in warm water. Thoroughly blow dry with compressed air.	Weekly (daily if in dusty area).
4. Check frequency standard, and adjust if necessary per paragraph 5-21.	Monthly (or if excessive drift is observed on all paths simultaneously.
5. Make visual inspection of all interconnecting cables and connectors at rear of units. Ensure that plugs are fully inserted and that no undue strain is being placed on cables.	Monthly
6. Remove top covers from receiver units and make visual inspection of interiors. Ensure that modules are properly seated and that no loose wires or signs of overheating exist.	Quarterly
7. Check all low voltage DC power supplies per instructions of paragraph 5-13.	Semi-Annually

Table 5-3. Troubleshooting Guide

Indication	Location/cause
1. System main power pushbutton (on 4028 unit) does not illuminate.	Main line input disconnected; Fuse F 1 blown Transformer T1, diode bridge CR1, lamp malfunction, or overvoltage crow-bar U9.
2. No CRT raster	Cabling to 6025 disconnected; CRT drive or tube malfunction (check fuse F101 on assembly 1A7). 4028 power supply or 6025 voltage regulator malfunction.
3. CRT raster, but no video display.	Transmitter out of sync; current PATH PROGRAMMER switch off; antenna cable disconnected; antenna relay malfunction; Perform self-test (see fault indications, step 9).
4. AGC display, but no Chirp-sounder record display.	Receiver baseband section faulty; spectrum analyzer or receiver control circuit mal-function. Check presence or absence of audible tone and of cursor lines in lower part of display.
5. Chirpsounder record display, but no AGC.	Input attenuator set too high; fault in receiver. AGC detector or output amplifier.
6. Audio tone absent, or incorrect frequency or volume.	Fault with receiver oscillator Y1 or assoc-iated divider, etc. (receiver output section assembly 2A2). Use test push-button to check effect of calibrator oscillator; also check speaker, audio amplifier and gain control.
7. Excessive drift of Chirp sounder record display on CRT.	When use of the slip rate switch to correct vertical path display drift is insufficient or too frequently required for all received paths the cause is prob-ably frequency standard precession in receiver. Refer to paragraph 5-21 for adjustment.
8. Numeric display stopped or incorrect.	For Frequency; Fault in frequency counter 1A4A2, sweep synthesizer 2A1, display elements 1A9, or +5V supply. Check per-forming LAMP TEST (for display ele-ments) and receiver TEST (for power supply).

Table 5-3. Troubleshooting Guide - Continued

Indication	Location /cause
	For Time: Fault in 3-path programmer 1A4A1, frequency standard 1A6, or display elements 1A9.
9. In receiver self-test, RCVR red lamp lights.	Indicates fault in any of 6025 regulated DC supplies, or 4028 unregulated supplies. Alternatively, the lamp will also indicate a fault occurring in any functional part of the control circuits processing the received signal. A malfunction can be isolated to either the power supplies or the receiver functional circuits, as follows: a. Stop the synthesizer sweep by setting MODE switch to MAN position, pressing STOP switch, and then pressing RESET switch. b. Repeat the receiver test. If the red RCVR lamp lights, the fault is in the power supplies; if the green RCVR lamp lights, the fault is in a receiver functional circuit.
10. In receiver self-test, BATT red lamp lights.	Check that BATT switch is ON. Replace batteries (if non-rechargeable supply). Check and recharge (if rechargeable supply).
11. Less than six cursors available for storage/display.	Cursors stored in off screen frequency. Perform cursors erase (paragraph 3-8, step e). If fault remains, turn off system power, wait several seconds, turn on system power.

WARNING

Use extreme care when making internal adjustments with power on. Potentially lethal voltages are present in the receiver.

5-13. POWER SUPPLY ADJUSTMENT. The 4028 unit supplies regulated DC voltages of +5, +12, -12, and +24 VDC for its own receiver circuitry, and unregulated +5, +11, +20, -20 and +35 VDC for use by the 6025 unit. None of the DC voltages require adjustment; however, they should be periodically checked to detect diminished operation. Voltages are checked using a multimeter and measuring the value as marked in figures 5-2 through 5-9 for each of the module test

points. To measure DC voltages in the 4028, it is necessary to remove the unit cover and the four screws which secure the 2A1 and the 2A2 assemblies to the chassis plate. The two assemblies are then lifted to allow access to the assembly test points. To measure DC voltages in the 6025, it is necessary to remove the unit cover. The assembly test points are readily accessible without further disassembly. Note that the AC ripple for all regulated supplies measures less than 10 mV peak-to-peak.

5-14. Voltage variations from the normal 115 or 230 VAC input can be accommodated by changing connections on the terminal board 2A3TB 1 located on the 4028 chassis plate. The unit cover must be removed to allow access to the terminal board. Upper limits of 120 (or 250) VAC can be tolerated using the same factory wiring as for 115 (or 230) VAC. If the line voltage approaches 105 (or 220) VAC, turn power off, and transfer the connection on 2A3TB 1 pin 1 to 2A3TB 1 pin 2 (figure FO-26/1).

5-15. STANDBY BATTERY SUPPLY TEST. Two different types of standby battery assemblies are used in the RCS- 4B. Some receivers have a non-rechargeable battery assembly (part number 6025-1008) that uses standard D-cell batteries. Other receivers have a rechargeable battery assembly (part number 6025-1018) that includes an integral charging circuit and uses sealed lead acid cells. Conditions for testing the charge of the battery supply differ between the non-rechargeable and rechargeable assemblies. These different conditions are noted in steps a and b below. The test results as defined in step c apply to the test of non-rechargeable and rechargeable assemblies.

For the non-rechargeable battery assembly (P/N 6025-1008), a test may be conducted at any time during operation with AC line power on or off and the BATT switch on. Pressing the TEST pushbutton switch on the 6025 front panel initiates the test and the BATT lamps light to indicate the charge condition of the battery supply as described in step c below.

b. For the rechargeable battery assembly (P/N 6025-1018), an accurate test of battery charge condition requires that the AC line power is turned off. If the TEST switch is pressed with AC power on, the green BATT lamp should always light since the charging circuit, which is on when AC power is on, provides a 28 volt potential across the battery supply terminals. A red or red/green lamp indication may result if battery supply is very weak, fully discharged, or defective. A battery protection circuit in the rechargeable battery assembly automatically disconnects the supply if the battery voltage is below approximately 17 volts in which case neither BATT lamp would light during test and loss of synchronization occurs if AC power is off. For an accurate test of battery condition, press the TEST switch with AC power off and the BATT switch on and note the BATT lamp indications of step c.

c. The BATT lamp indications are as follows:

(1) Green BATT test lamp only lights: Battery measures greater than 22 volts. Conditions are acceptable for operation on battery power.

(2) Green and red BATT test lamps both light:	Battery is between 18 and 22 volts. Conditions are marginal for operation. Battery pack must be charged soon (if rechargeable type).
(3) Red BATT test lamp only lights:	Battery is less than 18 volts. Battery pack must be replaced or recharged; or BATT switch is off.

5-16. BATTERY CHARGER ADJUSTMENT (For Battery Assembly P/N 6025-1018). The battery charger circuit, located inside the rechargeable battery box, automatically recharges depleted batteries and provides a floating trickle charge to maintain the batteries in a fully charged state during normal AC line power operation of the RCS receiver. Battery capacity and lifetime are dependent on the charging circuit output voltage. A charging voltage that is too high can damage the batteries, and too low a voltage does not maintain adequate charge in the battery cells. The battery charger circuit is set at the factory for a trickle charge voltage of +28.2 VDC which results in a 5 mA trickle charge current when connected to a fully charged battery pack. (This voltage will vary depending on the state of charge of the batteries). The battery charger circuit should not normally require readjustment. If adjustment is required due to replacement or aging of components, adjust as follows:

a. Remove battery pack (6025-1018) from the 6025 unit.

b. Remove top cover of battery pack.

c. Carefully connect a +35 VDC (±2V) external laboratory-type power supply to the battery charger circuit card inside the battery box. The positive (+) output lead of the power supply must connect to terminal E1 of the circuit card and the negative (-) output lead must connect to terminal E2 (ground).

d. Connect the positive lead of a digital voltmeter to TP1 and the negative lead to E 2 of the charger circuit card.

e. Turn on the +35 VDC supply and adjust potentiometer R3 on the card for a voltage of +28.9 VDC at TP1.

f. Move the voltmeter to terminal E4. Meter should read +28.2 VDC (±0.1 VDC) if the batteries are charging properly.

g. If the voltage at E4 is greater than +28.3 volts, check fuse F2 and switch S1 for continuity or replace battery pack.

h. If voltage at E4 is less than +28.1 volts, allow battery pack to charge for 24 hours, then repeat steps e and f. If E4 voltage is still low, replace battery pack.

i. Turn off +35 VDC supply, disconnect supply and DVM, and momentarily depress pushbutton switch S1 on the circuit card.

j. Replace battery box cover and reinsert battery drawer in 6025 front panel.

5-17. RECEIVER BASEBAND GAIN ADJUSTMENT. To measure the receiver baseband gain the 4028 cover must be removed. Then the four screws which secure the 2A1 and 2A2 assemblies to the chassis plate must be removed. Using the setup shown in figure 5-1 with the TCS-4B and RCS- 4B synchronized, apply a -70 dBm signal into the 6043 from the 1024. To determine the baseband gain, attach an oscilloscope to TP2 on the 2A2A2 assembly (refer to figure 5-6), and check for a nominal output of 2.8 ±0.4 volts peak-to-peak during normal operation. If the nominal output is outside this range, remove the cover for the 2A2A 2 assembly, and adjust R110 clockwise to increase gain or counter-clockwise to decrease gain.

5-18. AGC DISPLAY ADJUSTMENT . The offset adjustment (R161) and the gain adjustment (R168) are located in the AGC output amplifier of the receiver output section (2A2A2) (figure FO-33/4). They provide position and gain control, respectively, over the AGC analog output before being converted to a digitized bargraph by the timing and control circuit (1A2A2) for display by the CRT. Adjustment must be performed while the RCS-4B is synchronized (using the 1024 Unit of TCS - 4B as test equipment). Assemble the test setup per figure 5-1. Synchronize the 1024 and 6025 and proceed with the test.

a. Set the input signal to -120dBm into ANT 1 of the 4028 (bypass the 6043 power divider). Measure signal out of Variable Attenuator' with Spectrum Analyzer. Adjust attenuator as required.

b. Adjust offset control R161 on 2A2A2 (4028-2002) circuit card to display a continuous line at the bottom cell of CRT AGC bargraph.

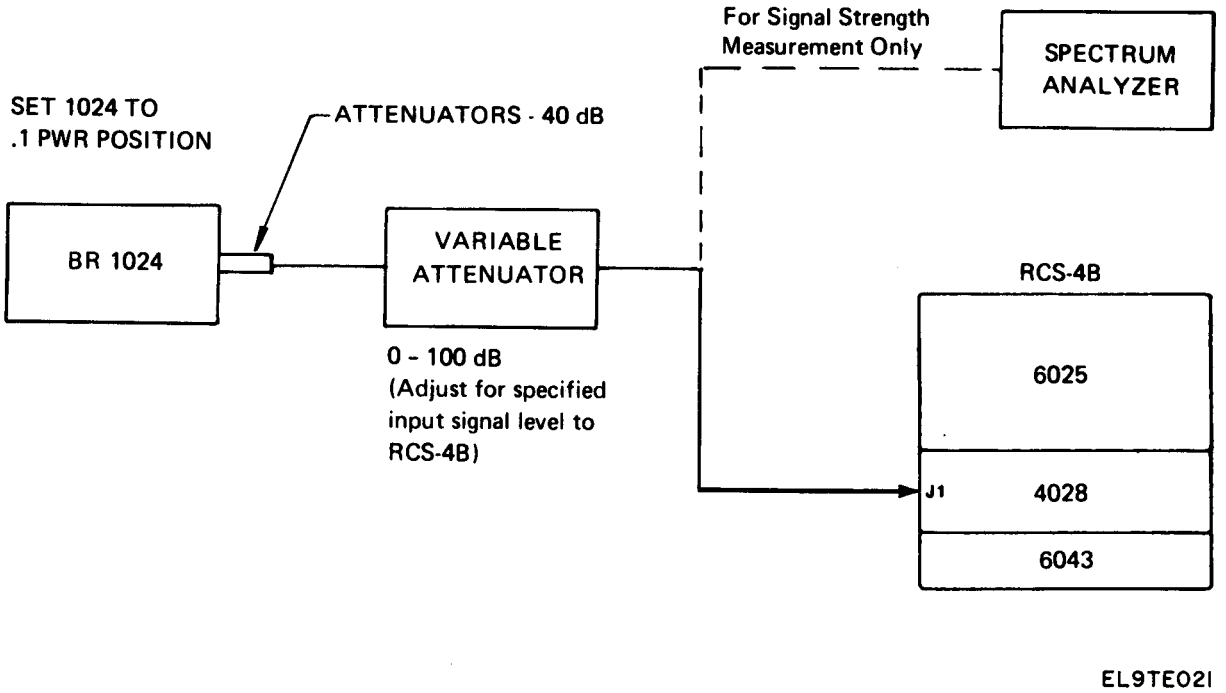


FIGURE 5-1. AGC Display Gain Adjustment Setup.

Increase the input signal 55 dB and adjust gain control R 168 until the bar-graph reaches the top of the display. Decrease the gain by one cell.

d. Repeat steps a through c until no further adjustment is needed.

e. Allow the RCS- 4B to run one full sweep with -120 dBm input. The AGC bar-graph should display in the bottom cell ±1 cell.

5-19. SYSTEM SENSITIVITY ADJUSTMENT. The Chirpsounder record display should be present on the CRT with signal levels as low as -137 dBm into the 4028 receiver or -130 dBm into the 6043 power divider. The display should not be present for signals weaker than -147 dBm into the 4028 or -140 dBm into the 6043. This can be adjusted with the slicing level adjustment, accessible through the top of the display logic (1A2) module. Use the test setup as shown in figure 5-1 (signal into the 4028). Decrease the signal level to -137 dBm. A solid line should be present for a minimum of 80% of the full sweep (2-30 MHz). To increase sensitivity, adjust the slicing level control counterclockwise and, conversely, to decrease sensitivity and reduce background noise, adjust the slicing level clockwise.

5-20. SPECTRUM ANALYZER BANDWIDTH ADJUSTMENTS. The 500 Hz bandwidth is controlled by ramp length R56, gain R37, and DC R49 adjustments on the 1A1A2 assembly (figure FO-10/5). The bandwidth adjustments are made as follows :

a. Assemble equipment as shown in figure 5-1. Synchronize RCS- 4B with TCS-4B using the 2-30 MHz sweep with a -80 dBm sweep input to the receiver (connect to J1 on 4028).

b. Connect a frequency counter to 4028 rear panel BNC connector J9 Baseband Out. Fine adjust RCS- 4B synchronization using Manual Sync (at 1 ms/sec) until counter reads 257 ±2 Hz. Make no further sync adjustments for the remainder of this test.

c. Then connect equipment as shown in figure 5-2.

d. Set the audio oscillator for approximately 0 dBm (50 Q) , and 200 Hz. Observe two horizontal traces on CRT near top and bottom of Chirp sounder record display area.

e. Slowly increase audio frequency until one trace disappears and note the audio frequency as measured on the counter. Continue to increase audio frequency until the remaining trace disappears and note audio frequency. Both frequency readings should be in the range of 250 ±7 Hz.

f. If adjustments are necessary, remove the module 1A1 cover to access the spectrum analyzer output board 1A1A2 (2006-2002).

Connect an oscilloscope to E35 (SYNC A). Adjust R56 until the positive going (+4V) pulse at E35 is 59 ±1 msec long. This pulse goes high for 59 msec once every second while the sounder is sweeping.

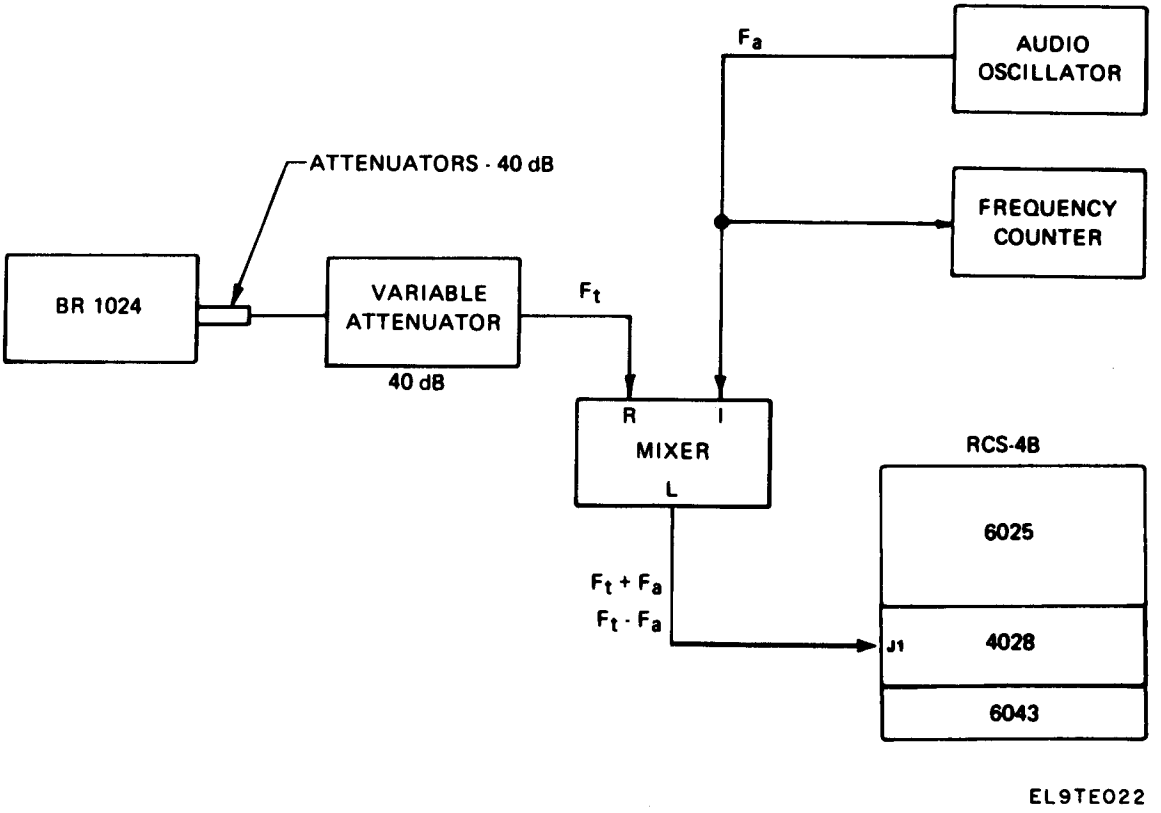


FIGURE 5-2. Bandwidth Adjustment Test Setup.

h. Adjust R49 DC and R37 GAIN controls until step e above is satisfied. R49 will move both traces up and down together on the CRT; R37 will spread or compress the spacing between the traces for a given audio frequency. Note that these adjustments interact slightly so care must be taken and adjustments repeated until proper alignment is achieved.

NOTE

If adjustment procedure time takes longer than one sweep of the RCS-4B (280 seconds), allow second sweep to start under PROGRAM mode and then repeat steps a and b above to verify sounder sync.

5-21. FREQUENCY STANDARD ADJUSTMENT. Over long periods of time, the temperature controlled quartz crystal in the frequency standard will show effects of precession (frequency change due to crystal aging) . When the rate of precession in the receiver and transmitters is not equal, the Chirpsounder record displays may drift up or down on the receiver CRT display. Normally, a record can be recentered on the CRT by means of the receiver SLIP control. If adjustment of the SLIP control is required more than once in eight hours, there is need to adjust the frequency standard. If all transmitter displays drift on the CRT in the same direction, it is necessary to adjust the receiver frequency standard. However, if at least one transmitter does not drift, or drifts in an opposite direction, then adjustment of the TCS-4B transmitter frequency standard is required. The operator of the drifting transmitter should be notified and informed as to the rate and direction of drift as observed on the receiver CRT. (For example, Chirpsounder record drifts up 20% of CRT height per 24 hours.)

5-22. To make the receiver adjustment, the direction and rate of drift on the CRT are determined. Then, if' the display is drifting downward, the front panel fine control (STD ADJ) is turned clockwise; if the display is drifting upward, the STD ADJ control is turned counter-clockwise. One full turn of the front panel STD ADJ control will compensate for a drift of approximately 10% of CRT height per 24 hours for 2-30 MHz sweep, or 0.5 milliseconds per 24 hours. (One full turn will compensate for a drift of 5% of CRT height per 24 hours for 2-16 MHz sweep,) If the STD ADJ control adjustment range is insufficient (at physical limits which are 20 turns end to end) to make the correction, it should be recentered, and the adjustment made on the course control located on the 6025, assembly 1A6 (figure 5-3). The control is adjusted in an opposite direction to that of the front panel STD ADJ control. For coarse control adjustment, turn counter-clockwise if display is drifting down; turn clockwise if display is drifting up. One turn of the coarse adjustment control will compensate for a drift of 100% of CRT height per 24 hours (5 milliseconds per 24 hours) for a 2-30 MHz sweep, or 50% of CRT height for 2-16 MHz sweep.

5-23. CRT DISPLAY ADJUSTMENTS . Controls for the CRT drive and synchronization signals are adjusted following replacement of circuit elements or when dis - continuities are observed in the position or linearity of the display. The brightness control for the CRT is on the front panel and is an operator adjustment. (Refer to Section 3, and check brightness adjustment). The schematic diagram of figure FO-18 should be referenced for location of adjustments. To perform the adjustments described in paragraphs 5-24 thru 5-27, the following disassembly actions must be performed:

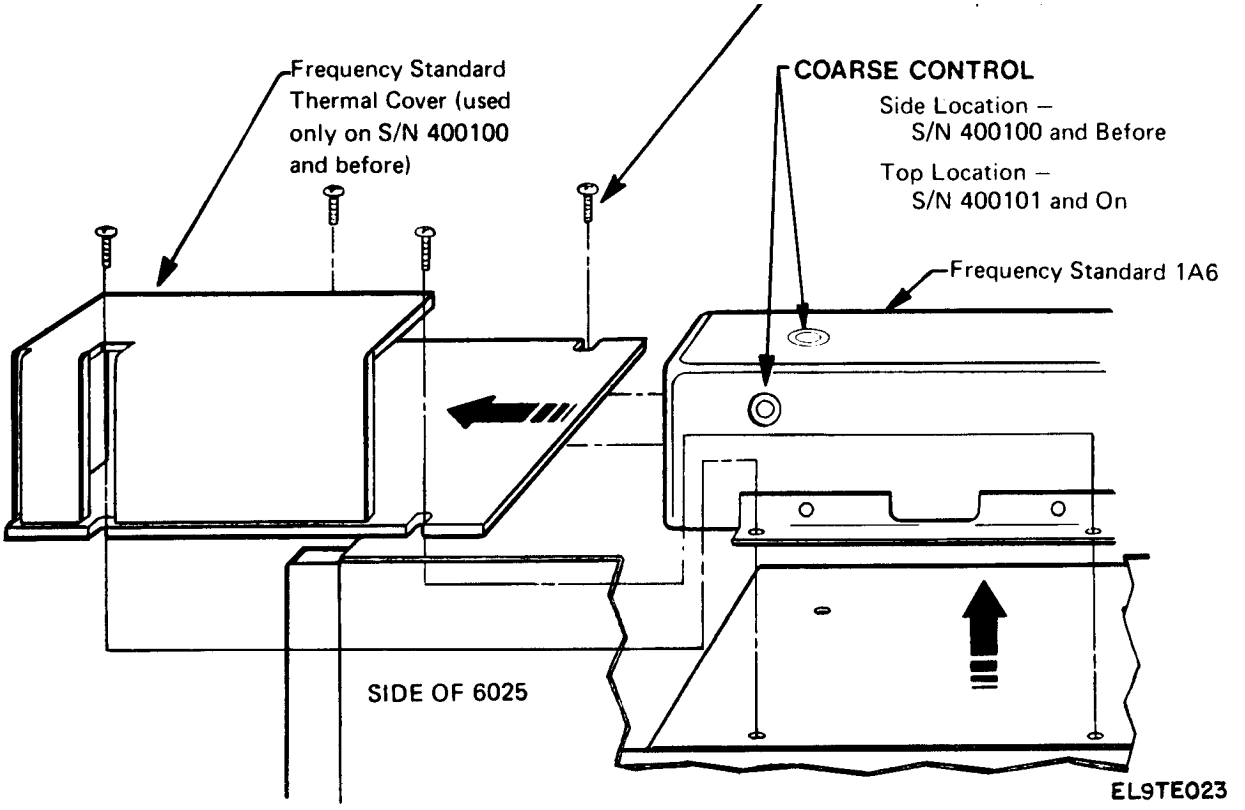


FIGURE 5-3. Crystal Oscillator Frequency Adjust.

a. Remove the 6025 cover, module retaining bar, and the four screws securing the 1A6 assembly to the mounting bracket.

b. Remove the plug to the 1A7 CRT display assembly, and then raise and set aside the 1A 6 assembly.

c. Remove the four screws securing the 1A7 assembly to the mounting bracket.

d. Remove the 1A7 assembly and reconnect the plug to 1A7J1.

e. All of the adjustment points discussed in paragraphs 5-24 through 5-27 are now accessible through holes in the CRT side cover.

NOTE

The CRT beam scans vertically. The yoke has been rotated 90-degrees counterclockwise from the normal (NTSC) television positions. Horizontal and vertical refer to the actual beam motion in this unit.

5-24. HORIZONTAL ADJUSTMENTS. There is some interaction between the horizontal frequency, width, and linearity controls. The adjustment procedure should be performed in the sequence indicated (see figure FO-18):

a. Apply video and synchronization signals to the CRT monitor.

b. Set the horizontal frequency control, R116, in the middle of the stable region of the adjustment.

c. Adjust the horizontal width control, R124, for desired width.

d. Adjust the horizontal linearity control, R121, for best horizontal linearity.

e. Readjust the horizontal frequency control, R116, for stable picture.

f. Recheck width and linearity.

5-25. VERTICAL ADJUSTMENTS. Raster height is affected by a combination of the low volt age supply, height coil L101 and the linearity sleeve located on the neck of the CRT beneath the yoke. Adjust for vertical linearity as follows:

a. Apply video and synchronization signals to the monitor.

b. Adjust the width coil, L101, for desired height.

5-26. FOCUS ADJUSTMENT. The focus control, R107, provides an adjustment for maintaining best overall display focus. However, because of the construction of the gun assembly, in the CRT this control has only small effect on focus.

5-27. CENTERING. If the raster is not centered properly, it may be repositioned by rotating the ring magnets behind the deflection yoke. The ring magnets should not be used to offset the raster from its nominal center position because it would degrade the resolution of the display. If the picture is tilted, rotate the entire yoke.

5-28. PERFORMANCE TEST PROCEDURE

5-29. Performance tests on the receiver involve use of the automatic self-test routine and measurement of the module test point characteristics to verify normal operation. The test equipment required for test point measurement is listed in table 5-1.

5-30. RECEIVER TEST. The receiver test routine activated by the front panel TEST switch, performs a self diagnostic check of receiver functional circuits and power supplies. When the test is initiated, a calibrated test signal is injected into the receiver front end at a point close to the antenna input. The calibrated test signal, in conjunction with synthesizer inputs, is subjected to exactly the same filtering and IF treatment as is a received RF signal. The results of a test are an audible monitor tone, a go/no-go lamp indication, and a solid bar (350 Hz signal) across the CRT screen. The test is performed with the receiver sweeping in either manual or program mode, as follows:

a. Press the TEST switch, and hold depressed for 10 seconds.

b. Within five seconds, check that the green RCVR lamp lights. If the red lamp remains lighted, a malfunction is indicated. Refer to step 9, table 5-3 for additional checks to isolate malfunction.

c. On the CRT, verify that a, horizontal line is displayed at 350 Hz (approximately mid screen on the CRT or 3/4-inch (2 cm) below the bottom of the AGC bargraph) and that a fixed tone (1050 Hz) is audible.

d. AGC bargraph should display four cells (plus or minus one cell).

5-31. TEST POINT VERIFICATION. Figures 5-4 through 5-11 provide a description of test point parameters. Used in conjunction with the schematics, test point measurements enable a fault indication to be diagnosed and isolated. All test point parameters have expected or nominal test results and include tolerances where applicable.

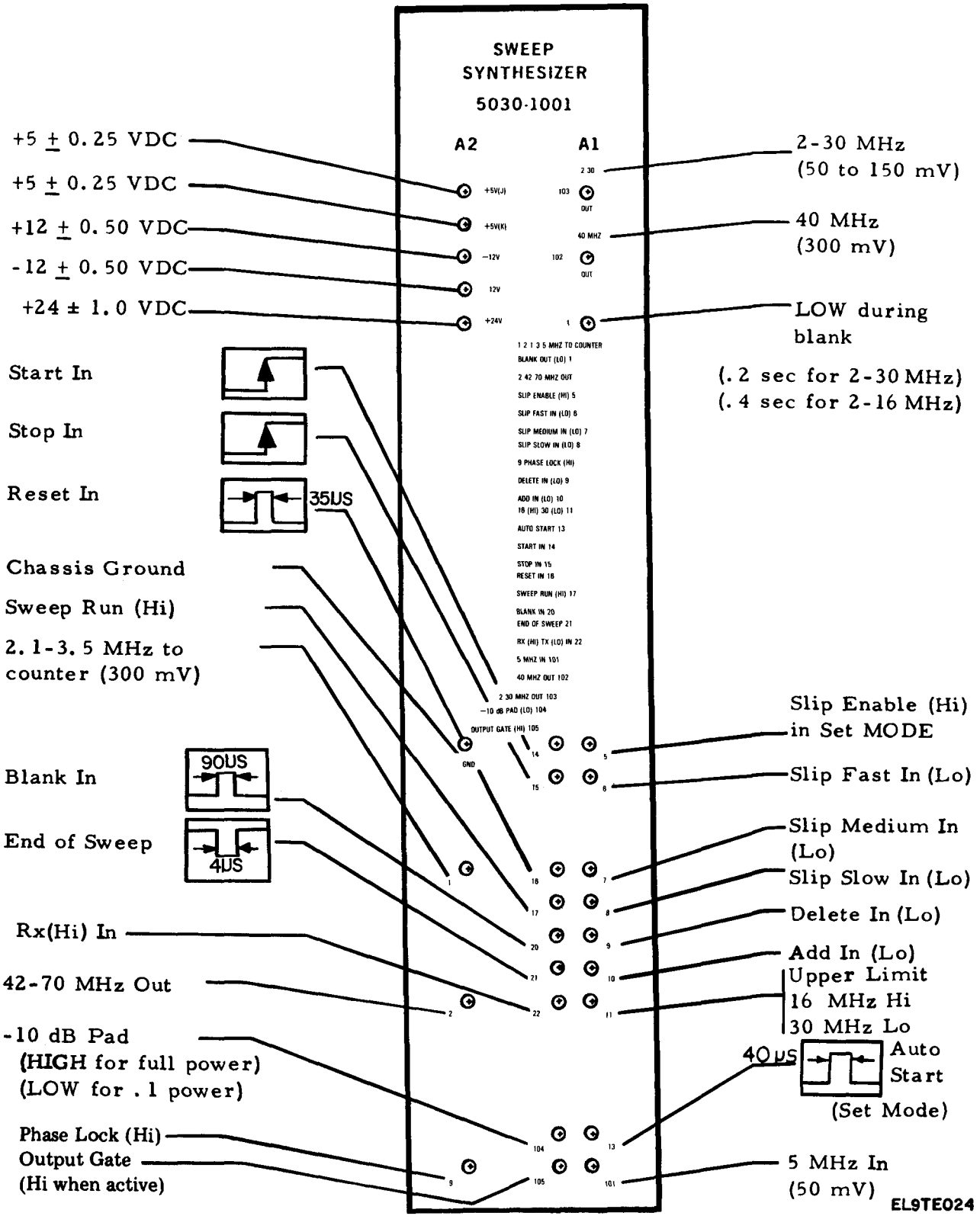


FIGURE 5-4. Test Point Verification for Sweep Synthesizer Module (2A1) (P/N 5030-1001 Only).

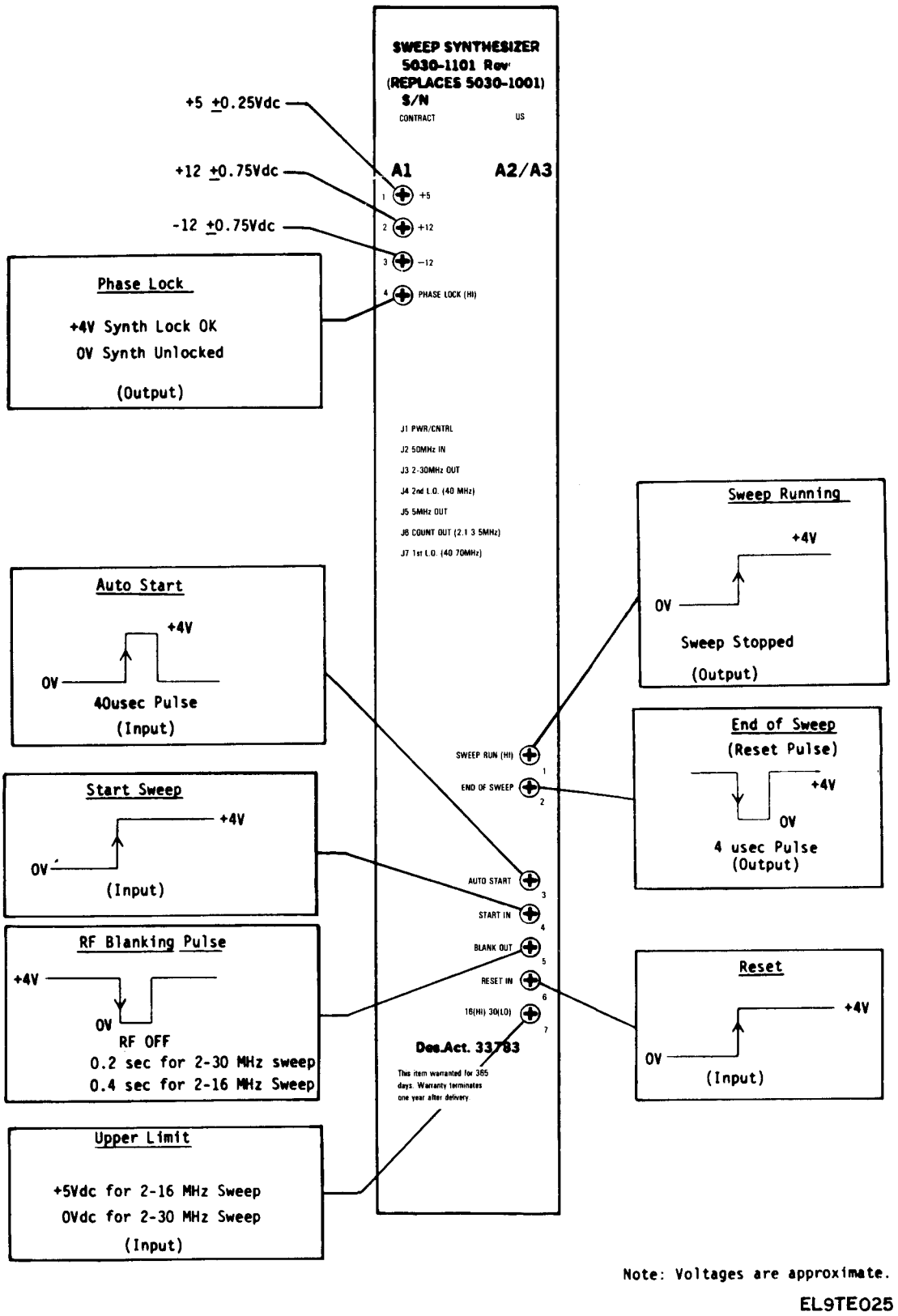


FIGURE 5-5. Test Point Verification for Synthesizer Module (2A1) (P/N 5030-1101 Only).

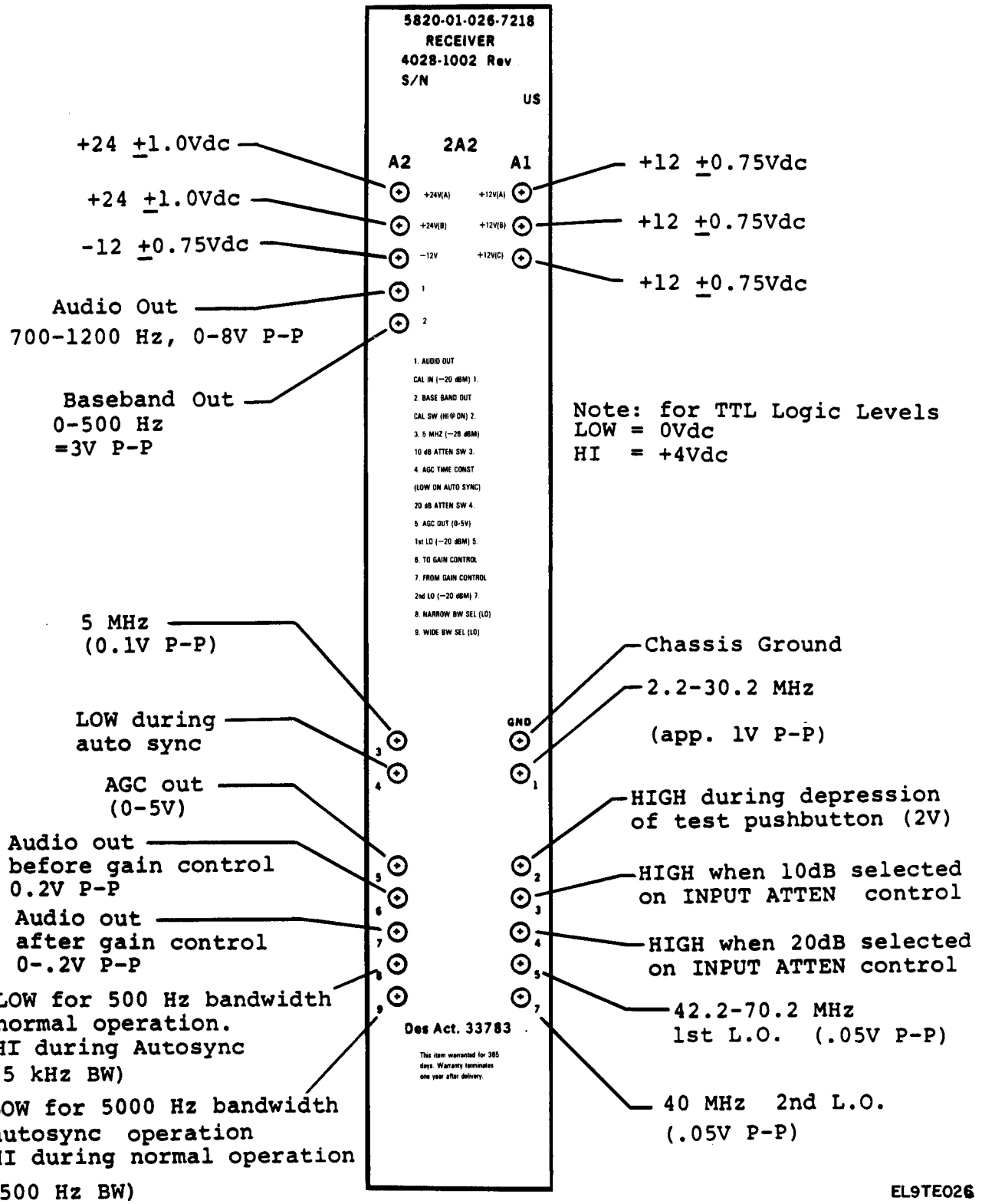


FIGURE 5-6. Test Point Verification for Receiver Module 2A2.

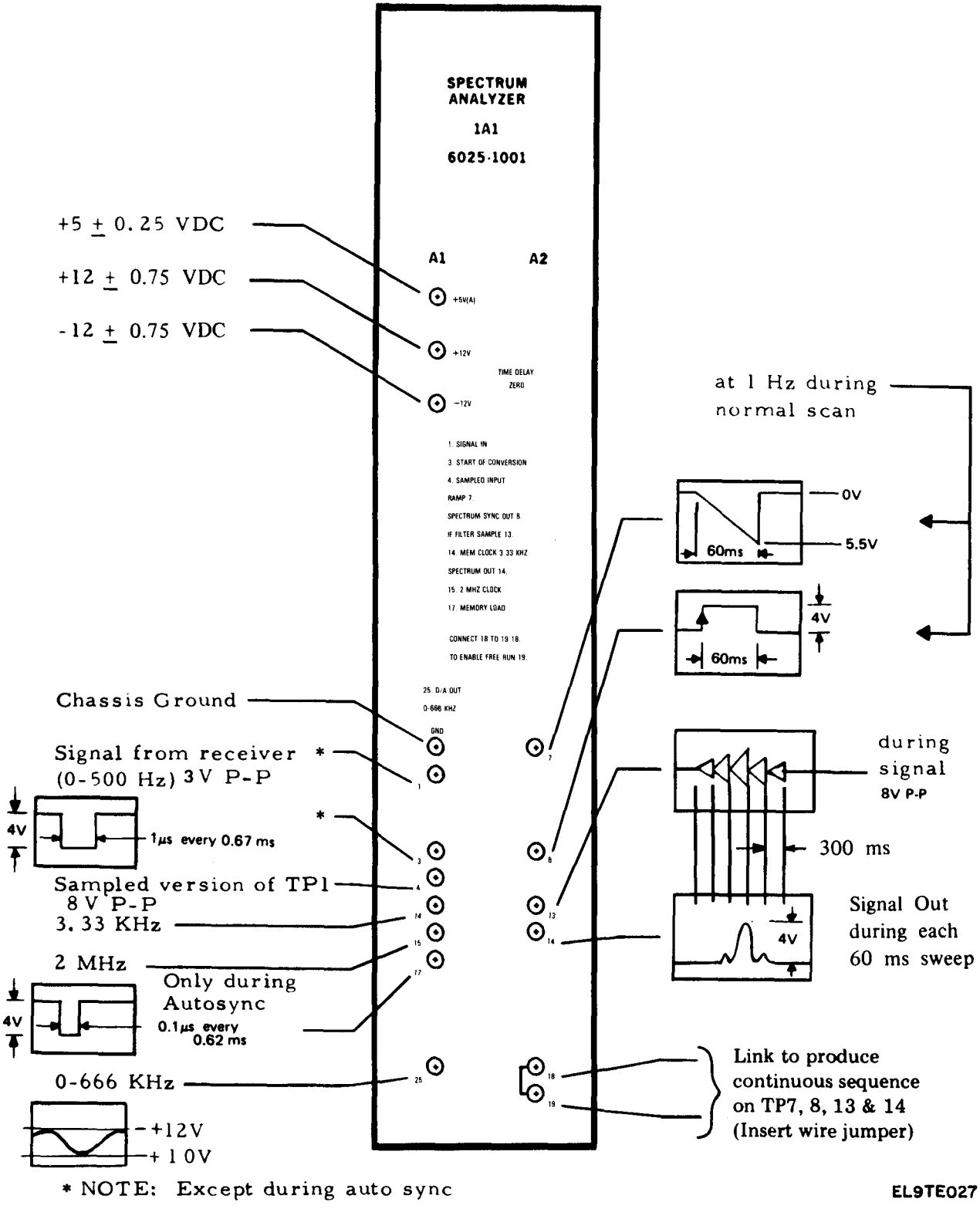


FIGURE 5-7. Test Point Verification for Spectrum Analyzer Module 1A1.

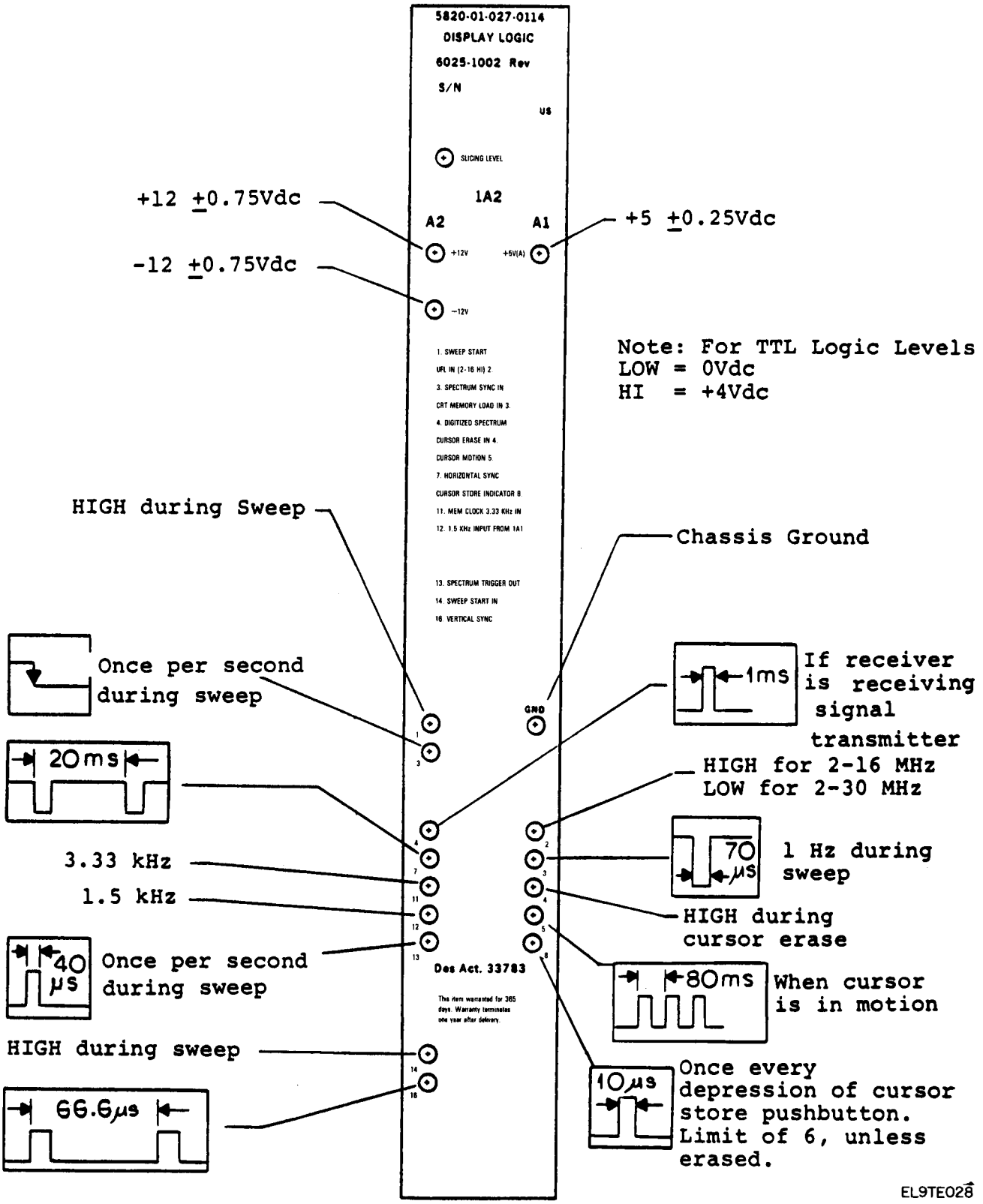


FIGURE 5-8. Test Point Verification for Display Logic Module 1A2.

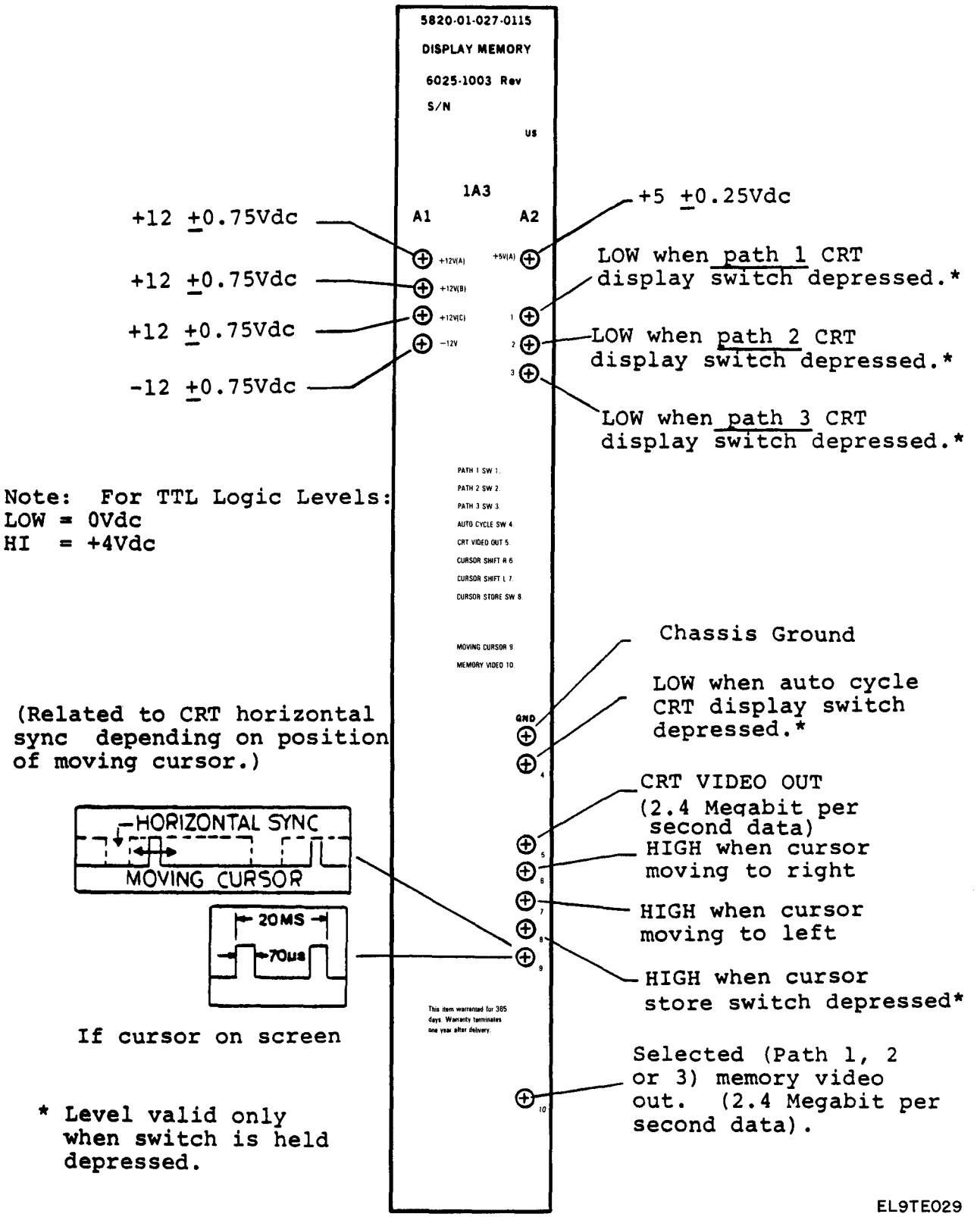


FIGURE 5-9. Test Point Verification for Display Memory Module 1A3.

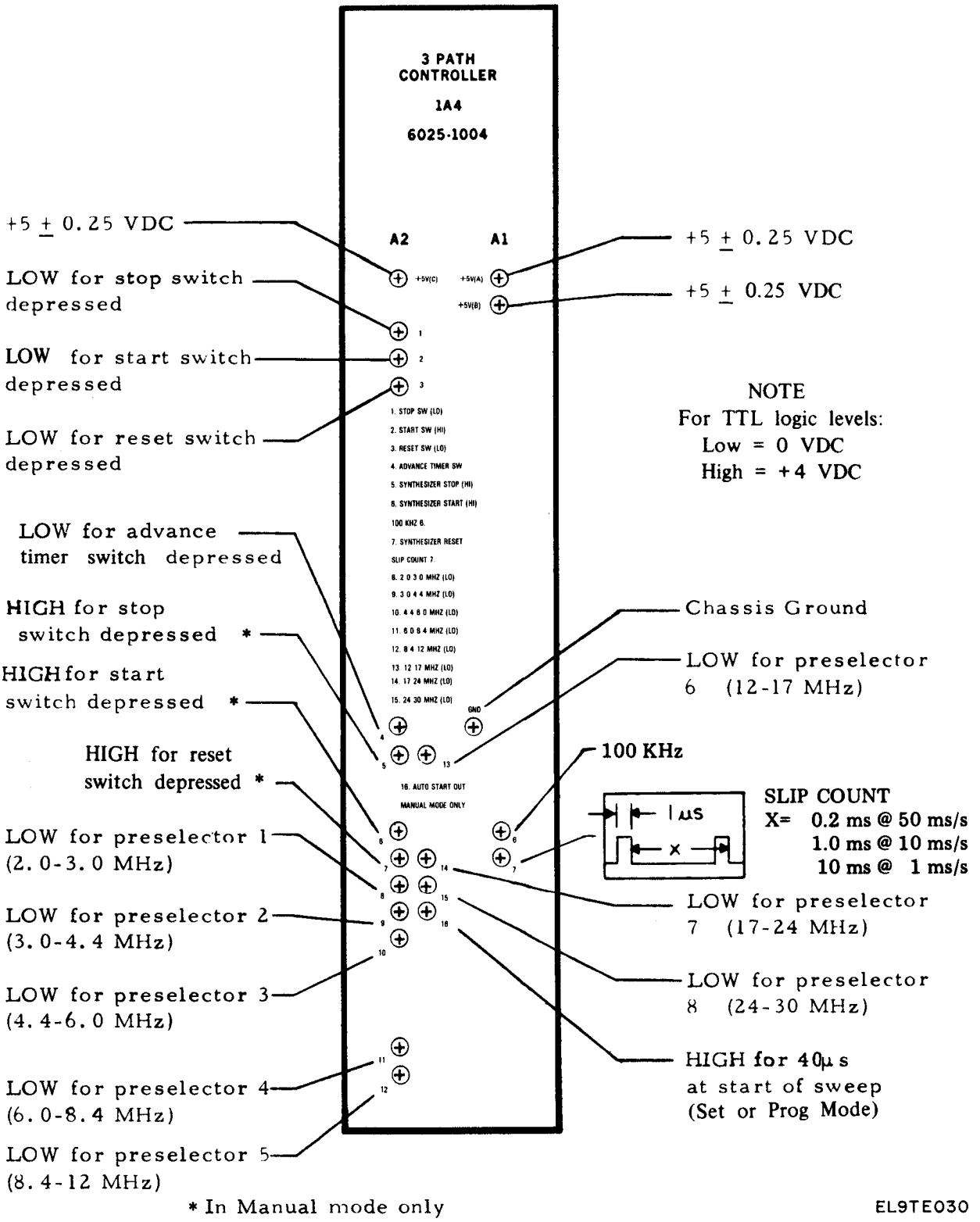


FIGURE 5-10. Test Point Verification for 3-Path Controller Module 1A4.

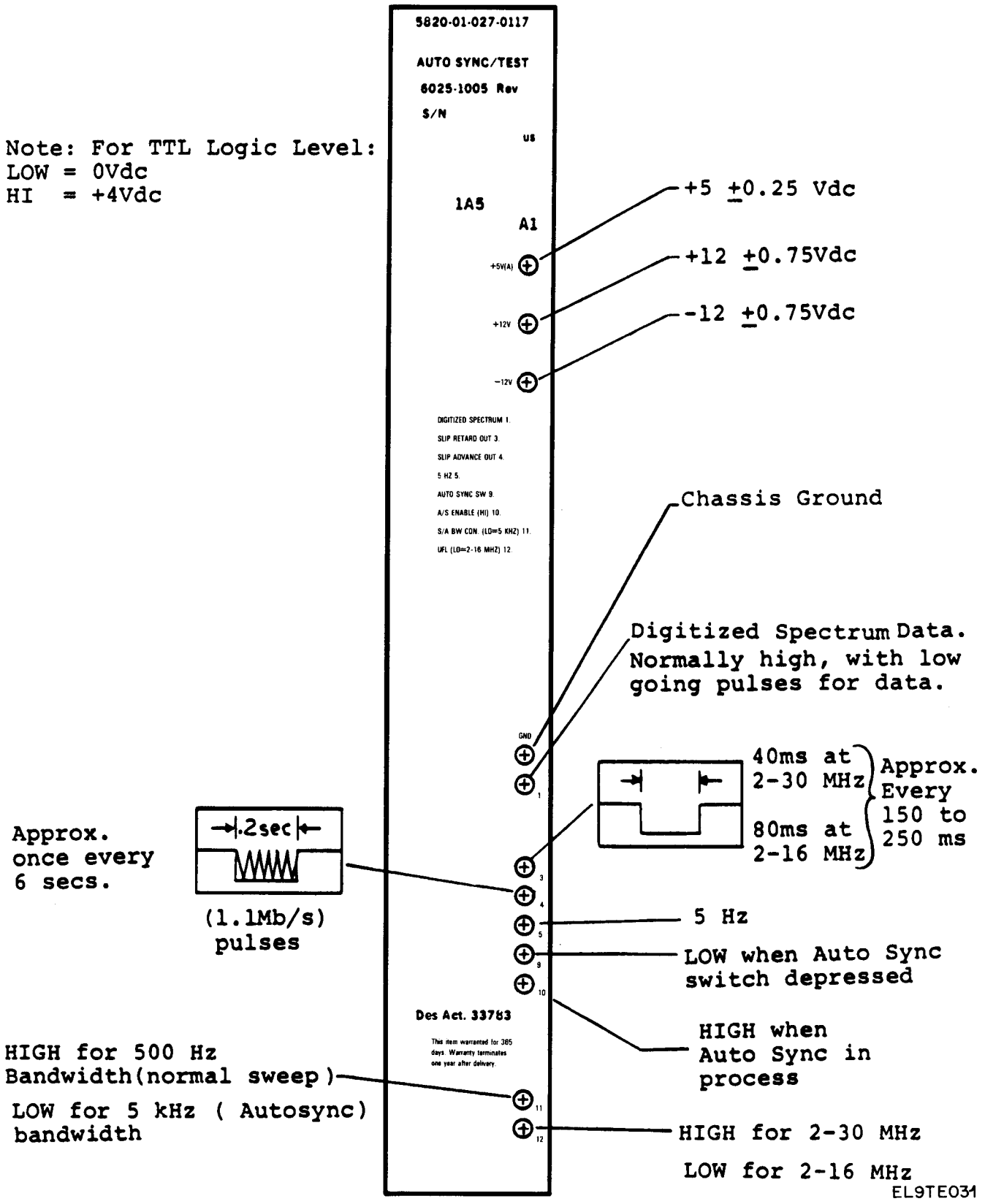


FIGURE 5-11. Test Point Verification for Auto Sync 1 Test Module 1A5.

SECTION 6

WIRE LIST INDEX

6-1. WIRE LIST INDEX The wire lists for the RCS-4B are compiled in this section in the sequence as listed below.

NOTE

Wiring for Sweep Synthesizer Assy (5030-1101) is diagrammed in figure FO-23.7.

WIRE NO	ITEM NO	COLOR	FROM DEVICE	PIN NO	TO DEVICE	PIN NO	LENGTH	REMARKS
1	21	—	4028-J1	—	6043-J1A	—	—	ANT 1
2	20	—	4028-J2	—	6043-J2A	—	—	ANT 2
3	19	—	4028-J3	—	6043-J3A	—	—	ANT 3

SIZE	CODE IDENT NO	DWG NO		REV
A	33783	WL	9225-1000 and 9225-1100	A

SHEET 2 OF 2

RCS-4B Receiver (9225-1000 and 9225-1100)

WIRE Nº	ITEM Nº	COLOR	FROM DEVICE	PIN Nº	TO DEVICE	PIN Nº	LENGTH	REMARKS
1	6		6025-J2		4028-J5			CONTROL
2	15		6025-J3		4028-J4			5 MHz
3	15		6025-J4		4028-J9			L.O. COUNT
4	9		6025-J1		4028-J6			POWER SUPPLY
5	12		4028-J7					POWER PLUG

SIZE	CODE IDENT Nº	DWG Nº		REV
A	33783	WL	9125-1000 and 9125-1100	D

SHEET 2 OF 2

RCS-4B Chirpsounder Receiver (9125-1000 and 9125-1100)

WIRE Nº	ITEM Nº	COLOR	FROM DEVICE	PIN Nº	TO DEVICE	PIN Nº	LENGTH	REMARKS
3	4		J1	IN	A1	1N		ANT 1 IN
5	3		J1	A	A1	1A		ANT 1 OUT
4	4		J1	B	A1	1B		" "
2	3		J1	C	A1	1C		" "
1	3		J1	D	A1	1D		" "
13	3		J2	IN	A2	2N		ANT 2 IN
15	5		J2	A	A2	2A		ANT 2 OUT
14	5		J2	B	A2	2B		" "
12	5		J2	C	A2	2C		" "
11	5		J2	D	A2	2D		" "
8	4		J3	IN	A3	3N		ANT 3 IN
10	3		J3	A	A3	3A		ANT 3 OUT
9	4		J3	B	A3	3B		" "
7	3		J3	C	A3	3C		" "
6	3		J3	D	A3	3D		" "

SIZE	CODE IDENT Nº	DWG Nº	REV
A	33783	WL 6043-1000	C

SHEET 2 OF 2

6043 Power Divider - Unit 3 (6043-1000)

WIRE NO	ITEM NO	COLOR	FROM DEVICE	PIN NO	TO DEVICE	PIN NO	LENGTH	REMARKS
			1A11A1	P15	1A11A2	J6		
			1A11A2	P1	1A1	J1		
			1A11A2	P2	1A2	J1		
			1A11A2	P3	1A3	J1		
			1A11A2	P4	1A4	J1		
			1A11A2	P6	1A4	J3		
			1A11A2	P7	1A5	J1		
			1A11A2	P8	1A5	J2		
			1A11A2	P9	1A6	J1		
			1A11A2	P10	1A10	J2		
			1A11A2	P11	1A10	J1		
			1A11A2	P12	1A4	J4		
			1A11A2	P13	1A6	J2		
			1A11A2	P14	1A7	J1		
			1A11A2	P16	1A5	J3		
			1A11A2	P17	1A6	J4		
			1A11A2	P18	1A4	J5		
			1A11A2	P19	1A6	J3		
			1A11A2	P20	1A8	P1		
			1A9	P1	1A4	J2		

SIZE	CODE IDENT NO	DWG NO	REV
A	33783	WL 6025-1000	D

SHEET 2 OF 2

6025 Control/Display - Unit 1 (6025-1000)

WIRE Nº	ITEM Nº	COLOR	FROM DEVICE	PIN Nº	TO DEVICE	PIN Nº	LENGTH	REMARKS
1	6	0	J1	1	A1	E11		GND
2	6	0	J1	2	A1	E29		GND
3	6	2	J1	3	A1	E8		+5V
4			J1	4				
5			J1	5				
6	6	3	J1	6	A1	E9		+12V
7	6	6	J1	7	A1	E10		-12V
8			J1	8				
9			J1	9				
10	7	90	J1	10	A2	E34		SYNC B
11	7	91	J1	11	A2	E34		SYNC B
12	7	92	J1	12	A2	E42		TRIG IN
13	7	93	J1	13	A1	E17		1.5K
14	7	94	J1	14	A1	E21		MTA-2/SAM
15	7	95	J1	15	A1	E12		SIGNAL IN [1]
16	7	0	J1	16	A1	E11		GND [1]
17	7	96	J1	17	A2	E25		SPECTRUM OUT
18	7	96	J1	18	A2	E25		SPECTRUM OUT
19	7	97	J1	19	A1	E15		500 Hz
20	7	98	J1	20	A1	E14		5 kHz
21								
22	6	0	A1	E13	A2	E31		GND
23	6	2	A1	E8	A2	E27		+5 V
24	6	3	A1	E9	A2	E29		+12V
25	6	6	A1	E10	A2	E37		-12V

SIZE	CODE IDENT Nº	DWG Nº	REV
A	33783	WL 6025-1001	F

SHEET 2 OF 3

Spectrum Analyzer Assy (6025-1001) (Sheet 1 of 2)

WIRE NO	ITEM NO	COLOR	FROM DEVICE	PIN NO	TO DEVICE	PIN NO	LENGTH	REMARKS
26	7	901	A1	E27	A2	E40		2MHz [1]
27	7	0	A1	E26	A2	E39		GND [1]
28	7	912	A1	E23	A2	E33		MTB
28	7	913	A1	E22	A2	E28		MTA1
30	7	914	A1	E7	A2	E24		DATA OUT/0-666 [1]
31	7	0	A1	E29	A2	E23		GND [1]
32								
33	7	2	A1	E8	casting TP (A1 side)	+5VA		+5V
34	7	3	A1	E9	casting TP (A1 side)	+12V		+12V
35	7	6	A1	E10	casting TP (A1 side)	-12V		-12V
36	16		A1	TP1	casting TP (A1 side)	1		ANALOG IN
37	16		A1	TP3	casting TP (A1 side)	3		START OF CONVERSION
38	16		A1	TP4	casting TP (A1 side)	4		SAMPLED INPUT
39	16		A1	TP14	casting TP (A1 side)	14		MEMORY TAIL
40	16		A1	TP15	casting TP (A1 side)	15		MEMORY CLOCK
41	16		A1	TP17	casting TP (A1 side)	17		LOAD MEM BUFFER
42	16		A1	TP25	casting TP (A1 side)	25		DATA OUT/0-666 kHz
43	16		A2	TP7	casting TP (A2 side)	7		RAMP
44	16		A2	TP8	casting TP (A2 side)	8		SPECTRUM SYNC
45	16		A2	TP13	casting TP (A2 side)	13		IF FILTER SAMPLE
46	16		A2	TP14	casting TP (A2 side)	14		SPECTRUM OUT
47	7		A2	E43	casting TP (A2 side)	18		EXT TRIG EN
48	7	2	A2	E27	casting TP (A2 side)	19		+5V

SIZE	CODE IDENT NO	DWG NO	REV
A	33783	WL 6025-1001	F

SHEET 3 OF 3

Spectrum Analyzer Assy (6025-1001) (Sheet 2 of 2)

WIRE NO	ITEM NO	COLOR	FROM DEVICE	PIN NO	TO DEVICE	PIN NO	LENGTH	REMARKS
1	8	0	J1	1	A1	E42		GND
2	8	0	J1	2	A2	E24		GND
3	8	2	J1	3	A1	E41		+5V
4			J1	4				
5			J1	5				
6			J1	6				
7	8	6	J1	7	A2	E8		-12V
8	8	3	J1	8	A2	E7		+12V
9			J1	9				
10	7	90	J1	10	A2	E49		S/S/SRS
11	7	91	J1	11	A2	E1		SA SYNC
12	7	92	J1	12	A2	E5		SA TRIG
13	7	93	J1	13	A2	E52		1.5K
14	7	94	J1	14	A1	E22		UFL
15	7	95	J1	15	A2	E3		PD1/PDC1
16	7	96	J1	16	A2	E2		PD2/PDC2
17	7	97	J1	17	A2	E31		THS
18	7	98	J1	18	A2	E13		SAM
19	7	901	J1	19	A2	E15		SRE
20	7	902	J1	20	A2	E16		SRO
21	7	903	J1	21	A2	E43		SLB
22	7	904	J1	22	A2	E14		SSD
23	7	904	J1	23	A2	E14		SSD
24	7	905	J1	24	A2	E11		SPEC
25	7	906	J1	25	A2	E27		VS1

SIZE	CODE IDENT NO	DWG NO	REV
A	33783	WL 6025-1002	C

SHEET 2 OF 5

Display Logic Assy **(6025-1002) (Sheet 1 of 4)**

WIRE NO	ITEM NO	COLOR	FROM DEVICE	PIN NO	TO DEVICE	PIN NO	LENGTH	REMARKS
26	7	907	J1	26	A2	E23		VERT
27	7	908	J1	27	A2	E29		01A
28	7	912	J1	28	A2	E18		02A
29	7	913	J1	29	A2	E20		CSA1
30	7	914	J1	30	A2	E19		CSB1
31	7	915	J1	31	A2	E21		CSC1
32	7	916	J1	32	A2	E22		CSD1
33	7	917	J1	33	A2	E17		TVS
34	7	918	J1	34	A2	E32		EQT
35	7	923	J1	35	A2	E12		AGC
36	7	924	J1	36	A2	E9		PNG
37	7	925	J1	37	A2	E10		FMK
38	7	926	J1	38	A2	E4		SNG
39	7	927	J1	39	A1	E43		CLD
40	7	928	J1	40	A1	E13		UCS
41	7	90	J1	41	A1	E14		DCS
42	7	91	J1	42	A1	E15		CCC
43	7	92	J1	43	A1	E17		CCK
44	7	93	J1	44	A1	E16		CUL
45	7	94	J1	45	A1	E18		SAC
46	7	95	J1	46	A1	E26		EC1
47	7	96	J1	47	A2	E28		01B
48	7	97	J1	48	A2	E25		02B
49	7	91	J1	49	A2	E1		SA SYNC
50	7	905	J1	50	A2	E11		SPEC

SIZE	CODE IDENT NO	DWG NO	REV
A	33783	WL 6025-1002	C

SHEET 3 OF 5

Display Logic Assy (6025- 1002) (Sheet 2 of 4)

WIRE Nº	ITEM Nº	COLOR	FROM DEVICE	PIN Nº	TO DEVICE	PIN Nº	LENGTH	REMARKS
51	7	98	J1	51	A2	E13		SAM/MTA-2
52	7	90	J1	52	A2	E56		S/S/SRS
53	7	923	J1	53	A2	E12		AGC
54	7	98	J1	54	A2	E44		SLR
55	7	94	J1	55	A1	E22		UFL
56								
57	7	98	A1	E19	A2	E53		RSO
58	7	901	A1	E32	A2	E41		CMP0
59	7	902	A1	E34	A2	E40		CMP1
60	7	903	A1	E33	A2	E39		CMP2
61	7	904	A1	E36	A2	E36		CMP3
62	7	905	A1	E37	A2	E37		CMP4
63	7	906	A1	E38	A2	E38		CMP5
64	7	907	A1	E35	A2	E33		CMP6
65	7	908	A1	E39	A2	E34		CMP7
66	7	912	A1	E40	A2	E35		CMP8
67	7	0	A1	E21	A1	E42		2MHz
68	7	0	A1	E42	A2	E24		GND
69	8	2	A1	E41	A2	E42		+5V
70	7	94	A1	E22	A2	E51		UFL
71	7	906	A1	E25	A2	E27		VS1
72	7	913	A1	E31	A2	E20		CSA1
73	7	914	A1	E29	A2	E19		CSB1
74	7	915	A1	E28	A2	E21		CSC1
75	7	916	A1	E27	A2	E22		CSD1

SIZE	CODE IDENT Nº	DWG Nº	REV
A	33783	WL 6025-1002	C

SHEET 4 OF 5

Display Logic Assy (6025-1002) (Sheet 3 of 4)

WIRE Nº	ITEM Nº	COLOR	FROM DEVICE	PIN Nº	TO DEVICE	PIN Nº	LENGTH	REMARKS
76	7	918	A1	E30	A2	E32		EOT
77	7	94	A2	E51	A2	E46		UFL/SWEEP RATE 100
78	7	90	A2	E56	A2	E55		START/STOP
79	7		A1	E41	casting TP (A1 side)	+5VA		+5VA
80	16		A1	TP2	casting TP (A1 side)	2		Upper Frequency Limit (High 2-16/low, 2-30)
81	16		A1	TP3	casting TP (A1 side)	3		CRT MEMORY LOAD IN
82	16		A1	TP4	casting TP (A1 side)	4		CURSOR ERASE IN
83	16		A1	TP5	casting TP (A1 side)	5		CURSOR MOTION
84	16		A1	TP8	casting TP (A1 side)	8		CURSOR STORE INDICATOR
85	7		A2	E7	casting TP (A2 side)	+12V		+12V
86	7		A2	E8	casting TP (A2 side)	-12V		-12V
87	16		A2	TP1	casting TP (A2 side)	1		SWEEP START
88	16		A2	TP3	casting TP (A2 side)	3		SPECTRUM SYNC IN
89	16		A2	TP4	casting TP (A2 side)	4		DIGITIZED SPECTRUM
90	16		A2	TP7	casting TP (A2 side)	7		HORIZONTAL SYNC
91	16		A2	TP11	casting TP (A2 side)	11		MEM CLOCK
92	16		A2	TP12	casting TP (A2 side)	12		1.5 kHz INPUT
93	16		A2	TP13	casting TP (A2 side)	13		SPECTRUM TRIGGER OUT
94	16		A2	TP14	casting TP (A2 side)	14		SWEEP START IN
95	16		A2	TP16	casting TP (A2 side)	16		VERTICAL SYNC

SIZE	CODE IDENT Nº	DWG Nº	REV
A	33783	WL 6025-1002	C

SHEET 5 OF 5

Display Logic Assy (6025-1002) (Sheet 4 of 4)

WIRE NO	ITEM NO	COLOR	FROM DEVICE	PIN NO	TO DEVICE	PIN NO	LENGTH	REMARKS
1	10	0	J1	1	A2	E1		GND
2	10	0	J1	2	A1	E25		GND
3	10	2	J1	3	A2	E15		+5V
4			J1	4				
5	10	1	J1	5	A2	E47		+5C
6	10	3	J1	6	A1	E11		+12V/+12VA
7	10	6	J1	7	A1	E12		-12V
8	10	3	J1	8	A1	E14		+12V/+12VB
9	10	3	J1	9	A1	E23		+12V/+12VC
10	7	90	J1	10	A2	E46		PD1
11	7	91	J1	11	A2	E45		PD2
12	7	92	J1	12	A2	E43		PD3
13	7	93	J1	13	A2	E49		PDC1
14	7	94	J1	14	A2	E48		PDC2
15	7	95	J1	15	A2	E19		THS
16	7	96	J1	16	A2	E56		SRE
17	7	97	J1	17	A2	E55		SRO
18	7	98	J1	18	A2	E52		SLB
19	7	901	J1	19	A2	E50		SSD
20	7	902	J1	20	A2	E20		VS1
21	7	903	J1	21	A2	E53		01
22	7	904	J1	22	A2	E54		Ø2
23	7	905	J1	23	A2	E33		CSA1
24	7	906	J1	24	A2	E36		CSB1
25	7	907	J1	25	A2	E35		CSC1

SIZE	CODE IDENT NO	DWG NO	REV
A	33783	WL 6025-1003	E

SHEET 2 OF 5

Display Memory Assy (6025-1003) (Sheet 1 of 4)

WIRE NO	ITEM NO	COLOR	FROM DEVICE	PIN NO	TO DEVICE	PIN NO	LENGTH	REMARKS
26	7	908	J1	26	A2	E34		CSD1
27	7	912	J1	27	A2	E31		EQT
28	7	913	J1	28	A2	E13		PNG
29	7	914	J1	29	A2	E17		FMK
30	7	915	J1	30	A2	E37		SNG
31	7	916	J1	31	A2	E24		LC1
32	7	917	J1	32	A2	E25		LC2
33	7	918	J1	33	A2	E30		CLD
34	7	923	J1	34	A2	E22		UCS
35	7	924	J1	35	A2	E23		DCS
36	7	925	J1	36	A2	E27		RS1
37	7	926	J1	37	A2	E26		RS2
38	7	927	J1	38	A2	E28		LS1
39	7	928	J1	39	A2	E29		LS2
40	7	90	J1	40	A2	E16		PVO
41	7	91	J1	41	A2	E60		SAC
42	7	92	J1	42	A2	E38		AC1
43	7	93	J1	43	A2	E39		ACL/AC2
44	7	94	J1	44	A2	E41		PDL1
45	7	95	J1	45	A2	E42		PDL2
46	7	96	J1	46	A2	E40		PDL3
47	7	97	J1	47	A2	E44		LPT/LT
48	7	98	J1	48	A2	E59		MLS1/TVL1
49	7	901	J1	49	A2	E58		MLS2/TVL2
50	7	902	J1	50	A2	E57		MLS3/TVL3

SIZE	CODE IDENT NO	DWG NO	REV
A	33783	WL 6025-1003	E

SHEET 3 OF 5

Display Memory Assy (6025-1003) (Sheet 2 of 4)

WIRE Nº	ITEM Nº	COLOR	FROM DEVICE	PIN Nº	TO DEVICE	PIN Nº	LENGTH	REMARKS
51	7	903	J1	51	A1	E16		B01
52	7	904	J1	52	A1	E15		B02
53				53				
54				54				
55	7	97	J1	55	A2	E51		MAN
56	7	91	A1	MI1	A2	E13		MI1
57	7	901	A1	E10	A2	E6		M01
58	7	92	A1	MI2	A2	E9		MI2
59	7	902	A1	E13	A2	E3		MO2
60	7	93	A1	MI3	A2	E12		MI3
61	7	903	A1	E17	A2	E5		MO3
62	7	94	A1	MI4	A2	E8		MI4
63	7	904	A1	E19	A2	E4		MO4
64	7	95	A1	MI5	A2	E11		MI5
65	7	905	A1	E22	A2	E7		MO5
66	7	96	A1	MI6	A2	E10		MI6
67	7	906	A1	E24	A2	E2		MO6
68	10	0	A1	E25	A2	E1		GND
69	10	2	A1	E18	A2	E15		+5V
70								
71								
72	7	903	A1	E16	A1	E9		A01/B01
73	7	903	A1	E16	A1	E21		B01/C01
74	7	904	A1	E15	A1	E8		A02/B02
75	7	904	A1	E15	A1	E20		B02/C02

SIZE	CODE IDENT Nº	DWG Nº	REV
A	33783	WL 6025-1003	E

SHEET 4 OF 5

Display Memory Assy (6025-1003) (Sheet 3 of 4)

WIRE Nº	ITEM Nº	COLOR	FROM DEVICE	PIN Nº	TO DEVICE	PIN Nº	LENGTH	REMARKS
76	16		A2	TP1	CASTING TP	1		PATH 1 SW.
77	16		A2	TP2	CASTING TP	2		PATH 2 SW.
78	16		A2	TP3	CASTING TP	3		PATH 3 SW
79	16		A2	TP4	CASTING TP	4		AUTO CYCLE
80	16		A2	TP5	CASTING TP	5		DISPLAY VIDEO
81	16		A2	TP6	CASTING TP	6		CURSOR R SHIFT
82	16		A2	TP7	CASTING TP	7		CURSOR L SHIFT
83	16		A2	TP8	CASTING TP	8		LOAD CURSOR
84	16		A2	TP9	CASTING TP	9		MOVE CURSOR
85	16		A2	TP10	CASTING TP	10		MEM VIDEO
86	7	3	A1	E11	CASTING +12VA			+12VA
87	7	6	A1	E12	CASTING -12V			-12V
88	7	3	A1	E14	CASTING +12VB			+12VB
89	7	3	A1	E23	CASTING +12VC			+12VC
90	10	2	A2	E15	CASTING +5V			+5V

SIZE	CODE IDENT Nº	DWG Nº	REV
A	33783	WL 6025-1003	F

SHEET 5 OF 5

Display Memory Assy (6025-1003) (Sheet 4 of 4)

WIRE Nº	ITEM Nº	COLOR	FROM DEVICE	PIN Nº	TO DEVICE	PIN Nº	LENGTH	REMARKS
1	11	1	J1	1	A1	E1		GND
2	11	1		2	A2	E1		GND
3	11	2		3	A1	E6		+5 VA
4	11	5		4	A1	E11		+5 B
5	30	4		5	A2J1	15		+5C
6				6				
7	8	91		7	A2	E27		TVL1/ MLS1
8	8	92		8	A2	E28		TVL2/ MLS2
9	8	93		9	A2	E29		TVL3/ MLS3
10	30	2		10	A1J6	16		CFS (Cursor Freq Select)
11	30	94		11	A1J6	10		CCC (Start Cursor Count)
12	30	96		12	A1J6	9		CCK (Cursor Clock)
13	30	92		13	A1J6	11		CUL (Cursor Upper Limit)
14	30	7		14	A2J3	4		TVL1/ MLS1
15	8	91		15	A2	E27		TVL1/ MLS1
16	30	9		16	A2J3	5		TVL2/ MLS2
17	8	92		17	A2	E28		TVL2/ MLS2
18	30	1		18	A2J3	1		TVL3/ MLS3
19	8	93		19	A2	E29		TVL3/ MLS3
20	30	6		20	A1J2	14		ASA
21	30	8		21	A1J2	13		ASD
22	30	6		22	A2J3	14		LT/LPT (Lamp Test)
23	8	6		23	A2	E26		LT/LPT (Lamp Test)
24	31	3		24	A1 J2	2		DEL (Delete)
25	8	3	J1	25	A1	E23		DEL (Delete)

SIZE	CODE IDENT Nº	DWG Nº	REV
A	33783	WL 6025-1004	C

SHEET 2 OF 9

3-Path Programmer Assy (6025-1004) (Sheet 1 of 8) (S/N 100101 and on)

WIRE NO	ITEM NO	COLOR	FROM DEVICE	PIN NO	TO DEVICE	PIN NO	LENGTH	REMARKS
26	31	94	J1	26	A1J2	10		ADD
27	8	94		27	A1	E24		ADD
28	31	2		28	A1J2	16		SLF
29	31	92		29	A1J2	11		SLM
30	31	0		30	A1J2	12		SLS
31	30	93		31	A2J3	7		STP
32	30	95		32	A2J3	8		STR
33	30	96		33	A2J3	9		RES
34	30	94		34	A2J3	10		SSDA
35	30	0		35	A2J3	12		AST
36	30	9		36	A1J6	5		PRE 1
37	30	91		37	A1J6	6		PRE 2
38	30	5		38	A1J6	3		PRE 3
39	30	7		39	A1J6	4		PRE 4
40	30	1		40	A1J6	1		PRE 5
41	30	3		41	A1J6	2		PRE 6
42	30	95		42	A1J6	8		PRE 7
43	30	93		43	A1J6	7		PRE 8
44	8	901		44	J1	54		EOS
45	8	2		45	A1	E27		SLF (SLIP FAST)
46	8	92		46	A1	E26		SLM (SLIP MEDIUM)
47	8	0		47	A1	E25		SLS (SLIP SLOW)
48	30	8		48	A2J1	13		SET 1
49	30	9		49	A2J1	5		SET 2
50	30	0	J1	50	A2J1	12		SET 3

SIZE	CODE IDENT NO	DWG NO	REV
A	33783	WL 6025-1004	C

SHEET 3 OF 9

3-Path Programmer Assy (6025-1004) (Sheet 2 of 8) (S/N 400101 and on)

WIRE NO	ITEM NO	COLOR	FROM DEVICE	PIN NO	TO DEVICE	PIN NO	LENGTH	REMARKS
51	31	9	J1	51	A1J2	5		PPS
52	30	91	J1	52	A2J3	6		SRS
53			J1	53				
54								
55	30	91	J1	55	A2J1	6		MAN
56								
57	30	3	J2	1	A2J3	2		GND
58	30	5		2	A2J3	3		+5VC
59	31	7		3	A1J2	4		PLX (PATH 1)
60	31	5		4	A1J2	3		PLY (" 2)
61	31	96		5	A1J2	9		PLS (PATH STROBE)
62	30	7		6	A1J5	4		4D1/10kHz-"1"
63	30	9		7	A1J5	5		4D2/10kHz-"2"
64	30	91		8	A1J5	6		4D4/10kHz-"4"
65	30	5		9	A1J5	3		4D8/10kHz-"8"
66	30	1		10	A1J5	1		5D1/100kHz-"1"
67	30	95		11	A1J5	8		5D2/100kHz-"2"
68	30	93		12	A1J5	7		5D4/100kHz-"4"
69	30	3		13	A1J5	2		5D8/100kHz-"8"
70	30	4		14	A1J5	15		6D1/MHz-"1"
71	30	0		15	A1J5	12		6D2/MHz-"2"
72	30	96		16	A1J5	9		6D4/MHz-"4"
73	30	2		17	A1J5	16		6D8/MHz-"8"
74	30	6		18	A1J5	14		7D1/10MHz-"1"
75	30	8	J2	19	A1J5	13		7D2/10MHz-"2"

SIZE	CODE IDENT NO	DWG NO	REV
A	33783	WL 6025-1004	C
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3-Path Programmer Assy (6025-1004) (Sheet 3 of 8) (S/N 400101 and on)

WIRE Nº	ITEM Nº	COLOR	FROM DEVICE	PIN Nº	TO DEVICE	PIN Nº	LENGTH	REMARKS
76	30	94	J2	20	A1J5	10		7D4/10MHz-"4"
77	8	6		21	A2	E26		LT/LPT
78	31	1		22	A2J4	1		1S1/Sec-"1"
79	31	2		23	A2J4	16		1S2/Sec-"2"
80	31	3		24	A2J4	2		1S4/Sec"4"
81	31	4		25	A2J4	15		1S8/Sec"8"
82	31	5		26	A2J4	3		10S1/10Sec-"1"
83	31	6		27	A2J4	14		10S2/10 Sec - "2"
84	31	7		28	A2J4	4		10S4/10Sec - "4"
85	31	9		29	A2J4	5		10S8/10 Sec - "8"
86	31	8		30	A2J4	13		1M1/Min - "1"
87	31	91		31	A2J4	6		1M2/Min "2"
88	31	0		32	A2J4	12		1M4/Min "4"
89	31	93		33	A2J4	7		1M8/Min - "8"
90	31	92		34	A2J4	11		10M1/10 Min - "1"
91	31	94		35	A2J4	10		10M2/10Min "2"
92	31	96		36	A2J4	9		10M4/10Min "4"
93	31	95	J2	37	A2J4	8		10M8/10 Min - "8"
94								
95	8	8	J3	1	A2	E30		Set 1
96	8	9		2	A2	E31		Set 2
97	8	0		3	A2	E32		Set 3
98	8	6		4	A2	E26		LT/LPT (Lamp Test)
99	30	6		5	A2J1	14		Cont.
100	8	91	J3	6	A2	E33		MAN

SIZE	CODE IDENT Nº	DWG Nº	REV
A	33783	WL 6025-1004	C

SHEET 5 OF 9

3-Path Programmer Assy (6025-1004) (Sheet 4 of 8) (S/N 400101 and on)

WIRE Nº	ITEM Nº	COLOR	FROM DEVICE	PIN Nº	TO DEVICE	PIN Nº	LENGTH	REMARKS
101	30	7	J3	7	A2J1	4		PROG
102				8				
103	30	92		9	A2J1	11		HPB2 (STOP SW)
104	30	93		10	A2J1	7		SPB1 (START SW)
105				11				
106	30	94		12	A2J1	10		RPB1 (RESET SW)
107				13				
108	30	96		14	A2J1	9		APB1/ADV1
109	30	95		15	A2J1	8		APB2/ADV2
110	30	1		16	A2J1	1		STRL (START LAMP)
111	30	3		17	A2J1	2		STPL (STOP LAMP)
112	30	5		18	A2J1	3		RESL (RESET LAMP)
113	31	6		19	A2J5	14		PSØ (00 Mir)
114	31	5		20	A2J5	3		PS1 (05 min)
115	31	8		21	A2J5	13		PS2 (10 MIN)
116	31	7		22	A2J5	4		PS3 (15 MIN)
117	31	0		23	A2J5	12		PS4 (20 MIN)
118	31	9		24	A2J5	5		PS5 (25 MIN)
119	31	92		25	A2J5	11		PS6 (30 MIN)
120	31	91		26	A2J5	6		PS7 (35 MIN)
121	31	94		27	A2J5	10		PS8 (40 MIN)
122	31	93		28	A2J5	7		PS9 (45 MIN)
123	31	96		29	A2J5	9		PS10 (50 MIN)
124	31	95		30	A2J5	8		PS11 (55 MIN)
125	31	2	J3	31	A2J5	16		Path 1 Retain

SIZE	CODE IDENT Nº	DWG Nº	REV
A	33783	WL 6025-1004	

SHEET 6 OF 9

3-Path Programmer Assy (6025-1004) (Sheet 5 of 8) (S/N 400101 and on)

WIRE Nº	ITEM Nº	COLOR	FROM DEVICE	PIN Nº	TO DEVICE	PIN Nº	LENGTH	REMARKS
126	31	3	J3	32	A2J5	2		Path 2 Retain
127	31	4	J3	33	A2J5	15		Path 3 Retain
128	30	2	J3	34	A2J3	16		DISA/Display CLK 1
129				35				
130				36				
131				37				
132								
133	11	2	A1	E6	A2	E9		+5A
134	11	5	A1	E11	A2	E16		+5B
135	8	902	A1	E12	A2	E12		Path 3 1PPS
136	8	903	A1	E13	A2	E14		Path 2 1 PPS
137	8	904	A1	E14	A2	E13		Path 1 1PPS
138	8	905	A1	E16	A2	E25		Path Strobe enable
139	8	906	A1	E17	A2	E7		Path 3 in PROG
140	8	907	A1	E18	A2	E5		Path 2 In PROG
141	8	908	A1	E19	A2	E6		Path 1 in PROG
142	8	912	A1	E20	A2	E23		SLIP ENABLE "3"
143	8	913	A1	E21	A2	E22		SLIP ENABLE "2"
144	8	914	A1	E22	A2	E24		SLIP ENABLE "1"
145	30	2	A2J1	16	A2	E20		GND
146	9		J4		A1J3			COUNT IN
147	9		J5		A1J1			5 MHz IN
148	31	91	A1J2	6	A2	E21		CLK 3
149	31	93	A1J2	7	A2	E19		CLK 2
150	31	95	A1J2	8	A2	E18		CLK 1

SIZE	CODE IDENT Nº	DWG Nº	REV
A	33783	WL 6025-1004	C

SHEET 7 OF 9

3-Path Programmer Assy (6025-1004) (Sheet 6 of 8) (S/N 400101 and on)

WIRE NO	ITEM NO	COLOR	FROM DEVICE	PIN NO	TO DEVICE	PIN NO	LENGTH	REMARKS
151			TEST POINT WIRING					
152			CASTING					
153			A2 SIDE					
154	30	4	+5 (C)		A2J2	15		+5 (C) UNREG.
155	30	94	TP1			10		STOP SW.
156	30	93	TP2			7		START SW.
157	30	96	TP3			9		RESET SW.
158	30	95	TP4			8		ADV. TIMER
159	30	7	TP5			4		STOP TO SYNTH
160	30	9	TP6			5		START TO SYNTH
161	30	92	TP7			11		RESET TO SYNTH
162	30	5	TP16		A2J2	3		AUTO START TO SYNTH
163								
164			CASTING					
165			A1 SIDE		P.C. BOARD			
166	30	95	+5V (A)		A1J4	8		+5V (A)
167	30	96	+5V (B)		A1J4	9		+5Volts (Standby Battery)
168	31	1	TP6		A1J2	1		100 kHz
169	31	4	TP7		A1J2	15		SLIP COUNT
170	30	1	TP8		A1J4	1		Filter Select 2.-3.0
171	30	2	TP9		A1J4	16		Filter Select 3.0-4.4
172	30	3	TP10		A1J4	2		Filter Select 4.4-6.0
173	30	4	TP11		A1J4	15		Filter Select 6.0-8.4
174	30	5	TP12		A1J4	3		Filter Select 8.4-12
175	30	6	TP13		A1J4	14		Filter Select 12-17

SIZE	CODE IDENT NO	DWG NO	REV
A	33783	WL 6025-1004	C
		SHEET 8 OF 9	

3-Path Programmer Assy (6025-1004) (Sheet 7 of 8) (S/N 400101 and on)

WIRE Nº	ITEM Nº	COLOR	FROM DEVICE	PIN Nº	TO DEVICE	PIN Nº	LENGTH	REMARKS
176	30	8	TP 14		A1J4	13		Filter Select 17-24
177	30	0	TP 15		A1J4	12		Filter Select 24-30

SIZE	CODE IDENT Nº	DWG Nº	REV
A	33783	WL 6025-1004	C

SHEET 9 OF 9

3-Path Programmer Assy (6025-1004) (Sheet 8 of 8) (S/N 400101 and on)

WIRE NO	ITEM NO	COLOR	FROM DEVICE	PIN NO	TO DEVICE	PIN NO	LENGTH	REMARKS
1	6	0	A1	E22	J2	1		GND
2	6	0	A1	E62	J2	2		GND
3	6	2	A1	E26	J2	3		+5A/+5V (AS)
4	6	5	A1	E79	J2	4		+5B
5	6	1	A1	E80	J2	5		+5C
6	6	3	A1	E15	J2	6		+12A/+12V (AS)
7	6	6	A1	E17	J2	7		-12A/-12V (AS)
8	6	3	A1	E19	J2	8		+12B
9	6	6	A1	E16	J2	9		-12B
10	7	90	A1	E21	J2	10		SYNC
11	7	91	A1	E42	J2	11		TV TRIG
12	7	92	A1	E67	J2	12		SA TRIG
13	7	93	A1	E49	J2	13		UFL
14					J2	14		N.U.
15	7	94	A1	E25	J2	15		SSD
16	7	95	A1	E58	J2	16		SPECT IN
17	7	96	A1	E33	J2	17		TVL1
18	7	97	A1	E32	J2	18		TVL2
19	7	98	A1	E31	J2	19		TVL3
20	7	901	A1	E48	J2	20		SET1
21	7	902	A1	E47	J2	21		SET2
22	7	903	A1	E46	J2	22		SET3
23	7	904	A1	E51	J1	1		START
24	7	905	A1	E69	J1	2		LAMP
25	7	906	A1	E63	J2	23		ASA

SIZE	CODE IDENT NO	DWG NO	REV
A	33783	WL 6025-1005	B

SHEET 2 OF 5

Auto Sync/Test Assy (6025-1005) (Sheet 1 of 4)

WIRE Nº	ITEM Nº	COLOR	FROM DEVICE	PIN Nº	TO DEVICE	PIN Nº	LENGTH	REMARKS
26	7	906	A1	E63	J2	24		ASA
27	6	0	A1	E61	J2	25		GND
28	7	907	A1	E66	J2	26		ASD
29	7	907	A1	E66	J2	27		ASD
30	7	908	A1	E73	J2	28		500 Hz
31	7	908	A1	E73	J2	29		500 Hz
32	7	912	A1	E72	J2	30		5 kHz
33	7	912	A1	E72	J2	31		5 kHz
34	7	913	A1	E78	J2	32		LT/LPT
35	7	914	A1	E77	J2	33		SRS
36	7	915	A1	E13	J2	34		OOL
37	7	926	A1	E34	J2	35		ATN1
38	7	927	A1	E35	J2	36		ATN2
39	7	928	A1	E29	J2	37		RAS2
40	7	90	A1	E27	J2	38		RAS3
41	7	91	A1	E24	J2	39		CAL
42								
43	6	7	A1	E75	J1	3		BATT
44	6	3	A1	E20	J1	4		+12C
45	6	3	A1	E18	J1	5		+12D
46	6	2	A1	E82	J1	6		+5D
47	6	2	A1	E83	J1	7		+5E
48	6	2	A1	E85	J1	8		+5F
49	6	8	A1	E14	J1	9		+29
50	7	916	A1	E23	J1	10		TS1

SIZE	CODE IDENT Nº	DWG Nº	REV
A	33783	WL 6025-1005	B

SHEET 2 OF 5

Auto Sync/Test Assy (6025-1005) (Sheet 2 of 4)

WIRE Nº	ITEM Nº	COLOR	FROM DEVICE	PIN Nº	TO DEVICE	PIN Nº	LENGTH	REMARKS
51	7	917	A1	E74	J1	11		TS2
52	7	918	A1	E84	J1	12		BTG
53	7	923	A1	E86	J1	13		BTR
54	7	924	A1	E81	J1	14		CTG
55	7	925	A1	E76	J1	15		CTR
56	7	92	A1	E38	J1	16		10DB
57	7	93	A1	E37	J1	17		20DB
58	7	94	A1	E36	J1	18		30DB
59	7	95	A1	E30	J1	19		TO2
60	7	96	A1	E28	J1	20		TO3
61	7	97	A1	E39	J1	21		TC1
62	7	98	A1	E40	J1	22		TC2
63	7	901	A1	E41	J1	23		TC3
64	8		A1	E50	J3			5 MHz
64A	8	0	A1	E52		shield		GND [1]
65	7	90	A1	E21	A1	E55		SYNC/SA SYNC
66	6	2	A1	E26	A1	E60		+5A/+5V (AS)
67	6	3	A1	E15	A1	E56		+12A/+12V (AS)
68	6	6	A1	E17	A1	E59		-12A/-12V (AS)
69	7	913	A1	E78	A1	E71		LT/LPT/LAMP TEST
70	6	1	A1	E70	A1	E80		+5C
71	7	96	A1	E33	A1	E43		TVL1/MLS1
72	7	97	A1	E32	A1	E44		TVL2/MLS2
73	7	98	A1	E31	A1	E45		TVL3/MLS3
74								

SIZE	CODE IDENT Nº	DWG Nº	REV
A	33783	WL 6025-1005	B

SHEET 4 OF 5

Auto Sync/Test Assy (6025-1005) (Sheet 3 of 4)

WIRE Nº	ITEM Nº	COLOR	FROM DEVICE	PIN Nº	TO DEVICE	PIN Nº	LENGTH	REMARKS
75								
76	7		A1	E26	Casting TP	+5VA		+5VA
77	7		A1	E15	Casting TP	+12V		+12A
78	7		A1	E17	Casting TP	-12V		-12A
79	19		A1	TP1	Casting TP	1		DIGITIZED SPECTRUM
80	19		A1	TP3	Casting TP	3		SLIP RETARD OUT
81	19		A1	TP4	Casting TP	4		SLIP ADVANCE OUT
82	19		A1	TP5	Casting TP	5		5 Hz
83	19		A1	TP9	Casting TP	9		AUTO SYNC SW (LOW)
84	19		A1	TP10	Casting TP	10		AUTO SYNC ENABLE (HIGH)
85	19		A1	TP11	Casting TP	11		S/A BANDWIDTH (HIGH FOR 500 Hz BW)
86	19		A1	TP12	Casting TP	12		UFL (HIGH FOR 2-30 MHz)

SIZE	CODE IDENT Nº	DWG Nº	REV
A	33783	WL 6025-1005	B

SHEET 5 OF 5

Auto Sync/Test Assy (6025-1005) (Sheet 4 of 4)

WIRE Nº	ITEM Nº	COLOR	FROM DEVICE	PIN Nº	TO DEVICE	PIN Nº	LENGTH	REMARKS
1	37	7	J1	5	A2	E15		BATT
2	37	7	J1	6	A2	E15		BATT
3	37	Ø	J1	1	A2	E16		GND
4	37	Ø	J1	2	A2	E13		Std Adjust Gnd
5	37	8	J1	3	A2	E17		+35VC
6	37	8	J1	4	A2	E17		+35VC
7	37	5	J1	7	A2	E12		+5VB
8	37	5	J1	8	A2	E12		+5VB
9	37	5	J1	9	A2	E12		+5VB
10	37	8	FL	2	A2	E12		+5VB
11	37	9	FL	1	A2	E1		
12	36		A1J1		A2J1			
13	38	91	A1J1	3	A2	E14		
14	38	92	A1J1	2	A2	E9		
15	38	93	A1J1	1	A2	E8		
16	38	94	A1J1	4	A2	E10		
17	38	95	J1	10	A2	E6		Std Adjust
18	38	8	J1	11	A2	E17		+29V Test/+35VC
19	37	5	J1	12	A2	E11		+8V
20	38	98	J3		A2	E3		
21	38	901	J5		A2	E5		
22	38	902	J4		A2	E4		
23	38	903	J2		A2	E2		
24	21	—	FL	1	FUSE	—		
25	21	—	FUSE	—	A3	E1		

SIZE	CODE IDENT Nº	DWG Nº	REV
A	33783	WL 6025-1006	J

SHEET 2 OF 3

Frequency Standard Assy (6025-1006) (Sheet 1 of 2) (S/N 400101 and on)

WIRE NO	ITEM NO	COLOR	FROM DEVICE	PIN NO	TO DEVICE	PIN NO	LENGTH	REMARKS
26	37	8	FL	2	A3	E2		+5VB

SIZE	CODE IDENT NO	DWG NO	REV
A	33783	WL 6025-1006	J

SHEET 3 OF 3

Frequency Standard Assy (6025-1006) (Sheet 2 of 2) (S/N 400101 and on)

WIRE Nº	ITEM Nº	COLOR	FROM DEVICE	PIN Nº	TO DEVICE	PIN Nº	LENGTH	REMARKS
1	10	0	J1	1	A2	5	18"	ARC GND
2	10	0	J1	2	A2	1	18"	V GND
3	10	3	J1	3	A2	7	18"	+12V
4	10	3	J1	4	A2	7	18"	+12V
5	10	901	J1	5	A2	6	18"	V DRIVE
6	10	902	J1	6	A2	9	18"	H DRIVE
7	10	903	J1	7	A2	8	18"	VIDEO
8	10	904	J1	8	A2	2	18"	BRIGHT 2
9	10	905	J1	9	A2	3	18"	BRIGHT 3
10	10	906	J1	10	A2	4	18"	BRIGHT 4
11	10	0	A2	5	A2	1		
12	10	0	A2	10	A2	1		
13	8	--	A2 J101	--	L1 P101	--		MATE CONNECTORS
14	1	--	A2 J102	--	A1 P102	--		MATE CONNECTORS
15	7	--	A2 J104	--	T1 P104	--		MATE CONNECTORS
16	7	--	A2 J105	--	T1 P105	--		MATE CONNECTORS
17	1	--	A2 J106	--	A1 P106	--		MATE CONNECTORS
18	1		A1-AQUADAG		A2	1		CONE STATIC GND
19	6		A2J1	--	A1	--		
20	7		T1/CR2	--	A1	--		

SIZE	CODE IDENT Nº	DWG Nº	REV
A	33783	WL 6025-1007	F

SHEET 2 OF 2

CRT Display (6025-1007)

WIRE NO	ITEM NO	COLOR	FROM DEVICE	PIN NO	TO DEVICE	PIN NO	TO	PIN NO	TO	PIN NO	TO	PIN NO	LENGTH	REMARKS
1	19	0	E1		P1	1	P1	2						GND
2		7	E4		P1	3								+35
3	30		P1	3	P1	4	P1	5						JUMPER
4			E2		E3									
5			P1	8	F1									FUSE
6			P1	3	F1									FUSE

SIZE	CODE IDENT NO	DWG NO	REV
A	33783	WL 6025-1008	B

SHEET 2 OF 2

Battery Supply Assy (6025- 1008)

WIRE Nº	ITEM Nº	COLOR	FROM DEVICE	PIN Nº	TO DEVICE	PIN Nº	LENGTH	REMARKS
1	22	2	BRKT 1	E1	BRKT 2	E1		
2	22	2	BRKT 1	E2	BRKT 1	E3		
3	22	2	BRKT 1	E4	BRKT 1	E5		
4	22	2	BRKT 1	E6	A1	E3		
5	22	2	BRKT 2	E2	BRKT 2	E3		
6	22	2	BRKT 2	E4	BRKT 2	E5		
7	22	2	BRKT 2	E6	BRKT 3	E6		
8	22	2	BRKT 3	E5	BRKT 3	E4		
9	22	2	BRKT 3	E3	BRKT 3	E2		
10	22	2	BRKT 3	E1	BRKT 4	E1		
11	22	2	BRKT 4	E2	BRKT 4	E3		
12	22	2	BRKT 4	E4	BRKT 4	E5		
13	22	Ø	BRKT 4	E6	A1	E5		
14	22	Ø	P1	2	A1	E2		
15	22	2	P1	7	A1	E1		
16	22	2	P1	4	A1	E4		
17	23		P1	2	P1	1		
18	23		P1	3	P1	4		
19	23		P1	4	P1	5		

NOTES:

	SIZE	CODE IDENT Nº	DWG Nº	REV
NEXT ASSY:	A	33783	WL 6025-1018	B
	BR COMMUNICATIONS		SHEET 2 OF 2	

Battery Supply (6025-1018)

WIRE Nº	ITEM Nº	COLOR	FROM DEVICE	PIN Nº	TO DEVICE	PIN Nº	LENGTH	REMARKS
1	6	0	A2-GND		P1	1		
2	6	1	+5C		P1	2		
3	6	90	PATH 1		P1	3		
4	6	91	PATH 2		P1	4		
5	6	92	STROBE		P1	5		
6	6	93	10KHz	1	P1	6		FREQ-10KHz
7	6	94	10KHz	2	P1	7		4D1-8
8	6	95	10KHz	4	P1	8		
9	6	96	10KHz	8	P1	9		
10	6	97	100KHz	1	P1	10		100KHz
11	6	98	100KHz	2	P1	11		5D1-8
12	6	901	100KHz	4	P1	12		
13	6	902	100KHz	8	P1	13		
14	6	903	1MHz	1	P1	14		1MHz
15	6	904	1MHz	2	P1	15		6D1-8
16	6	905	1MHz	4	P1	16		
17	6	906	1MHz	8	P1	17		
18	6	907	10MHz	1	P1	18		10MHz
19	6	908	10MHz	2	P1	19		7D1-8
20	6	912	10MHz	4	P1	20		
21	6	913	LT		P1	21		LAMP TEST
22	6	914	1SEC	1	P1	22		TIME-SEC
23	6	915	1SEC	2	P1	23		
24	6	916	1SEC	4	P1	24		

SIZE	CODE IDENT Nº	DWG Nº	REV
A	33783	WL 6025-1009	K

SHEET 2 OF 3

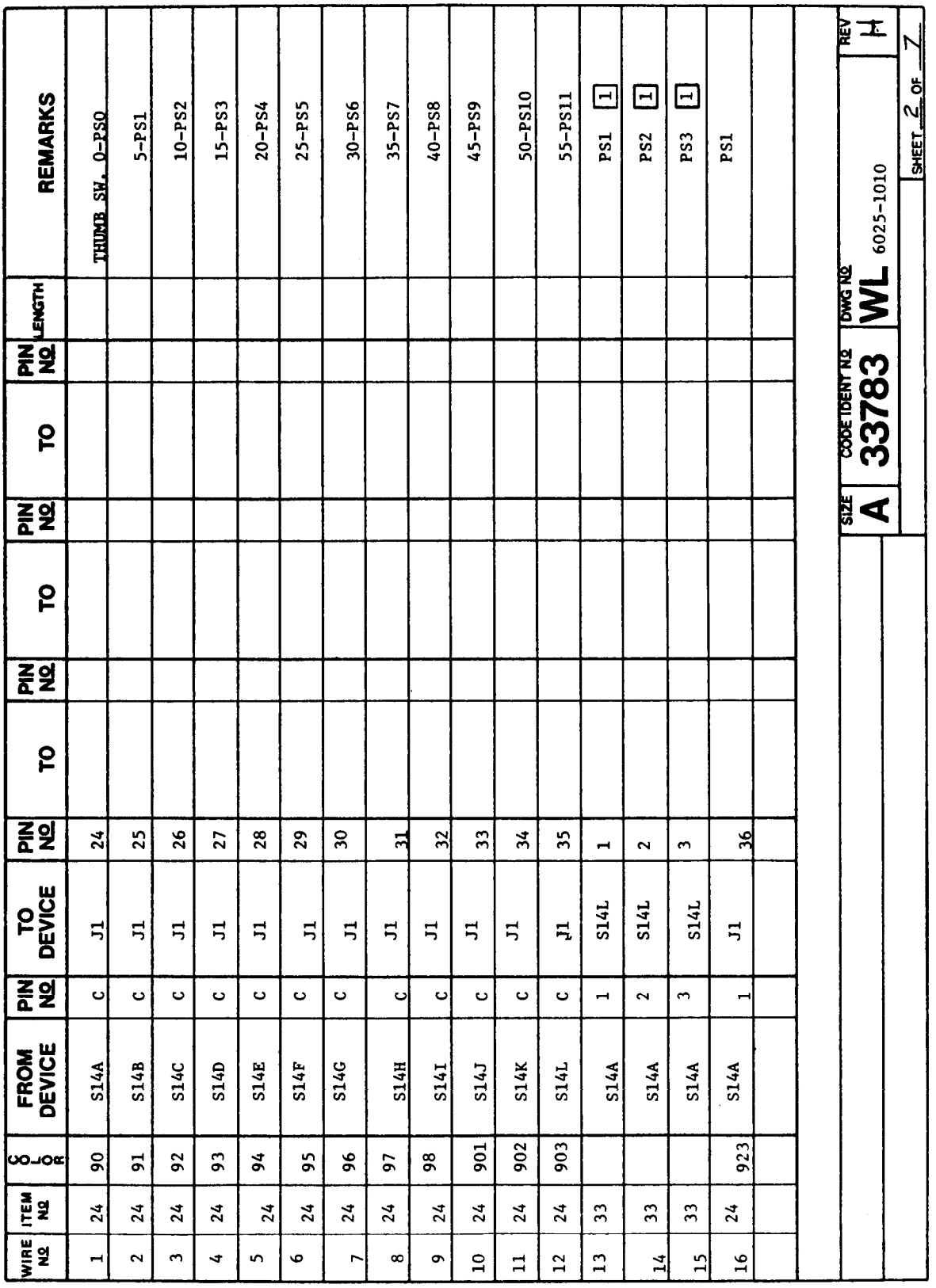
Numeric Display Assy (6025-1009) (Sheet 1 of 2)

WIRE Nº	ITEM Nº	COLOR	FROM DEVICE	PIN Nº	TO DEVICE	PIN Nº	LENGTH	REMARKS
25	6	917	A2 1SEC	8	P1	25		
26	6	918	A2 10SEC	1	P1	26		TIME - 10 SEC
27	6	923	A2 10SEC	2	P1	27		
28	6	924	A2 10SEC	4	P1	28		
29	6	925	A2 10SEC	8	P1	29		
30	6	926	A2 1MIN	1	P1	30		1 MIN
31	6	927	A2 1MIN	2	P1	31		
32	6	928	A2 1MIN	4	P1	32		
33	6	90	A2 1MIN	8	P1	33		
34	6	91	A2 10MIN	1	P1	34		10 MIN
35	6	92	A2 10MIN	2	P1	35		
36	6	93	A2 10MIN	4	P1	36		
37	6	94	A2 10MIN	8	P1	37		
38	9	—	A1 +5		A2 +5 (feed through)			
39	9	—	A1 GND		A2 GND (feed through)			
40	6	0	10MHz	8	GND			
41	9	—	A1 GND	—	A1 E1			

SIZE	CODE IDENT Nº	DWG Nº	REV
A	33783	WL 6025-1009	K

SHEET 3 OF 3

Numeric Display Assy (6025 - 1009) (Sheet 2 of 2)



WIRE NO	ITEM NO	COLOR	FROM DEVICE	PIN NO	TO DEVICE	PIN NO	TO	PIN NO	TO	PIN NO	LENGTH	REMARKS
1	24	90	S14A	C	J1	24						THUMB SW. 0-PS0
2	24	91	S14B	C	J1	25						5-PS1
3	24	92	S14C	C	J1	26						10-PS2
4	24	93	S14D	C	J1	27						15-PS3
5	24	94	S14E	C	J1	28						20-PS4
6	24	95	S14F	C	J1	29						25-PS5
7	24	96	S14G	C	J1	30						30-PS6
8	24	97	S14H	C	J1	31						35-PS7
9	24	98	S14I	C	J1	32						40-PS8
10	24	901	S14J	C	J1	33						45-PS9
11	24	902	S14K	C	J1	34						50-PS10
12	24	903	S14L	C	J1	35						55-PS11
13	33		S14A	1	S14L	1						PS1 [1]
14	33		S14A	2	S14L	2						PS2 [1]
15	33		S14A	3	S14L	3						PS3 [1]
16	24	923	S14A	1	J1	36						PS1

SIZE A | CODE IDENT NO 33783 | DWG NO WL 6025-1010 | REV H | SHEET 2 OF 7

Subpanel Controls Assy (6025-1010) (Sheet 1 of 6)

WIRE NO	ITEM NO	COLOR	FROM DEVICE	PIN NO	TO DEVICE	PIN NO	TO	PIN NO	TO	PIN NO	TO	PIN NO	LENGTH	REMARKS
17	24	924	S14A	2	J1	37								PS2
18	24	925	S14A	3	J1	38								PS3
19	24	0	E3		J2	1								GND IN
20	24	0	E1		S1	1	S4	2						GND TO SW
21	24	0	E3		S2	1	S3	1						COMMON
22	24	0	E3		S5	2	S5	3						
23	24	0	E1		S6	C								
24	24	0	E2		S8	C								
25	24	0	E2		S9	2								
26	24	0	E3		S10	C								
27	24	0	E3		S11	2	S11	3						
28	24	0	E2		S12	2	S12	3						
29	24	0	E2		S13	2	S13	3						COMMON
30	24	0	J2	12	R1	1								STD ADJUST GND
31	24	904	S10	3	J1	1								SET 1
32	24	905	S10	4	J1	2								SET 2
32a	24	0	E1		E2		E3							

SIZE	CODE IDENT NO	DWG NO	REV
A	33783	WL 6025-1010	

SHEET 3 OF 7

Subpanel Controls Assy (6025-1010) (Sheet 2 of 6)

WIRE NO	ITEM NO	COLOR	FROM DEVICE	PIN NO	TO DEVICE	PIN NO	TO	PIN NO	TO	PIN NO	TO	PIN NO	LENGTH	REMARKS
33	24	906	S10	5	J1	3								SET 3
34	24	907	S10	1	J1	4								CONT.
35	24	908	S10	2	J1	5								MANUAL
36	24	912	S10	6	J1	6								PROGRAM
37	24	913	S2	2	J1	7								LT
38	24	914	S12	6	J1	8								HPB1/STOP N/C
39	24	915	S12	5	J1	9								HPB2 N/O
40	24	916	S11	5	J1	10								SPB1/START N/O
41	24	917	S11	6	J1	11								SPB2 N/C
42	24	918	S13	5	J1	12								RPB1/RESET N/O
43	24	923	S13	6	J1	13								RPB2 N/C
44	24	924	S1	3	J1	14								ADV1 N/C
45	24	925	S1	2	J1	15								ADV1 N/O
46	24	926	S11	1	J1	16								START LAMP-STRL
47	24	927	S12	1	J1	17								STOP LAMP-STPL
48	24	928	S13	1	J1	18								RESET LAMP-RESL

SIZE	CODE IDENT NO	DWG NO	REV
A	33783	WL 6025-1010	H5

SHEET 4 OF 7

Subpanel Controls Assy (6025-1010) (Sheet 3 of 6)

WIRE NO	ITEM NO	COLOR	FROM DEVICE	PIN NO	TO DEVICE	PIN NO	TO	PIN NO	TO	PIN NO	TO	PIN NO	LENGTH	REMARKS
49	24	90	S9	1	J1	19								DELETE
50	24	91	S9	3	J1	20								ADD
51	24	92	S8	3	J1	21								SLIP RATE-FAST
52	24	93	S8	2	J1	22								SLIP RATE-MEDIUM
53	24	94	S8	1	J1	23								SLIP RATE-SLOW
54	24	95	S3	2	J1	39								DIS A
55	24	96	S15	1	J1	40								BATTERY (AUTO SYNC) [3]
56	24	97	S5	5	J1	41								AUTO SW. - N/O
57	24	98	S5	1	J1	42								AUTO LAMP
58	24	901	S6	2	J1	43								10 dB
59	24	902	S6	3	J1	44								20 dB
60	24	903	S6	4	J1	45								30 dB
61	33		S7A	2	S7C	2								[2] TO 2
62	33		S7A	3	S7C	3								[2] TO 3
63	24	904	S7A	2	J1	46								TO 2 ANT SEL
64	24	905	S7A	3	J1	47								TO 3

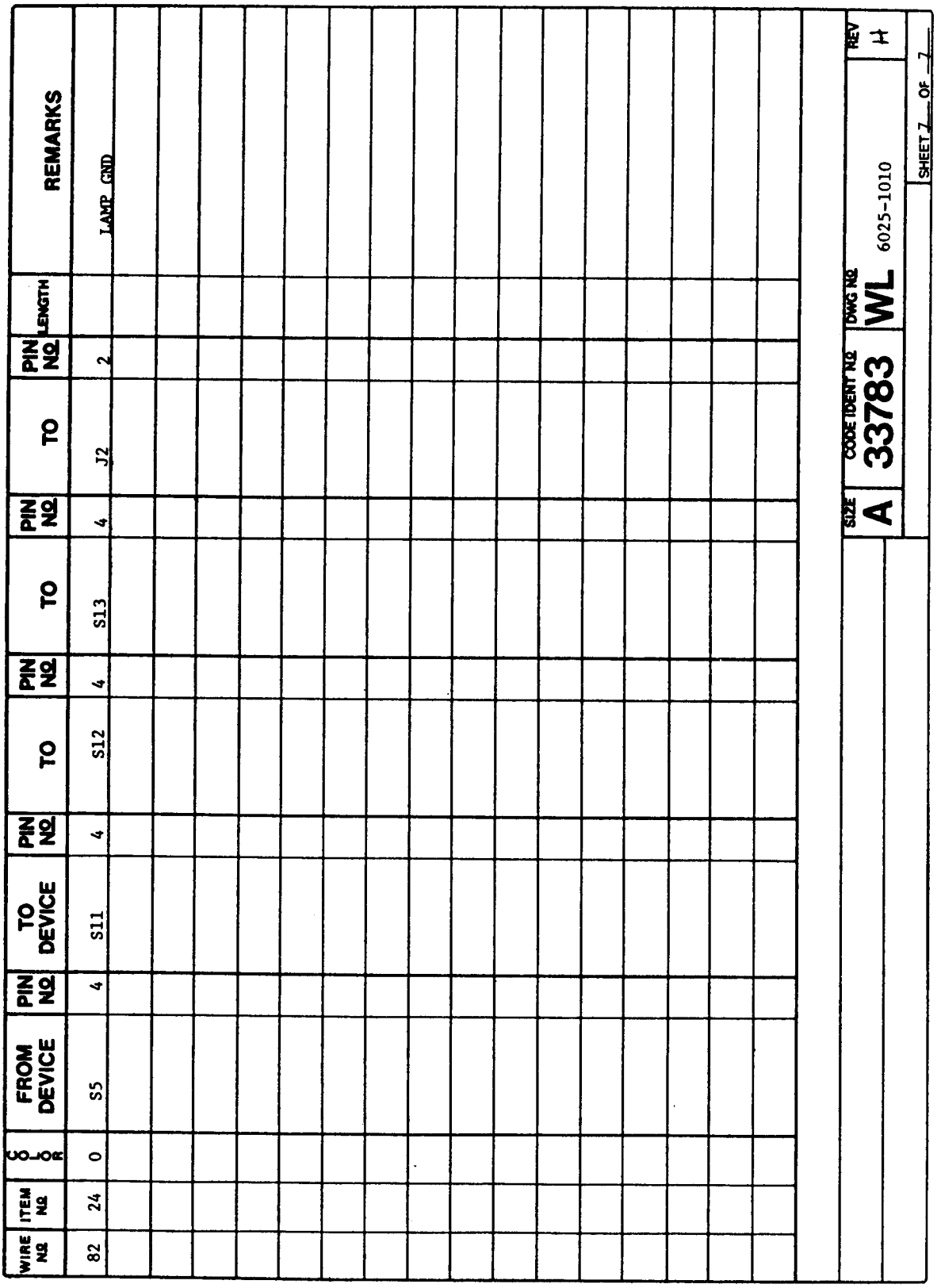
SIZE	CODE IDENT NO	DWG NO	REV
A	33783	WL 6025-1010	H

SHEET 5 OF 7

WIRE NO	ITEM NO	COLOR	FROM DEVICE	PIN NO	TO DEVICE	PIN NO	TO	PIN NO	TO	PIN NO	TO	PIN NO	LENGTH	REMARKS
65	24	906	57A	C	J1	48								TC1
66	24	907	57B	C	J1	49								TC2
67	24	908	57C	C	J1	50								TC3
68	24	912	S4	3	J1	51								UFL - A.S.
69	24	912	S4	3	J1	52								UFL - TIMING
70	24	912	S4	3	J1	53								UFL - SYNTH
71														
72														
73	24	5	R1	3	J2	3								+5B TO STD. ADJ.
74	24	913	R1	2	J2	4								EFC TO FREQ.
75	24	914	R2	1	J2	5								CRT ADJ.
76	24	915	R2	2	J2	6								CRT ADJ.
77	24	916	R2	3	J2	7								CRT ADJ.
78	24	97	S15	2	J2	8								BATTERY IN
79	24	97	S15	2	J2	9								BATTERY IN
80	24	7	S15	1	J2	10								BATTERY OUT
81	24	7	S15	1	J2	11								BATTERY OUT

SIZE	CODE IDENT NO	DWG NO	REV
A	33783	WL 6025-1010	M

SHEET 6 OF 7



Subpanel Controls Assy (6025-1010) (Sheet 6 of 6)

WIRE Nº	ITEM Nº	COLOR	FROM DEVICE	PIN Nº	TO DEVICE	PIN Nº	LENGTH	REMARKS
1	53	Ø	P15	1	S1	1		GND
2	53	5	P15	2	S9	5		+5VB TO TEST SW.
3	54	90	P15	3	S1	3		PD1 N/O
4	54	91	P15	4	S2	3		PD2 N/O
5	54	92	P15	5	S3	3		PD3 N/O
6	54	93	P15	6	S8	2		LC1 N/C
7	54	94	P15	7	S8	3		LC2 N/O
8	54	95	P15	8	S7	2		RS1 N/C
9	54	96	P15	9	S7	3		RS2 N/O
10	54	97	P15	10	S6	2		LS1 N/C
11	54	98	P15	11	S6	3		LS2 N/O
12	54	901	P15	12	S5	2		EARSE ECL N/C
13	54	902	P15	13	S4	3		AUTO AC1
14	54	903	P15	14	S4	8		AUTO LAMP
15	54	904	P15	15	S1	8		PATH 1 LAMP
16	54	905	P15	16	S2	8		PATH 2 LAMP
17	54	906	P15	17	S3	8		PATH 3 LAMP
18	54	907	P15	18	S9	3		TEST SW 1
19	54	908	P15	19	S9	2		TEST SW 2
20	54	912	P15	20	XDS2	1		BATT GREEN
21	54	913	P15	21	XDS4	1		BATT RED
22	54	914	P15	22	XDS1	1		REC GREEN
23	54	915	P15	23	XDS3	1		REC RED
24	54	916	P15	25	S10	2		CURS/FREQ SW
25	53	Ø	P15	26	S9	4		GND

SIZE	CODE IDENT Nº	DWG Nº	REV
A	33783	WL 6025-1013	A

SHEET 2 OF 3

Front Panel Assy (6025-1013) (Sheet 1 of 2)

WIRE NO	ITEM NO	COLOR	FROM DEVICE	PIN NO	TO DEVICE	PIN NO	LENGTH	REMARKS
26	52	-	S1	1	S1	9		GND
26	52		S1	9	S2	1		GND
26	52		S2	1	S2	9		GND
26	52		S2	9	S3	1		GND
26	52		S3	1	S3	9		GND
26	52		S3	9	S4	1		GND
26	52		S4	1	S4	9		GND
26	52		S4	9	S5	1		GND
26	52		S5	1	S6	1		GND
26	52		S6	1	S7	1		GND
26	52		S7	1	S8	1		GND
26	52		S8	1	S10	1		GND
27	52		S9	4	S9	6		GND
28	52		S9	2	S9	1		
39	52		S9	6	XDS1	E3		GND
30	52		XDS1	E3	XDS2	E4		GND
30	52		XDS2	E4	XDS3	E5		GND
30	52		XDS3	E5	XDS4	E6		GND

SIZE	CODE IDENT NO	DWG NO	REV
A	33783	WL 6025-1013	A

SHEET 3 OF 3

Front Panel Assy (6025-1013) (Sheet 2 of 2)

WIRE NO	ITEM NO	COLOR	FROM DEVICE	PIN NO	TO DEVICE	PIN NO	LENGTH	REMARKS
1	60	-	XU1	C	XU2	C		GND
1	60	-	XU2	C	XU3	C		GND
2	62	0	XU3	C	E1			GND
3	60	-	XU4	C	XU5	C		GND
3	60	-	XU5	C	XU6	C		GND
4	62	0	XU4	C	E1			GND
5	60	-	XU7	C	XU8	C		GND
5	60	-	XU8	C	XU9	C		GND
6	62	0	XU9	C	E1			GND
7	60	-	XU10	C	XU11	B		GND
7	60	-	XU11	B	XU12	B		GND
8	62	0	XU10	C	E1			GND
9	62	209	J1	A	XU1	B		+11VC (unreg)
-	10	-	XU1	B	C1	+		+11VC (unreg)
-	10	-	XU1	C	C1	-		+11VC (unreg)
10	62	209	J1	B	XU2	B		+11VC (unreg)
-	10	-	XU2	B	C2	+		+11VC (unreg)
-	10	-	XU2	C	C2	-		+11VC (unreg)
11	62	209	J1	C	XU3	B		+11VC (unreg)
-	10	-	XU3	B	C3	+		+11VC (unreg)
-	10	-	XU3	C	C3	-		+11VC (unreg)
12	62	209	J1	D	XU4	B		+11VC (unreg)
13	62	209	XU4	B	XU5	B		+11VC (unreg)
	10	-	XU4	B	C4	+		+11VC (unreg)
-	10	-	XU4	C	C4	-		+11VC (unreg)

SIZE	CODE IDENT NO	DWG NO	REV
A	33783	WL 6025-1014	B

SHEET 2 OF 14

Rear Panel Assy (6025-1014) (Sheet 1 of 13)

WIRE Nº	ITEM Nº	COLOR	FROM DEVICE	PIN Nº	TO DEVICE	PIN Nº	LENGTH	REMARKS
-	10	-	XU5	B	C5	+		+11VC (unreg)
-	10	-	XU5	C	C5	-		+11VC (unreg)
14	62	31	J1	R	XU6	B		+20VC (unreg)
-	10	-	XU6	B	C6	+		+20VC (unreg)
	10		XU6	C	C6	-		+20VC (unreg)
15	62	31	J1	S	XU7	B		+20VC (unreg)
16	62	31	XU7	B	XU8	B		+20VC (unreg)
-	10	-	XU7	B	C7	+		+20VC (unreg)
-	10	-	XU7	C	C7	-		+20VC (unreg)
-	10	-	XU8	B	C8	+		+20VC (unreg)
-	10	-	XU8	C	C8	-		+20VC (unreg)
17	62	31	J1	T	XU9	B		+20VC (unreg)
18	62	31	XU9	B	XU10	B		+20VC (unreg)
-	10	-	XU9	B	C9	+		+20VC (unreg)
-	10	-	XU9	C	C9	-		+20VC (unreg)
-	10	-	XU10	B	C10	+		+20VC (unreg)
-	10	-	XU10	C	C10	-		+20VC (unreg)
19	62	609	J1	U	XU11	C		-20VC (unreg)
-	11	-	XU11	C	C11	-		-20VC (unreg)
-	11	-	XU11	B	C11	+		-20VC (unreg)
20	62	609	J1	V	XU12	C		-20VC (unreg)
	11		XU12	C	C12	-		-20VC (unreg)
	11		XU12	B	C12	+		-20VC (unreg)
	11		XU11	E	C14	-		-20VC (unreg)
	11		XU11	B	C14	+		-20VC (unreg)

SIZE	CODE IDENT Nº	DWG Nº	REV
A	33783	WL 6025-1014	B

SHEET 3 OF 14

Rear Panel Assy (6025-1014) (Sheet 2 of 13)

WIRE NO	ITEM NO	COLOR	FROM DEVICE	PIN NO	TO DEVICE	PIN NO	LENGTH	REMARKS
–	11	–	XU12	E	C15	–		-20VC (unreg)
–	11	–	XU12	B	C15	+		-20VC (unreg)
21	62	0	J1	P	E1			GND
22	62	0	J1	Q	E1			GND
–	14	–	TB1	1	TB1	9		R2 between TB1-1 & TB1-9
–	14	–	TB1	2	TB1	10		R1 between TB1-2 & TB1-10
–	12		TB1	2	C13	+		+5VC (unreg)
–	12		TB1	9	C13	–		-12VC (unreg)
23	62	1	J1	G	TB1	10		+5VC (unreg)
24	62	609	J1	U	TB1	1		-20VC (unreg)
25	55	2	B1	+	TB1	2		+5VC (unreg)
26	55	6	B1	–	TB1	9		-20VC (unreg)
27	65	90	J2	1	P2	10		SRS
28	65	90	J2	2	P8	33		SRS
29	65	90	J2	3	P4	52		SRS
30	65	91	J2	4	P2	35		AGC
31	65	92	J2	5	P8	24		[1] ASA
32	65	0	J2	6	P8	25		[1] GND
33	65	93	J2	7	P8	26		[1] ASD
34	65	94	J2	8	P8	29		500 Hz BW
35	65	95	J2	9	P8	31		5 kHz BW
36	65	96	J2	10	P8	35		ATN 1
37	65	97	J2	11	P8	36		ATN 2
38	65	98	J2	12	P8	37		RAS 2
39	65	901	J2	13	P8	38		RAS 3

SIZE	CODE IDENT NO	DWG NO	REV
A	33783	WL 6025-1014	B

SHEET 4 OF 14

Rear Panel Assy (6025-1014) (Sheet 3 of 13)

WIRE Nº	ITEM Nº	COLOR	FROM DEVICE	PIN Nº	TO DEVICE	PIN Nº	LENGTH	REMARKS
37	65	902	J2	14	P8	39		CAL
38	65	903	J2	15	P4	24		DEL
39	65	904	J2	16	P4	26		ADD
40	65	905	J2	17	P4	28		SLF
41	65	906	J2	18	P4	29		SLM
42	65	907	J2	19	P4	30		SLS
43	65	908	J2	20	P4	31		STP
44	65	912	J2	21	P4	32		STR
45	65	913	J2	22	P4	33		RES
46	65	914	J2	23	P4	34		SSDA
47	65	915	J2	24	P4	35		AST
48	65	916	J2	25	P4	36		PRE1
49	65	917	J2	26	P4	37		PRE2
50	65	918	J2	27	P4	38		PRE3
51	65	923	J2	28	P4	39		PRE4
52	65	924	J2	29	P4	40		PRE5
53	65	925	J2	30	P4	41		PRE6
54	65	926	J2	31	P4	42		PRE7
55	65	927	J2	32	P4	43		PRE8
56	65	928	J2	33	P4	44		EOS
57	65	90	J2	34	P8	34		OOL
58	65	92	J2	35	P1	15		[2] Analog Signal
59	65	0	J2	36	P1	16		[2] GND
60	65	93	J2	37	P11	53		UFL
61	67	-	J3	-	P13	-		5 MHz

SIZE	CODE IDENT Nº	DWG Nº	REV
A	33783	WL 6025-1014	B

SHEET 5 OF 14

Rear Panel Assy (6025-1014) (Sheet 4 of 13)

WIRE Nº	ITEM Nº	COLOR	FROM DEVICE	PIN Nº	TO DEVICE	PIN Nº	LENGTH	REMARKS
62	65	90	J5	—	P4	51		1PPS
63	67	—	J4	—	P12	—		RF FROM 4028
64	64	0	J7	1	E1	—		GND
65	65	91	J7	2	P2	49		SA SYNC
66	65	905	J7	3	P2	50		SPEC
67	65	98	J7	4	P2	51		SAM/MTA-2
68	65	90	J7	5	P2	52		SRS
69	65	923	J7	6	P2	53		AGC
70	65	94	J7	7	P2	55		UFL
71	65	91	J7	8	P4	7		TVL1/PIP1/MLS1
72	65	92	J7	9	P4	8		TVL2/PIP2/MLS2
73	65	93	J7	10	P4	9		TVL3/PIP3/MLS3
		—	J7	11				
		—	J7	12				
74	65	90	P1	10	P8	10		SA SYNC
75	65	90	P1	11	P2	11		SA SYNC
76	65	90	P2	12	P8	11		SA TRIG
77	65	91	P1	12	P8	12		TRIG
78	65	92	P1	13	P2	13		1.5 k
79	65	93	P11	51	P8	13		UFL
80	65	93	P11	52	P2	14		UFL
81	65	94	P3	10	J6	3		PD1
82	65	95	P3	11	J6	4		PD2
83	65	96	P3	12	J6	5		PD3
84	65	97	P3	13	P2	15		PDC1

SIZE	CODE IDENT Nº	DWG Nº	REV
A	33783	WL 6025-1014	B

SHEET 6 OF 14

Rear Panel Assy (6025-1014) (Sheet 5 of 13)

WIRE Nº	ITEM Nº	COLOR	FROM DEVICE	PIN Nº	TO DEVICE	PIN Nº	LENGTH	REMARKS
85	65	98	P3	14	P2	16		PDC2
86	65	901	P3	15	P2	17		THS
87	65	902	P1	14	P2	18		SAM
88	65	903	P3	16	P2	19		SRE
89	65	904	P3	17	P2	20		SRO
90	65	905	P3	18	P2	21		SLB
91	65	906	P3	19	P2	22		SSD
92	65	907	P8	15	P2	23		SSD
93	65	908	P1	17	P2	24		SPEC
94	65	908	P1	18	P8	16		SPEC
95	65	912	P3	20	P2	25		VS1
96	65	913	P14	5	P2	26		VERT TO TV
97	65	914	P3	21	P2	27		01A
98	65	915	P3	22	P2	28		02A
99	65	916	P3	23	P2	29		CSA1
100	65	917	P3	24	P2	30		CSB1
101	65	918	P3	25	P2	31		CSC1
102	65	923	P3	26	P2	32		CSD1
103	65	924	P14	6	P2	33		HORIZ TO TV
104	65	925	P3	27	P2	34		EQT
105	65	926	P3	28	P2	36		PNG
106	65	927	P3	29	P2	37		FMK
107	65	928	P3	30	P2	38		SNG
108	65	90	P3	31	J6	6		LC1
109	65	91	P3	32	J6	7		LC2

SIZE	CODE IDENT Nº	DWG Nº	REV
A	33783	WL 6025-1014	B

SHEET 7 OF 14

Rear Panel Assy (6025-1014) (Sheet 6 of 13)

WIRE NO	ITEM NO	COLOR	FROM DEVICE	PIN NO	TO DEVICE	PIN NO	LENGTH	REMARKS
110	65	92	P3	33	P2	39		CLD
111	65	93	P3	34	P2	40		UCS
112	65	94	P3	35	P2	41		DCS
113	65	95	P3	36	J6	8		RS1 N/C
113A	65	96	P3	37	J6	9		RS2 N/O
113B	65	97	P3	38	J6	10		LS1 N/C
114	65	98	P3	39	J6	11		LS2 N/O
115	65	901	P3	40	P14	7		PVD
116	65	902	P2	42	P4	11		CCC
117	65	903	P2	43	P4	12		CCK
118	65	904	P2	44	P4	13		CUL
119	65	905	P2	45	P3	41		SAC
120	65	906	P2	46	J6	12		ERASE
121	65	907	P3	42	J6	13		AC1
122	65	908	P3	43	J6	14		AC2
123	65	912	P3	44	J6	15		PDL1
124	65	913	P3	45	J6	16		PDL2
125	65	914	P3	46	J6	17		PDL3
126	65	916	P3	51	P2	47		01B
127	65	917	P3	52	P2	48		02B
128	65	918	P3	48	P4	14		TVL1/PIP1/MLS1
129	65	918	P4	15	P8	17		TVL1/PIP1/MLS1
130	65	923	P3	49	P4	16		TVL2/PIP2/MLS2
131	65	923	P4	17	P8	18		TVL2/PIP2/MLS2
132	65	924	P3	50	P4	18		TVL3/PIP3/MLS3

SIZE	CODE IDENT NO	DWG NO	REV
A	33783	WL 6025-1014	B

SHEET 8 OF 14

Rear Panel Assy (6025-1014) (Sheet 7 of 13)

WIRE Nº	ITEM Nº	COLOR	FROM DEVICE	PIN Nº	TO DEVICE	PIN Nº	LENGTH	REMARKS
133	65	924	P4	19	P8	19		TVL3/PIP3/MLS3
134	65	925	P11	1	P6	1		SET 1
135	65	925	P4	48	P8	20		SET 1
136	65	926	P11	2	P6	2		SET 2
137	65	926	P4	49	P8	21		SET 2
138	65	927	P11	3	P6	3		SET 3
139	65	927	P4	50	P8	22		SET 3
140	65	928	P7	1	P11	41		START AUTO SYNC
141	65	90	P7	2	P11	42		LAMP AUTO SYNC
142	65	91	P4	20	P8	23		ASA
143	65	92	P4	21	P8	27		ASD
144	65	93	P1	19	P8	28		500 Hz
145	65	94	P1	20	P8	30		5 kHz
146	65	95	P3	47	P4	22		LT
147	65	95	P4	23	P8	32		LT
148	65	7	P7	3	P11	40		BATT
149	65	97	P7	10	J6	18		TEST SW N/C
150	65	98	P7	11	J6	19		TEST SW N/O
151	65	901	P7	12	J6	20		BTG
152	65	902	P7	13	J6	21		BTR
153	65	903	P7	14	J6	22		CTG
154	65	904	P7	15	J6	23		CTR
155	65	905	P7	16	P11	43		10 dB
156	65	906	P7	17	P11	44		20 dB
157	65	907	P7	18	P11	45		30 dB

SIZE	CODE IDENT Nº	DWG Nº	REV
A	33783	WL 6025-1014	B

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Rear Panel Assy (6025-1014) (Sheet 8 of 13)

WIRE NO	ITEM NO	COLOR	FROM DEVICE	PIN NO	TO DEVICE	PIN NO	LENGTH	REMARKS
158	65	908	P7	19	P11	46		TO2
159	65	912	P7	20	P11	47		TO3
160	65	913	P7	21	P11	48		TC1
161	65	914	P7	22	P11	49		TC2
162	65	915	P7	23	P11	50		TC3
163	65	916	P11	19	P4	25		DEL
164	65	917	P11	20	P4	27		ADD
165	65	918	P11	21	P4	45		SLF
166	65	923	P11	22	P4	46		SLM
167	65	924	P11	23	P4	47		SLS
168	65	925	P11	4	P6	5		CONT
169	65	926	P11	5	P6	6		MAN
170	65	927	P11	6	P6	7		PROG
171	65	95	P11	7	P6	4		LT
172	65	90	P11	8	P6	8		HPB1 STOP SW
173	65	91	P11	9	P6	9		HPB2 STOP SW
174	65	92	P11	10	P6	10		SPB1 START SW
175	65	93	P11	11	P6	11		SPB2 START SW
176	65	94	P11	12	P6	12		RPB1 RESET SW
177	65	95	P11	13	P6	13		RPB2 RESET SW
178	65	96	P11	14	P6	14		ADV 1/APB1
179	65	97	P11	15	P6	15		ADV 2/APB1
180	65	98	P11	16	P6	16		STRL/START LAMP
181	65	901	P11	17	P6	17		STPL/STOP LAMP
182	65	902	P11	18	P6	18		RESL/RESET LAMP

SIZE	CODE IDENT NO	DWG NO	REV
A	33783	WL 6025-1014	B

SHEET 10 OF 14

Rear Panel Assy (6025-1014) (Sheet 9 of 13)

WIRE Nº	ITEM Nº	COLOR	FROM DEVICE	PIN Nº	TO DEVICE	PIN Nº	LENGTH	REMARKS
183	65	903	P11	24	P6	19		SWØ/TIME
184	65	904	P11	25	P6	20		Ø5 MIN
185	65	905	P11	26	P6	21		10 MIN
186	65	906	P11	27	P6	22		15 MIN
187	65	907	P11	28	P6	23		20 MIN
188	65	908	P11	29	P6	24		25 MIN
189	65	912	P11	30	P6	25		30 MIN
190	65	913	P11	31	P6	26		35 MIN
191	65	914	P11	32	P6	27		40 MIN
192	65	915	P11	33	P6	28		45 MIN
193	65	916	P11	34	P6	29		50 MIN
194	65	917	P11	35	P6	30		55 MIN
195	65	918	P11	36	P6	31		PS 1
196	65	923	P11	37	P6	32		PS 2
197	65	924	P11	38	P6	33		PS 3
198	64	7	P10	8	P20	4		BATT IN
199	64	7	P10	9	P20	5		BATT IN
200	64	7	P10	10	P9	5		BATT OUT
201	64	7	P10	11	P9	6		BATT OUT
202	65	925	P11	39	P6	34		DIS A
203	65	926	P10	5	P14	9		CRT POT CCW
204	65	927	P10	6	P14	10		CRT POT WIPER
205	65	928	P10	7	P14	8		CRT POT CW
206	65	90	P4	10	J6	25		CFS
207	64	5	P4	4	P9	7		+5VB

SIZE	CODE IDENT Nº	DWG Nº	REV
A	33783	WL 6025-1014	B

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Rear Panel Assy (6025-1014) (Sheet 10 of 13)

WIRE Nº	ITEM Nº	COLOR	FROM DEVICE	PIN Nº	TO DEVICE	PIN Nº	LENGTH	REMARKS
208	64	5	P8	4	P9	8		+5VB
209	64	5	J6	2	P9	9		+5VB
210	64	5	P10	3	P9	12		+8V
211	65	92	P10	4	P9	10		EFL TO FRONT PANEL
212	67	–	P16		P17			5 MHz
213	67	–	P18		P19			5 MHz
214	65	95	P7	9	P9	11		+29V TO TEST/+35VC
215	64	1	J1	E	P3	5		+5VC (unreg)
216	64	1	J1	E	P8	5		+5VC (unreg)
217	64	1	J1	F	P4	5		+5VC (unreg)
218	64	1	J1	F	P4	6		+5VC (unreg)
219	64	8	J1	H	P9	3		+35VC (unreg)
220	64	8	J1	J	P9	4		+35VC (unreg)
221	62	0	J1	K	E1			GND
222	62	0	J1	L	E1			GND
223	62	0	J1	M	E1			GND
224	60	–	E1		E2			GND
225	65	96	P3	55	P4	55		MAN
226	65	97	P2	54	P4	54		RESET
227	62	0	J1	N	E2			GND
228	64	0	P1	1	E2			GND
229	64	0	P1	2	E2			GND
230	64	0	P2	1	E2			GND
231	64	0	P2	2	E2			GND
232	64	0	P3	1	E2			GND

SIZE	CODE IDENT Nº	DWG Nº	REV
A	33783	WL 6025-1014	B

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Rear Panel Assy (6025-1014) (Sheet 11 of 13)

WIRE Nº	ITEM Nº	COLOR	FROM DEVICE	PIN Nº	TO DEVICE	PIN Nº	LENGTH	REMARKS
233	64	0	P3	2	E2			GND
234	64	0	P4	1	E2			GND
235	64	0	P4	2	E2			GND
236	64	0	P8	1	E2			GND
237	64	0	P8	2	E2			GND
238	64	0	P9	1	E2			GND
239	64	0	P9	2	P10	12		STD ADJUST GND
240	64	0	P14	1	E2			GND
241	64	0	P14	2	E2			GND
242	64	0	J6	26	E2			GND
243	64	0	P20	1	E2			GND
244	64	0	P20	2	E2			GND
245	64	0	J6	1	E2			GND
246	64	0	P10	1	E2			GND
247	64	0	P10	2	E2			GND
248	64	2	P1	3	XU1	E		+5VD
249	64	2	P7	6	XU1	E		+5VD
250	64	3	P1	6	XU10	E		+12VD
251	64	3	P7	5	XU10	E		+12VD
252	64	6	P1	7	XU11	E		-12VA
253	64	6	P8	7	XU11	E		-12VA
254	64	2	P2	3	XU4	E		+5VE
255	64	2	P7	7	XU4	E		+5VE TO TEST
256	64	3	P2	8	XU9	E		+12VE
257	64	3	P3	6	XU9	E		+12VE

SIZE	CODE IDENT Nº	DWG Nº	REV
A	33783	WL 6025-1014	B

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Rear Panel Assy (6025-1014) (Sheet 12 of 13)

WIRE Nº	ITEM Nº	COLOR	FROM DEVICE	PIN Nº	TO DEVICE	PIN Nº	LENGTH	REMARKS
258	64	6	P2	7	XU12	E		-12VB
259	64	6	P3	7	XU12	E		-12VB
260	64	6	P8	9	XU12	E		-12VB TO TEST
261	64	2	P3	3	XU3	E		+5VF
262	64	2	P7	8	XU3	E		+5VF TO TEST
263	64	3	P3	8	XU7	E		+12VA
264	64	3	P8	6	XU7	E		+12VA TO TEST
265	64	3	P3	9	XU8	E		+12VB
266	64	3	P8	8	XU8	E		+12VB TO TEST
267	64	2	P4	3	XU2	E		+5VG
268	64	2	P8	3	XU5	E		+5VA
269	64	3	P7	4	XU6	E		+12VC
270	64	3	P14	3	XU6	E		+12VC
271	64	3	P14	4	XU6	E		+12VC

SIZE	CODE IDENT Nº	DWG Nº	REV
A	33783	WL 6025-1014	B

SHEET 14 OF 14

Rear Panel Assy (6025-1014) (Sheet 13 of 13)

WIRE Nº	ITEM Nº	COLOR	FROM DEVICE	PIN Nº	TO DEVICE	PIN Nº	LENGTH	REMARKS
1	14		2W1P7		2A1J7			42-70 MHz FROM SYNTH
1	14		2W1P8		2A4J1			42-70 MHz TO FILTER
2	13		2W2P9		2A1J3			CAL FROM SYNTH (2-30 MHz)
2	13		2W2P10		2A1J5			CAL TO RCVR (2-30 MHz)
3	13		2W3P11		2A1J4			2nd LO OUT (40 MHz)
3	13		2W3P12		2A2J3			2nd LO IN (40 MHz)
4	13		2W4P13		2A1J5			5 MHz OUT
4	13		2W4P14		2A2J4			5 MHz IN
5	15		2W5P15		2A2J6			ANT 1 INPUT
5	15		2W5P16		2A3A1J1			ANT 1 INPUT
6	15		2W6P5		2A2J7			ANT 2 INPUT
6	15		2W6P17		2A3A1J2			ANT 2 INPUT
7	15		2W7P6		2A2J8			ANT 3 INPUT
7	15		2W7P18		2A3A1J3			ANT 3 INPUT
8	14		2W8P20		2A2J2			42-70 MHz TO RCVR
8	14		2W8P19		2A4J2			42-70 MHz FROM FILTER
ref			2A3A1P1		2A1J1			CONTROL TO SYNTH
ref			2A3A1P2		2A2J1			CONTROL TO RCVR
ref			2A3A1W1P3		2A1J2			5 MHz IN
ref			2A3A1W2P4		2A1J6			COUNT OUT

SIZE	CODE IDENT Nº	DWG Nº	REV
A	33783	WL 4028-1000 and 4028-1100	A

SHEET 2 OF 2

4028 HF Receiver -- Unit 2 (4028-1000 and 4028-1100)

WIRE Nº	ITEM Nº	COLOR	FROM DEVICE	PIN Nº	TO DEVICE	PIN Nº	LENGTH	REMARKS
1	8	0	J1	1	A1	E74		GNd
2	8	0	J1	2	A2	E29		GNd
3	8	2	J1	3	A2	E20		+5J
4	8	2	J1	4	A2	E21		+5K
5	8	3	J1	6	A2	E22		+12
6	8	6	J1	7	A2	E25		-12
7	8	4	J1	8	A2	E24		+24
8	8	0	J1	9	A2	E30		GNd
9	8	9	J1	10	A1	E75		GNd Hi for RX for TX
10	9	91	J1	11	A1	E66		SLF/Slip Fast
11	9	92	J1	12	A1	E65		SLM/Medium
12	9	93	J1	13	A1	E63		SLS/SLOW
13	9	94	J1	14	A1	E88		SSD/Becomes SSDA
14	9	95	J1	15	A1	F64		DEL/Delite
15	9	96	J1	16	A1	E67		ADD/Add
16	9	98	J1	17	A1	E76		ASD [1] Auto Sync
17	9	0	J1	18	A1	E80		GNd [1] Auto sync
18	9	908	J1	19	A1	E81		ASA [1] Auto Sync
19	9	901	J1	20	A1	E78		Aux Latch In
20	9	903	J1	22	A1	E10		AST/Auto Start
21	9	904	J1	23	A1	E9		STR/Start
22	9	905	J1	24	A1	E8		STP/Stop
23	9	906	J1	25	A1	E7		RES/Reset

SIZE	CODE IDENT Nº	DWG Nº	REV
A	33783	WL 5030-1001	G

SHEET 2 OF 6

Sweep Synthesizer Assy (5030 - 1001) (Sheet 1 of 5)

WIRE NO	ITEM NO	COLOR	FROM DEVICE	PIN NO	TO DEVICE	PIN NO	LENGTH	REMARKS
24	9	907	J1	26	A1	E6		SRS (HI FOR SWEEPING)
25	9	908	J1	27	A1	E84		E.O.S./END OF SWEEP
26	9	912	J1	28	A1	E82		BKI/BLANK IN
27	9	913	J1	29	A1	E91		BKO/BLANK OUT
28	9	914	J1	30	A1	E83		BKC/BLANK CLK
29	9	915	J1	31	A1	E105		GATE IN/END OF SWEEP BLANKING
30	9	916	J1	32	A2	E17		OOL/OUT OF LOCK
31	9	917	J1	33	A1	E6		SRS (HI FOR SWEEPING)
32	9	918	J1	34	A1	E6		SRS (HI FOR SWEEPING)
33	9	923	J1	35	A1	E6		SRS (HI FOR SWEEPING)
34	9	924	J1	36	A1	E103		PAD
35	9	925	J1	37	A1	E90		NEW BLANK (60 KHz B.W.)
36	9	925	A2	E13	A1	E56		SD "1" (TO SYNTH)
37	9	926	A2	E14	A1	E59		SD "2" (TO SYNTH)
38	9	927	A2	E15	A1	E60		SD "4" (TO SYNTH)
39	9	928	A2	E16	A1	E61		SD "8" (TO SYNTH)
40	9	90	A2	E12	A1	E62		CLK (FROM SYNTH)
41	9	91	A2	E3	A1	E38		T1
42	9	92	A2	E4	A1	E37		T2
43	9	93	A2	E5	A1	E36		T3
44	9	94	A2	E6	A1	E35		T4
45	9	95	A2	E7	A1	E87		T5
46	9	96	A2	E8	A1	E39		T6
47	9	97	A2	E9	A1	E85		T7
48	9	98	A2	E10	A1	E86		T8

SIZE	CODE IDENT NO	DWG NO	REV
A	33783	WL 5030-1001	G

SHEET 3 OF 6

Sweep Synthesizer Assy (5030-1001) (Sheet 2 of 5)

WIRE Nº	ITEM Nº	COLOR	FROM DEVICE	PIN Nº	TO DEVICE	PIN Nº	LENGTH	REMARKS
49	9	901	A1	E4	A1	E77		100 - AUX LATCH OUT
50	9	901	A1	E77	A1	E73		30 H - AUX LATCH OUT
51	9		A1	E1	A1	E2		JUMPER
52	9		A1	E2	A1	E72		JUMPER
53	9		A1	E89	A1	E107		JUMPER
54	9		A1	E69	A1	E74		JUMPER
55	13		J2		A1	P101		5MHz IN
56	11		J5		A1	P102		5MHz to REC
57	17		A2	P4	A1	P103		5MHz to SYNTH
58	12		J4		A1	P104		2nd L.O. to REC
59	19		J3		A1	P105		RF to 5018
60	18		A2	P2	A1	P106		42-70 to SYNTH
61	12		J7		A2	P1		1st L.O. to REC
62	20		J6		A2	P3		42-70 to PROG
			TEST POINTS :					
63	24		A2	TP3	+5VJ			
64	24		A2	TP4	+5VK			
65	24		A2	TP5	+12V			
66	24		A2	TP6	-12V			
67	24		A2	TP7	+24V			
68	24		A2	TP1	1			COUNT 42-70
69	24		A2	TP2	2			1st L.O. 42-70
70	24		A2	TP9	9			LOCK
71	24		A1	TP101	101			5MHz IN
72	24		A1	TP102	102			40 MHz OUT

SIZE	CODE IDENT Nº	DWG Nº	REV
A	33783	WL 5030-1001	G

SHEET 4 OF 5

Sweep Synthesizer Assy (5030-1001) (Sheet 3 of 5)

WIRE Nº	ITEM Nº	COLOR	FROM DEVICE	PIN Nº	TO DEVICE	PIN Nº	LENGTH	REMARKS
73	24		A1	TP5	5			SSD
74	24		A1	TP1	1			BKO
75	24		A1	TP6	6			SLF
76	24		A1	TP7	7			SLM
77	24		A1	TP8	8			SLS
78	24		A1	TP9	9			DEL
79	24		A1	TP10	10			ADD
80	24		A1	TP11	11			UPPER LIMIT SELECT
81	24		A1	TP13	13			AST
82	24		A1	TP103	103			2-30 MHz OUT
83	24		A1	TP14	14			STR
84	24		A1	TP15	15			STP
85	24		A1	TP16	16			RES
86	24		A1	TP17	17			SRS
87	24		A1	TP20	20			BKI
88	24		A1	TP21	21			EOS
89	24		A1	TP22	22			TX
90	24		A1	TP104	104			PAD
91	24		A1	TP105	105			GATE
		JUMPERS						
92	9	9	A1	E75	A1	E106		JUMPER
93	9	91	A1	E79	A1	E92		JUMPER
94	8	4	A1	E104	A2	E24		+24V
95	8	2	A1	E14	A2	E21		+5V
96	8	2	A1	E14	A1	E58		+5V

SIZE	CODE IDENT Nº	DWG Nº	REV
A	33783	WL 5030-1001	G

SHEET 5 OF 6

Sweep Synthesizer Assy (5030-1001) (Sheet 4 of 5)

WIRE Nº	ITEM Nº	COLOR	FROM DEVICE	PIN Nº	TO DEVICE	PIN Nº	LENGTH	REMARKS
97	8	3	A2	E22	A2	E23		+12V
98	8	3	A1	E102	A2	E22		+12V
99	8	6	A2	E25	A2	E26		−12V
100	8	2	A1	E58	A1	E101		+5V
101	8	0	CASTING A2 SIDE	GND	A2	E29		GND

SIZE	CODE IDENT Nº	DWG Nº	REV
A	33783	WL 5030-1001	G

SHEET 6 OF 6

Sweep Synthesizer Assy (5030-1001) (Sheet 5 of 5)

WIRE NO	ITEM NO	COLOR	FROM DEVICE	PIN NO	TO DEVICE	PIN NO	TO	PIN NO	TO	PIN NO	TO	PIN NO	LENGTH	REMARKS
1	35	0	J1	1	A1	E23								GND
2	35	0	J1	2	A2	E23								GND
3	34	0	A1	E23	A2	E23								GND
4	35	3	J1	9	A1	E14	A1	E21	A1	E22				+12V CONNECT
5	35	3	J1	5	A2	E1								+12V
6	35	3	J1	6	A2	E18								+12B FOR AUDIO
7	35	6	J1	7	A1	E15	A2	E6						-12
8	35	4	J1	8	A1	E16	A1	E17						+24V CONNECT
9	8	91	J1	10	A1	E1								RAS 2 ANT. SEL.
10	8	92	J1	11	A1	E2								RAS 3
11	8	93	J1	12	A1	E3								CAL
12	8	94	J1	13	A1	E4								ATN 1 10-20-30dB
13	8	95	J1	14	A1	E5								ATN 2
14	8	96	J1	15	A1	E6								PRE 8
15	8	97	J1	16	A1	E7								PRE 7
16	8	98	J1	17	A1	E8								PRE 6

SIZE	CODE IDENT NO	DWG NO	REV
A	33783	WL 4028-1002	E

SHEET 2 OF 5

Receiver Assy (4028-1002) (Sheet 1 of 5)

WIRE NO	ITEM NO	COLOR	FROM DEVICE	PIN NO	TO DEVICE	PIN NO	TO	PIN NO	TO	PIN NO	TO	PIN NO	LENGTH	REMARKS
17	8	901	J1	18	A1	E9								PRE 5
18	8	902	J1	19	A1	E10								PRE 4
19	8	903	J1	20	A1	E11								PRE 3
20	8	904	J1	21	A1	E12								PRE 2
21	8	905	J1	22	A1	E13								PRE 1
22	8	906	J1	23	A2	E2								500 Hz B.W.
23	8	907	J1	24	A2	E5								5 kHz B.W.
24	8	908	J1	25	A2	E9								AUDIO OUT
25	8	912	J1	26	A2	E10								BASEBAND - S/A
26	35	0	J1	27	A2	E21								L/11
27	8	913	J1	28	A2	E12								AGC - BARGRAPH
28	8	914	J1	29	A2	E16								AUDIO POT
29	8	915	J1	30	A2	E17								AUDIO WIPER
30	8	95	A2	E5	A2	E11								CONNECT
31	51		J2		A1	J5								1st LO 42-70 MHz
32	47		J3		A1	J9								2nd LO 40 MHz

SIZE	CODE IDENT NO	DWG NO	REV
A	33783	WL 4028-1002	E

SHEET 2 OF 6

Receiver Assy (4028-1002) (Sheet 2 of 5)

WIRE NO	ITEM NO	COLOR	FROM DEVICE	PIN NO	TO DEVICE	PIN NO	TO	PIN NO	TO	PIN NO	TO	PIN NO	LENGTH	REMARKS
33	15		J4		A2	J8								5 MHz
34	48		J5		A1	J4								CAL 2-30 MHz
35	49		J6		A1	J1								ANT 1 - RF IN
36	50		J7		A1	J2								ANT 2 - RF IN
37	52		J8		A1	J3								ANT 3 - RF IN
38	14		A1	J8	A2	J1								200 kHz IF
39	16		FL1	IN	A1	J6								IN FILTER
40	16		FL1	OUT	A1	J7								OUT
41	9		FL2	IN	A2	J2								IN FILTER 200.25 kHz
42	13		FL2	OUT	A2	J5								OUT FILTER, 200.25 kHz
43	35	3	A2	E1	A2	E7	A2	E8						JUMPER
44	8	916	J1	31	A2	E19								AUX BASEBAND OUT
45	33		A1	TP8	A1 casting tp	+12 VA								
46	33		A1	TP12	A1 casting tp	+12 VB								
47	33		A1	TP13	A1 casting tp	+12 VC								
48	33		A1	TP11	A2 casting tp	+24V								

SIZE	CODE IDENT NO	DWG NO	REV
A	33783	WL 4028-1002	M

SHEET 4 OF 6

Receiver Assy (4028-1002) (Sheet 3 of 5)

WIRE NO	ITEM NO	COLOR	FROM DEVICE	PIN NO	TO DEVICE	PIN NO	TO	PIN NO	TO	PIN NO	TO	PIN NO	LENGTH	REMARKS
49	33		A1	TP10	A2 casting tp	+24 vB								
50	33		A1	TP9	A2 casting tp	−12 V								
51	33													NO CONNECTION
52	33		A1	TP1	A1 casting tp	1								CAL L.O. (-20 dBm)
53	33			TP2		2								CAL ON-OFF
54	33			TP3		3								10 dB ATTN
55	33			TP4		4								20 dB ATTN
56	33			TP5		5								L.O. (-20 dBm)
57	33													
58	33		A1	TP7	A1 casting tp	7								40 MHz L.O.
59	33		A2	TP1	A2 casting tp	1								AUDIO OUT
60	33			TP2		2								BASEBAND OUT
61	33			TP3		3								5 MHz (-26dBm)
62	33			TP4		4								AGC TIME CONSTANT
63	33			TP5		5								AGC OUT
64	33		A2	TP6	A2 casting tp	6								TO GAIN CONTROL

SIZE	CODE IDENT NO	DWG NO	REV
A	33783	WL 4028-1002	E

SHEET 5 OF 6

Receiver Assy (4028-1002) (Sheet 4 of 5)

WIRE NO	ITEM NO	COLOR	FROM DEVICE	PIN NO	TO DEVICE	PIN NO	TO	PIN NO	TO	PIN NO	TO	PIN NO	LENGTH	REMARKS
65	33		A2	TP7	A2 casting tp	7								FROM GAIN CONTROL
66	33		A2	TP11	A2 casting tp	8								NARROW BAND SELECT
67	33		A2	TP9	A2 casting tp	9								WIDE BAND SELECT

SIZE	CODE IDENT NO	DWG NO	REV
A	33783	WL 4028-1002	E

SHEET 6 OF 6

Receiver Assy (4028-1002) (Sheet 5 of 5)

WIRE Nº	ITEM Nº	COLOR	FROM DEVICE	PIN Nº	TO DEVICE	PIN Nº	LENGTH	REMARKS
1	50	92	J11	H	J10	T		AUDIO
2	50	91	J11	J	R3	3		VOL POT-CW
3	50	90	J11	K	R3	2		VOL POT-WIPER
4A	54	9	J11	A	FL1	Line		Line - Hot
4B	54	Ø	J11	B	FL1	Line		Line - Common
---	47	Ø	Shld of 4 at FL1	---	Shld of 42 at FL1	---		Shld Gnd
5	47	1	J11	C	C1	+		+5VC
6	47	609	J11	D	C7	-		-20VC
7	47	31	J11	E	C6	+		+20VC
8	47	209	J11	F	C4	+		+11VC
9	47	8	J11	G	C9	+		+35VC
10	47	Ø	J11	L	E1	---		GND
11	47	Ø	J11	M	E1	---		GND
12	47	Ø	J11	N	E2	---		GND
13	47	209	C4	+	C3	+		+11VC
14	47	209	C3	+	C2	+		+11VC
15	47	31	C6	+	C5	+		+20VC
16	47	31	C5	+	CR3	+		+20VC
17	47	609	C7	-	CR4	-		-20VC
18	47	8	C9	+	C8	+		+35VC
19	47	8	C8	+	CR5	+		+35VC
20	50	1	C1	+	S1 (DS1)	5		+5VC
21	47	Ø	CR1	-	E1	---		GND
22	47	Ø	CR2	-	E1	---		GND

SIZE	CODE IDENT Nº	DWG Nº	REV
A	33783	WL 4028-1003	B

SHEET 2 OF 5

Enclosure Assy (4028- 1003) (Sheet 1 of 4) (S/N 400101 and on)

WIRE Nº	ITEM Nº	COLOR	FROM DEVICE	PIN Nº	TO DEVICE	PIN Nº	LENGTH	REMARKS
23	47	Ø	CR3	-	E1	---		GND
24	47	Ø	CR5	-	E1	---		GND
25	47	Ø	CR4	+	E1	---		GND
26	50	0	S1 (DS1)	6	E1	---		GND
27	47	209	C2	+	CR2	+		+10VC
28	47	Ø	C1	-	E2	---		GND
29	47	Ø	C2	-	C3	-		GND
30	47	Ø	C3	-	C4	-		GND
31	47	Ø	C4	-	E2	---		GND
32	47	Ø	C5	-	C6	-		GND
33	47	Ø	C6	-	E2	---		GND
34	47	Ø	C7	+	E2	---		GND
35	47	Ø	C8	-	C9	-		GND
36	47	Ø	C9	-	E2			GND
37	47	Ø	E1	---	E2	---		GND
38	47	Ø	E1	---	E2	---		GND
39	47	9	TB1	OUT 1	S2	2		115/230V [2]
Jumper	52	---	S2	2	S2	5		115/230V
40	47	91	TB1	OUT 2	S2	8		105/220V [2]
Jumper	52	---	S2	8	S2	11		105/220V
---	16	8	S2	1	T1			230V
Jumper	52	---	S2	1	S2	4		230V
Jumper	52	---	S2	3	S2	6		115V
---	16	9	S2	6	T1			115V
---	16	98	S2	7	T1			220V

SIZE	CODE IDENT Nº	DWG Nº	REV
A	33783	WL 4028-1003	B

SHEET 3 OF 5

Enclosure Assy (4028-1003) (Sheet 2 of 4) (S/N 400101 and on)

WIRE Nº	ITEM Nº	COLOR	FROM DEVICE	PIN Nº	TO DEVICE	PIN Nº	LENGTH	REMARKS
Jumper	52	---	S2	7	S2	10		220V
41	16	90	S2	9	T1			105V
Jumper	52	---	S2	9	S2	12		105V
42A	54	9	FL1	load	S1	1		Line - Hot
42B	54	Ø	FL1	load	S1	2		Line - Common
---	47	Ø	Shld of 42 at FL1		FL1	GND		Shld Gnd
43A	54	9	S1	3	TB1	IN 1		Line - Hot [2]
43B	54	Ø	S1	4	TB1	IN 3		Line - Common [2]
---	47	Ø	Shld of 43 at TB1		FL1	GND		Shld Gnd
---	16	Ø	TB1	OUT 3	T1			Xfmr- Common [2]
---	16	5	T1	5	E1	---		Xfmr - Ground
44	47	1	C1	+	CR1	+		+5VC
45	16	1	T1		CR1			+5VC
46	16	1	T1		CR1			+5VC
47	16	2	T1		CR2			+10VC
48	16	2	T1		CR2			+10VC
49	16	4	T1		CR3			+20VC
50	16	4	T1		CR3			+20VC
51	16	7	T1		CR4			-20VC
52	16	7	T1		CR4			-20VC
53	16	6	T1		CR5			+35VC
54	16	6	T1		CR5			+35VC
55	48	2	U9	+	CR2	+	24	+11VC [3]
56	48	Ø	U9	-	CR2	-	24	GND [3]
57	23	-	J10	T	J10	S		R4 Across T and S

SIZE	CODE IDENT Nº	DWG Nº	REV
A	33783	WL 4028-1003	B

SHEET 4 OF 5

Enclosure Assy (4028-1003) (Sheet 3 of 4) (S/N 400101 and on)

WIRE Nº	ITEM Nº	COLOR	FROM DEVICE	PIN Nº	TO DEVICE	PIN Nº	LENGTH	REMARKS
58	50	92	J10	N	LS1	2		Audio - NC
59	50	Ø	J10	S	LS1	1		Audio Gnd
60	50	Ø	LS1	1	E2	-		Audio Gnd
61	50	Ø	R3	1	E2	-		Vol Pot Gnd

SIZE	CODE IDENT Nº	DWG Nº	REV
A	33783	WL 4028-1003	B

SHEET 5 OF 5

Enclosure Assy (4028-1003) (Sheet 4 of 4) (S/N 400101 and on)

WIRE NO	ITEM NO	COLOR	FROM DEVICE	PIN NO	TO DEVICE	PIN NO	LENGTH	REMARKS
	23		XU1	B	C13	+		
	23		XU1	C	C13	-		
	23		XU1	E	C14	+		
	23		XU1	C	C14	-		
	23		XU2	B	C15	+		
	23		XU2	C	C15	-		
	23		XU2	E	C16	+		
	23		XU2	C	C16	-		
	23		XU3	B	C17	+		
	23		XU3	C	C17	-		
	23		XU3	E	C18	+		
	23		XU3	C	C18	-		
	23		XU4	B	C19	+		
	23		XU4	C	C19	-		
	23		XU4	E	C20	+		
	23		XU4	C	C20	-		
	23		XU5	B	C21	+		
	23		XU5	C	C21	-		
	23		XU5	E	C22	+		
	23		XU5	C	C22	-		
	22		XU6	B	C11	+		
	22		XU6	C	C11	-		
	22		XU6	E	C12	-		
	22		XU6	B	C12	+		
	24		XU7	B	C23	+		

SIZE	CODE IDENT NO	DWG NO	REV
A	33783	WL 4028-1004	D

SHEET 2 OF 7

Rear Panel Assy (4028-1004) (Sheet 1 of 6) (S/N 400101 and on)

WIRE Nº	ITEM Nº	COLOR	FROM DEVICE	PIN Nº	TO DEVICE	PIN Nº	LENGTH	REMARKS
	24		XU7	C	C23	-		
	23		XU7	E	C24	+		
	23		XU7	C	C24	-		
	24		XU8	B	C25	+		
	24		XU8	C	C25	-		
	23		XU8	E	C26	+		
	23		XU8	C	C26	-		
1	25		XU1	C	XU2	C		JUMPER
2	26	Ø	XU2	C	E1			GND
3	25		XU3	C	XU4	C		JUMPER
3	25		XU4	C	XU5	C		JUMPER
4	26	Ø	XU5	C	E1			GND
5	25		XU7	C	XU8	C		JUMPER
5	25		XU8	C	XU6	B		JUMPER
6	26	Ø	XU6	B	E1			GND
7	26	Ø	XU3	C	E1			GND
8	26	Ø	XU1	C	E1			GND
9	26	Ø	XU7	C	E1			GND
	44		TB1	2	C10	+		
	44		TB1	9	C10	-		
	45		TB1	2	TB1	10		R2 ACROSS TB1-2 & TB1-10
	45		TB1	1	TB1	9		R1 ACCROSS TB1-1 & TB1-9
	12	2	B1	+	TB1	2		+5VC
	12	6	B1	-	TB1	9		-20 VC

SIZE	CODE IDENT Nº	DWG Nº	REV
A	33783	WL 4028-1004	D

SHEET 3 OF 7

Rear Panel Assy (4028-1004) (Sheet 2 of 6) (S/N 400101 and on)

WIRE NO	ITEM NO	COLOR	FROM DEVICE	PIN NO	TO DEVICE	PIN NO	LENGTH	REMARKS
10	26	9	J7	A	XF1	1	3.0	LINE-HOT
11	26	5	J7	B	E1	-	6.0	LINE-GND
12	27	0	J7	C	P5	B	11	LINE-COMMON
13	27	9	XF1	2	P5	A	10	LINE-HOT
	27	shld	shld of 3 at P5		P5	L	3.0	SHIELD
14	26	209	J6	A	P5	F	9.0	+11VC
15	26	209	J6	A	J6	B	3.0	+11VC
16	26	209	J6	B	J6	C	3.0	+11VC
17	26	209	J6	C	J6	D	3.0	+11VC
18	26	209	J6	D	XU2	B	6.0	+11VC
19	26	209	XU2	B	XU1	B	4.0	+11VC
20	26	31	J6	R	P5	E	9.0	+20VC
21	26	31	J6	R	J6	S	3.0	+20VC
22	26	31	J6	S	J6	T	3.0	+20VC
23	26	31	J6	T	XU5	B	6.0	+20VC
24	26	31	XU5	B	XU4	B	2.5	+20VC
25	26	31	XU4	B	XU3	B	2.5	+20VC
26	26	609	J6	U	P5	D	9.0	-20VC
27	26	609	J6	U	J6	V	3.0	-20VC
28	26	609	J6	V	XU6	C	6.0	-20VC
29	26	8	J6	H	P5	G	9.0	+35VC
30	26	8	J6	H	J6	J		+35VC
31	26	8	J6	J	XU8	B		+35VC
32	26	8	XU8	B	XU7	B	2.5	+35VC
33	26	1	J6	E	P5	C	9.0	+5VC

SIZE	CODE IDENT NO	DWG NO	REV
A	33783	WL 4028-1004	D

SHEET 4 OF 7

Rear Panel Assy (4028-1004) (Sheet 3 of 6) (S/N 400101 and on)

WIRE Nº	ITEM Nº	COLOR	FROM DEVICE	PIN Nº	TO DEVICE	PIN Nº	LENGTH	REMARKS
34	26	1	J6	E	J6	F	3.0	+5VC
35	26	1	J6	F	J6	G	3.0	+5VC
36	26	0	J6	K	E1	-	3.0	GND
37	26	0	J6	L	E1	-	3.0	GND
38	26	0	J6	M	E1	-	3.0	GND
39	26	0	J6	N	E1	-	3.0	GND
40	26	0	J6	N	J6	P	3.0	GND
41	26	0	J6	P	J6	Q	3.0	GND
42	26	0	P5	L	E1	-	10.0	GND
43	26	0	P5	M	E1	-	10.0	GND
44	26	0	P5	N	E1		10.0	GND
45	26	1	P5	C	TB1	10	14.0	+5VC
46	26	609	P5	D	TB1	1	15.0	-20VC
47	29	92	P5	H	P2	25	39.0	AUDIO
48	29	91	P5	J	P2	29	39.0	AUDIO POT
49	29	90	P5	K	P2	30	39.0	AUDIO WIPER
50	54	2	XU1	E	P1	3	38.0	+5VA
51	54	2	XU2	E	P1	4	34.0	+5VA
52	54	3	XU3	E	P1	6	39.0	+12VA
53	54	3	XU4	E	P2	9	37.0	+12VA
54	54	3	XU4	E	P2	5	37.0	+12VA
55	54	3	XU5	E	P2	6	35.0	+12VA
56	54	6	XU6	E	P1	7	35.0	-12VA
57	54	6	XU6	E	P2	7	35.0	-12VA
58	54	4	XU7	E	P1	8	39.0	+24VA

SIZE	CODE IDENT Nº	DWG Nº	REV
A	33783	WL 4028-1004	D

SHEET 5 OF 7

Rear Panel Assy (4028-1004) (Sheet 4 of 6) (S/N 400101 and on)

WIRE Nº	ITEM Nº	COLOR	FROM DEVICE	PIN Nº	TO DEVICE	PIN Nº	LENGTH	REMARKS
59	54	4	XU8	E	P2	8	37.0	+24VA
60	54	0	E1	-	P1	1	30	GND
61	54	0	E1	-	P1	2	30	GND
62	54	0	E1	-	P2	1	30	GND
63	54	0	E1	-	P2	2	30	GND
-								
64	29	90	J5	1	P1	26	30	SRS
65	29	90	J5	2	P1	33	30	SRS
66	29	90	J5	3	P1	34	30	SRS
67	29	91	J5	4	P2	28	30	AGC (to Bargraph)
68	29	92	J5	5	P1	19	30	ASA
69	29	0	J5	6	P1	18	30	GND
70	29	93	J5	7	P1	17	30	ASD
71	29	94	J5	8	P2	23	30	500Hz Bw
72	29	95	J5	9	P2	24	30	5KHz Bw
73	29	96	J5	10	P2	13	30	ATN1
74	29	97	J5	11	P2	14	30	ATN2
75	29	98	J5	12	P2	10	30	RAS2
76	29	901	J5	13	P2	11	30	RAS3
77	29	902	J5	14	P2	12	30	CAL
78	29	903	J5	15	P1	15	30	DEL
79	29	904	J5	16	P1	16	30	ADD
80	29	905	J5	17	P1	11	30	SLF
81	29	906	J5	18	P1	12	30	SLM
82	29	907	J5	19	P1	13	30	SLS

SIZE	CODE IDENT Nº	DWG Nº	REV
A	33783	WL 4028-1004	D

SHEET 6 OF 7

Rear Panel Assy (4028-1004) (Sheet 5 of 6) (S/N 400101 and on)

WIRE Nº	ITEM Nº	COLOR	FROM DEVICE	PIN Nº	TO DEVICE	PIN Nº	LENGTH	REMARKS
83	29	908	J5	20	P1	24	30	STP
84	29	912	J5	21	P1	23	30	STR
85	29	913	J5	22	P1	25	30	RES
86	29	914	J5	23	P1	14	30	SSD/SSDA
87	29	915	J5	24	P1	22	30	AST
88	29	916	J5	25	P2	22	30	PRE 1
89	29	917	J5	26	P2	21	30	PRE 2
90	29	918	J5	27	P2	20	30	PRE 3
91	29	923	J5	28	P2	19	30	PRE 4
92	29	924	J5	29	P2	18	30	PRE 5
93	29	925	J5	30	P2	17	30	PRE 6
94	29	926	J5	31	P2	16	30	PRE 7
95	29	927	J5	32	P2	15	30	PRE 8
96	29	928	J5	33	P1	27	30	EOS
97	29	90	J5	34	P1	32	30	LOCK
98	29	92	J5	35	P2	26	30	Baseband (to SA)
99	29	0	J5	36	P2	27	30	GND
100	29	93	J5	37	P1	20	30	100
101	29	94	J9	-	P2	31	33	Aux Baseband Out
102	6	-	J4	-	P3	-		5 MHz - to 2A1J2
103	6	-	J8	-	P4	-		COUNT FROM 2A1J6

SIZE	CODE IDENT Nº	DWG Nº	REV
A	33783	WL 4028-1004	D

SHEET 7 OF 7

Rear Panel Assy (4028-1004) (Sheet 6 of 6) (S/N 400101 and on)

WIRE NO	ITEM NO	COLOR	FROM DEVICE	PIN NO	TO DEVICE	PIN NO	LENGTH	REMARKS
1	8	0	J1	1	A1	GND		
2		0		2	A2	GND		
3		0	A1	GND		GND		
4		0	J2	1		GND		To LED DISPLAY
5		2	J1	3	A1	+5VA		
6		2	A1	+5VA	A2	+5A		
7		5	J1	4	A1	+5B		
8		5	A1	+5B	A2	+5B		
9		1	J1	5		+5C		
10		1		6		+5C		
11		1	J2	2		+5C		
12		90	J1	10		CFS		
13		91		11		CCC		
14		92		12		CCK		
15		93		13		CIIL		
16		94		14		TVL1		Becomes MLS1
17		94	A2	TVL1		P1P1		
18		94	J1	15		P1P1		
19		95		16		TVL2		Becomes MLS2
20		95	A2	TVL2		P1P2		
21		95	J1	17		P1P2		
22		96		18		TVL2		Becomes MLS3

SIZE	CODE IDENT NO	DWG NO	REV
A	33783	WL 6025-1004	B

SHEET 2 OF 10

3-Path Programmer (6025-1004) (Sheet 1 of 9) (S/N 400100 and before)

WIRE NO.	ITEM NO.	COLOR	FROM DEVICE	PIN NO.	TO DEVICE	PIN NO.	LENGTH	REMARKS
23	8	96	A2	TVL3	A2	P1P3		
24		96	J1	19		P1P3		
25		97		20		ASD		USE ASD NEAR U32
26		98		21		ASP		
27		901	J3	1		SET		SUBPANEL SWITCH
28		901	J1	48		SET		
29		902	J3	2		SET		
30		902	J1	49		SET		
31		903	J3	3		SET		
32		903	J1	50		SET		
33		904	J3	4		LT		
34		904	J1	22		LT		
35		904		23		LT		
36		905	J3	5		CONT		
37		906		6		MAN		
38		906	A1	MAN		MAN		
39		907	J3	7		PROG		
40		908		8		HPB1		
41		908		9		HPB2		
42		912		10		SPB1		
43		912		11		SPB2		
44		913		12		RPB1		

SIZE	CODE IDENT NO.	DWG NO.	REV
A	33783	WL 6025-1004	B

SHEET 3 OF 10

3-Path Programmer (6025-1004) (Sheet 2 of 9) (S/N 400100 and before)

WIRE Nº	ITEM Nº	COLOR	FROM DEVICE	PIN Nº	TO DEVICE	PIN Nº	LENGTH	REMARKS
45	8	913	J3	13	A2	RPB2		
46		914		14		APB1		
47		914		15		APB2		
48		915	J1	52		SRS		
49		916	J3	16		STRL		
50		916		17		STPL		
51		917		18		RESL		
52		918		19	A1	PS0		
53		923		20		PS1		
54		924		21		PS2		
55		925		22		PS3		
56		926		23		PS4		
57		927		24		PS5		
58		928		25		PS6		
59		90		26		PS7		
60		91		27		PS8		
61		92		28		PS9		
62		93		29		PS10		
63		94		30		PS11		
64		95		31	A2	PS1		
65		96		32		PS2		
66		97		33		PS3		

SIZE	CODE IDENT Nº	DWG Nº	REV
A	33783	WL 6025-1004	B

SHEET 4 OF 10

3-Path Programmer (6025-1004) (Sheet 3 of 9) (S/N 400100 and before)

WIRE Nº	ITEM Nº	COLOR	FROM DEVICE	PIN Nº	TO DEVICE	PIN Nº	LENGTH	REMARKS
67	8	98	J3	34	A1	DISA		
68		901	J1	24		DEL		
69		901		25		DEL		
70		902		26		ADD		
71		902		27		ADD		
72		903		28		SLF		
73		903		45		SLF		
74		904		29		SLM		
75		904		46		SLM		
76		905		30		SLS		
77		905		47		SLS		
78		906		31	A2	STP		
79		907		32		STR		
80		908		33		RES		
81		912		34		SSDA		
82		913		35		AST		
83		914		36		PRE1		
84		915		37		PRE2		
85		916		38		PRE3		
86		917		39		PRE4		
87		918		40		PRE5		
88		923		41		PRE6		
88a	8	90	J1	55	A1	MAN		

SIZE	CODE IDENT Nº	DWG Nº	REV
A	33783	WL 6025-1004	B

SHEET 5 OF 10

3-Path Programmer (6025-1004) (Sheet 4 of 9) (S/N 400100 and before)

WIRE NO	ITEM NO	COLOR	FROM DEVICE	PIN NO	TO DEVICE	PIN NO	LENGTH	REMARKS
89	8	924	J1	42	A2	PRE7		
90		925		43		PRE8		
91		926		44		EOS		
92		927		51		PPS		TO J5
93		928	A1	MSP		MSP		
94		90		MSN		MSN		
95		91		ISP		ISP		
96		92		ISN		ISN		
97		93		2SP		2SP		
98		94		2SN		2SN		
99		95		3SP		3SP		
100		96		3SN		3SN		
101		97		PPS1		PPS1		
102		98		PPS2		PPS2		
103		901		1CLK		1CLK		
104		902		2CLK		2CLK		
105		903		3CLK		3CLK		
106		904		ADV1		ADV1		
107		905		RES1		RES1		
108		906		STR1		STR1		
109		907		ADV2		ADV2		
110		908		RES2		RES2		
110a		928		PPS3		PPS3		PATH 3 CLOCK

SIZE	CODE IDENT NO	DWG NO	REV
A	33783	WL 6025-1004	B

SHEET 6 OF 10

3-Path Programmer (6025-1004) (Sheet 5 of 9) (S/N 400100 and before)

WIRE NO	ITEM NO	COLOR	FROM DEVICE	PIN NO	TO DEVICE	PIN NO	LENGTH	REMARKS
111	8	912	A1	STR2	A2	STR2		
112		913		ADV3		ADV3		
113		914		RES3		RES3		
114		915		STR3		STR3		
115		916		PLC		PLC		
116		917		MCK		FCC		
117		918	J2	3		PLX		PATH 1
118		923		4		PLY		PATH 2
119		924		5		PLS		STROBE
120		925		6		4D1		FREQ-10kHz
121		926		7		4D2		TO LED
122		927		8		4D4		
123		928		9		4D8		
124		90		10		5D1		100kHz
125		91		11		5D2		
126		92		12		5D4		
127		93		13		5D8		
128		94		14		6D1		1MHz
129		95		15		6D2		
130		96		16		6D4		
131		97		17		6D8		
132		98		18		7D1		10MHz

SIZE	CODE IDENT NO	DWG NO	REV
A	33783	WL 6025-1004	B

SHEET 7 OF 10

3-Path Programmer (6025-1004) (Sheet 6 of 9) (S/N 400100 and before)

WIRE NO	ITEM NO	COLOR	FROM DEVICE	PIN NO	TO DEVICE	PIN NO	LENGTH	REMARKS
133	8	901	J2	19	A2	702		
134		902		20		704		
135		904		21		LT		LAMP TEST
136		904		22	A1	151		
137		905		23		152		
138		906		24		154		
139		907		25		158		
140		908		26		1051		
141		912		27		1052		
142		913		28		1054		
143		914		29		1058		
144		915		30		1M1		
145		916		31		1M2		
146		917		32		1M4		
147		918		33		1M8		
148		923		34		10M1		
149		924		35		10M2		
150		925		36		10M4		
151		926		37		10M8		
152	9		J5			5MHz		
			SHIELD			GND		
153			J4		A2	FC1		
			SHIELD			GND		

SIZE	CODE IDENT NO	DWG NO	REV
A	33783	WL 6025-1004	B

SHEET 8 OF 10

3-Path Programmer (6025-1004) (Sheet 7 of 9) (S/N 400100 and before)

WIRE NO	ITEM NO	COLOR	FROM DEVICE	PIN NO	TO DEVICE	PIN NO	LENGTH	REMARKS
154	8	927	A1	B	A2	B		
155	↓	928	↓	C	↓	C		
			TEST		POINTS			
			BOARD		CASTING TP			
156	8	2	A1	+5A	+5VA			
157	↓		↓	+5B	+5VB			
158	19		↓	TP6	TP6			
159	8	2	↓	MCK	TP7			
160	↓	↓	A2	+5C	+5VC			
161	↓	↓	↓	HPB2	TP1			
162	↓	↓	↓	SPB2	TP2			
163	↓	↓	↓	RPB1	TP3			
164	↓	↓	↓	APB2	TP4			
165	↓	↓	↓	STP	TP5			
166	↓	↓	↓	STR	TP6			
167	↓	↓	↓	RES	TP7			
168	↓	↓	↓	PPE1	TP8			
169	↓	↓	↓	PRE2	TP9			
170	↓	↓	↓	PRE3	TP10			
171	↓	↓	↓	PRE4	TP11			
172	↓		↓	PRE5	TP12			

SIZE	CODE IDENT NO	DWG NO	REV
A	33783	WL 6025-1004	B

SHEET 9 OF 10

3-Path Programmer (6025-1004) (Sheet 8 of 9) (S/N 400100 and before)

WIRE NO	ITEM NO	COLOR	FROM DEVICE	PIN NO	TO DEVICE	PIN NO	LENGTH	REMARKS
173	8	2	A2	PRE6	TP13			
174				PRE7	TP14			
175				PRE8	TP15			
176				AST	TP16			
177		903	J1	54	EOS TERM			

SIZE	CODE IDENT NO	DWG NO	REV
A	33783	WL 6025-1004	B

SHEET 10 OF 10

3-Path Programmer (6025-1004) (Sheet 9 of 9) (S/N 400100 and before)

WIRE NO	ITEM NO	COLOR	FROM DEVICE	PIN NO	TO DEVICE	PIN NO	LENGTH	REMARKS
1	18	0	A2	GND	J1	1		
2		0		GND		2		
3		8		+35V		3		
4		8		+35V		4		
5		7		BATT		5		
6		7		BATT		6		
7		5	FL2			7		WIRE FROM 1AXAZ SIDE
8		5	FL2			8		
9		5	FL2			9		
10		90	A2	EX		10		FREQ ADT
11		95	Q102	E		11		29V TEST
12		5	FL2			12		+5B → TEST SW
13		5	A3	+5B	FL2			FEED THROUGH TERMINAL
14		5	A2	+5B				
15		4	MIDDLE P.C. BOARD	SR	FL1			
16		4	A3	VIN				
17		93	A2	BV	Q102	C		2N3055-COLLECTOR
18		94		CV		B		BASE
19		95		EV		E		EMITTER
20		96		CL	Q101	C		2N3054-COLLECTOR
21		97		BL		B		BASE
22		98		EL		E		EMITTER
23		901	A1	1	A2	1		TWIST
24		903		4		501 GND		TOGETHER

SIZE	CODE IDENT NO	DWG NO	REV
A	33783	WL 6025-1006	A

SHEET 2 OF 4

Frequency Standard Assy (6025-1006) (Sheet 1 of 3) (S/N 400100 and before)

WIRE Nº	ITEM Nº	COLOR	FROM DEVICE	PIN Nº	TO DEVICE	PIN Nº	LENGTH	REMARKS
25	18	902	A1	3	A2	3		
26		904		5		5		
27		905		6		6		
28		906		8		8		
29		0		9		GND		
30		907		14		14		
31	18	908		15		CL		
32			R102		Q101	C		75Ω ACROSS
33						E		Q101 E&C
34			R101		E1			120Ω FROM TERMINAL
35					Q102	B		E1 TO Q102-B
36			Q103	D		C		
37				G		B		
38				S	E1			
39	17		A2	501	1A3	J4		
40				GND	SHIELD			
41				502	1A3	J3		
42				GND	SHIELD			
43				503	1A3	J2		
44				GND	SHIELD			
45				504	1A3	J5		
46	17			GND	SHIELD			
47	18	901	A3	B2	Q2	B		
48		903		E2		E		

SIZE	CODE IDENT Nº	DWG Nº	REV
A	33783	WL 6025-1006	A

SHEET 3 OF 4

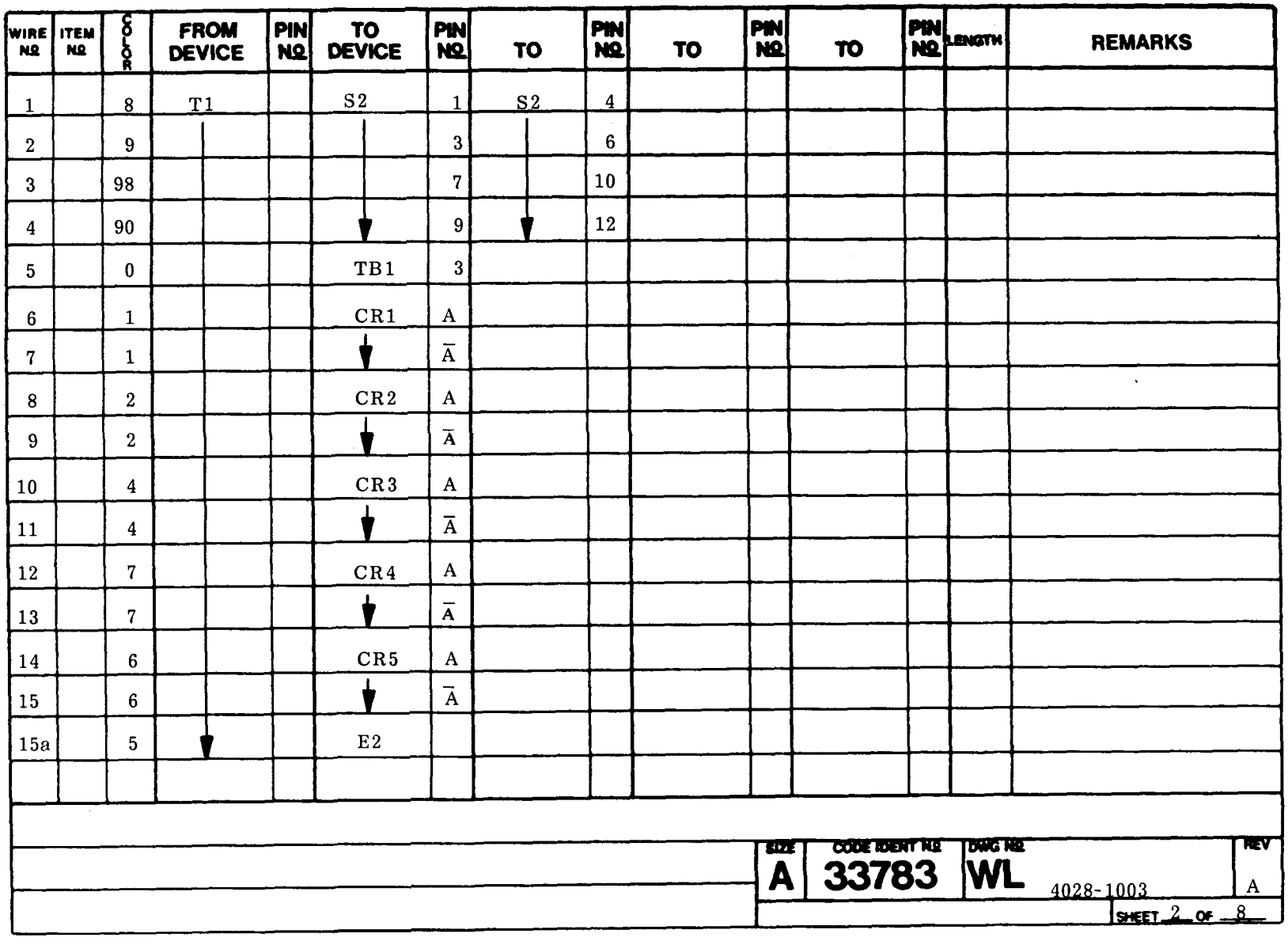
Frequency Standard Assy (6025-1006) (Sheet 2 of 3) (S/N 400100 and before)

WIRE Nº	ITEM Nº	COLOR	FROM DEVICE	PIN Nº	TO DEVICE	PIN Nº	LENGTH	REMARKS
49	18	902	A3	B3	Q3	B		
50	↓	904	↓	E3	↓	E		
51	↓	905	↓	XC	↓	C		
52			Q2	C	Q3	C		BUS COLLECTORS TOGETHER
53	18	95	K1	1	Q102	E		
54			↓	2	K1	7		JUMPER
55	18	7	↓	7	A1	BAT		
56			↓	4	K1	5		JUMPER
57	18	4	↓	5	FL1			
58	18	0	↓	8	A1	GND		

SIZE	CODE IDENT Nº	DWG Nº	REV
A	33783	WL 6025-1006	A

SHEET 4 OF 4

Frequency Standard Assy (6025-1006) (Sheet 3 of 3) (S/N 400100 and before)



WIRE NO	ITEM NO	COLOR	FROM DEVICE	PIN NO	TO DEVICE	PIN NO	TO	PIN NO	TO	PIN NO	TO	PIN NO	LENGTH	REMARKS
1		8	T1		S2	1	S2	4						
2		9				3		6						
3		98				7		10						
4		90				9		12						
5		0			TB1	3								
6		1			CR1	A								
7		1				$\overline{A}$								
8		2			CR2	A								
9		2				$\overline{A}$								
10		4			CR3	A								
11		4				$\overline{A}$								
12		7			CR4	A								
13		7				$\overline{A}$								
14		6			CR5	A								
15		6				$\overline{A}$								
15a		5			E2									

SIZE	CODE IDENT NO	DWG NO	REV
A	33783	WL 4028-1003	A

SHEET 2 OF 8

Enclosure Assy (4028-1003) (Sheet 1 of 7) (S/N 400100 and before)

WIRE NO.	ITEM NO.	COLOR	FROM DEVICE	PIN NO.	TO DEVICE	PIN NO.	TO	PIN NO.	TO	PIN NO.	TO	PIN NO.	LENGTH	REMARKS
16	62	9	TB1	1	S2	2	S2	5			NOTE			WIRE NO.16 AT TB1-1 AND WIRE NO.81 AT
17	↓	0	↓	2	↓	8	↓	11						TB1-1 MUST BE ON SEPARATE SOLDER
18	63		CR1	-	CR2	-	CR3	-	CR4	+	CR5	-		LUGS
19	62	0	CR1	-	C1	-								
20		1	CR1	+	C1	+								
21		0	CR2	-	C2	-	C3	-						
22		209	CR2	+	C2	+	C3	+						
23		0	CR3	-	C4	-	C5	-						
24		31	CR3	+	C4	+	C5	+						
25		0	CR4	+	C6	+								
26		609	CR4	-	C6	-								
27		0	CR5	-	C7	-	C8	-						
28		8	CR5	+	C7	+	C8	+						
29		0	E1		E2									
30	↓		CR1	-	E2									

SIZE	CODE IDENT NO.	DWG NO.	REV
A	33783	WL 4028-1003	A

SHEET 3 OF 8

Enclosure Assy (4028-1003) (Sheet 2 of 7) (S/N 400100 and before)

WIRE NO.	ITEM NO.	COLOR	FROM DEVICE	PIN NO.	TO DEVICE	PIN NO.	TO	PIN NO.	TO	PIN NO.	TO	PIN NO.	LENGTH	REMARKS
31	62	0	CR2	-	E2									
32			CR3	-	E2									
33			CR4	+	E2									
34			CR5	-	E2									
35		1	CR1	+	J6	E								
36		209	CR2	+	J6	A								
37		31	CR3	+	J6	R								
38		609	CR4	-	J6	U								
39		8	CR5	+	J6	H								
40		0	J6	K	E1									
41				M										
42				P										
43	65	9	J6	X	S2	12								
44		0		Y	TB1	3								
45		SHLD		Z	E1									

SIZE	CODE IDENT NO.	DWG NO.	REV
A	33783	WL 4028-1003	A

SHEET 4 OF 8

Enclosure Assy (4028-1003) (Sheet 3 of 7) (S/N 400100 and before)

WIRE NO.	ITEM NO.	COLOR	FROM DEVICE	PIN NO.	TO DEVICE	PIN NO.	TO	PIN NO.	TO	PIN NO.	TO	PIN NO.	LENGTH	REMARKS
46		9	F1	2	FL1	1								
47		0	J7	C	FL1	2								
48		5	J7	B	E1									
49		0	XU1	C	E1									
50			XU2	C										
51			XU3	C										
52			XU5	C										
53			XU6	B										
54			XU7	C										
55		209	XU1	B	CR2	+								
56			XU2	B										
57		31	XU3	B	CR3	+								
58			XU4	B										
59			XU5	B										
60		609	XU6	C	CR4	-								

SIZE	CODE IDENT NO.	DWG NO.	REV
A	33783	WL 4028-1003	A

SHEET 5 OF 8

Enclosure Assy (4028-1003) (Sheet 4 of 7) (S/N 400100 and before)

WIRE NO.	ITEM NO.	COLOR	FROM DEVICE	PIN NO.	TO DEVICE	PIN NO.	TO	PIN NO.	TO	PIN NO.	TO	PIN NO.	LENGTH	REMARKS
61		8	XU7	B	CR5	+								
62		↓	XU8	B	↓	↓								
63		0	P1	1	F1									
64		↓	↓	2	↓									
65		↓	P2	1	↓									
66		↓	↓	2	↓									
67			R1	1	C9	1								
68			R1	2	C9	2								
69			R2	1	C10	1								
70			R2	2	C10	2								
71			C9	1	E5									
72			C9	2	E3									
73			C10	1	E6									
74			C10	2	E4									
75	62	9	E5		E6									

SIZE	CODE IDENT NO.	DWG NO.	REV
A	33783	WL 4028-1003	A

SHEET 6 OF 8

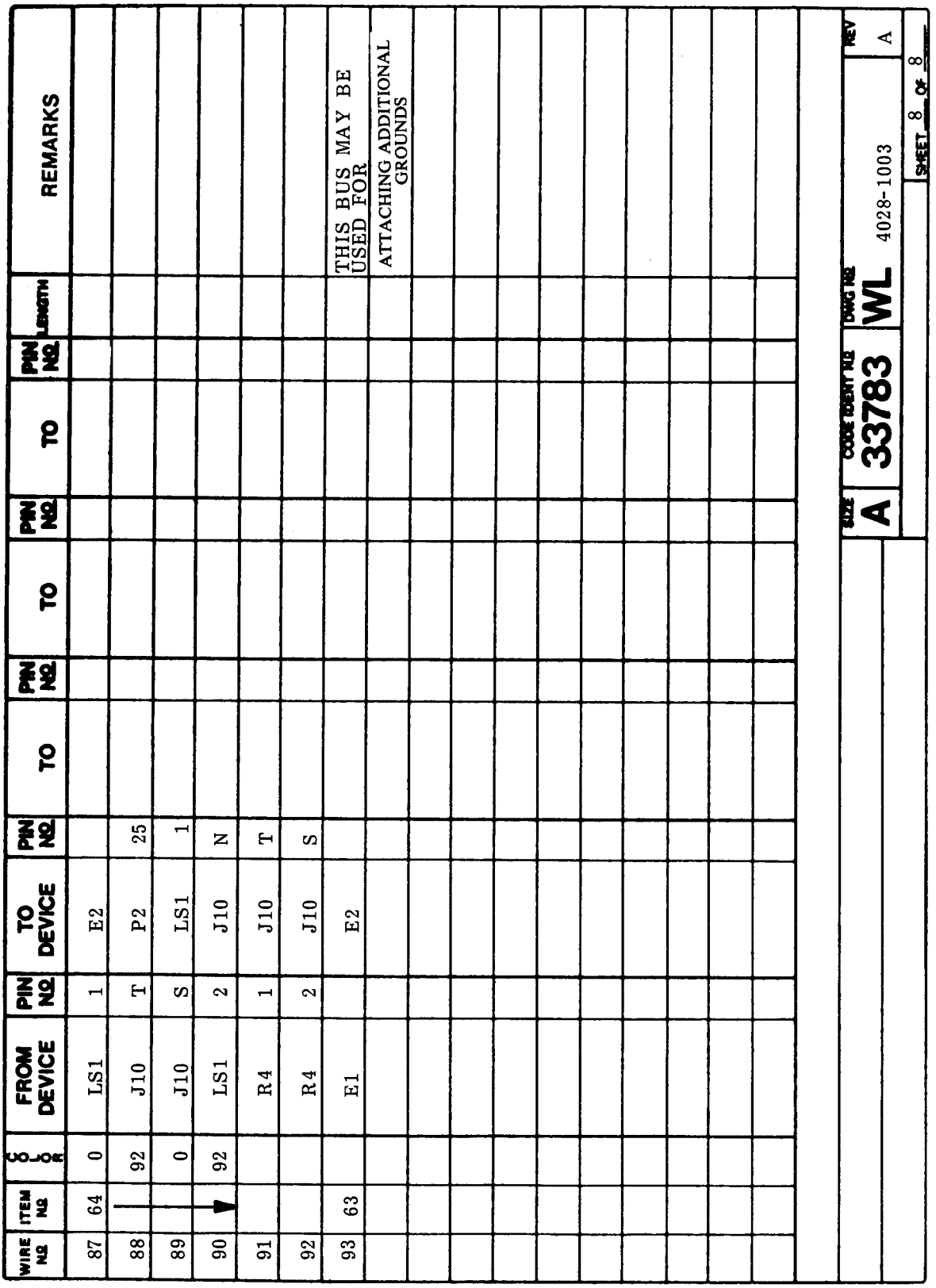
Enclosure Assy (4028-1003) (Sheet 5 of 7) (S/N 400100 and before)

WIRE NO.	ITEM NO.	COLOR	FROM DEVICE	PIN NO.	TO DEVICE	PIN NO.	TO	PIN NO.	TO	PIN NO.	TO	PIN NO.	LENGTH	REMARKS
76		5	B1		E3									
77		9	B1		E4									
78		6	B1		TB1	3								
79	64	9	S2	6	E4									
80	65	9	FL1	3	S1	1								
		0	FL1	4	S1	2								
		SHLD	E2		(FLOAT)									
81	65	9	S1	3	TB1	1					NOTE			WIRE #81 AT TB1-1 AND WIRE #16 AT
		0	↓	4	TB1	3								TB1-1 MUST BE ON SEPARATE SOLDER
		SHLD	(FLOAT)		E2									LUGS
82	64	1	S1	5	CR1	+								
83	↓	0	↓	6	E2									
84		0	R3	1	E2									
85		90	↓	2	P2	30								
86	↓	91	↓	3	↓	29								

SIZE	CODE IDENT NO.	DWG NO.	REV
A	33783	WL 4028-1003	A

SHEET 7 OF 8

Enclosure Assy (4028-1003) (Sheet 6 of 7) (S/N 400100 and before)



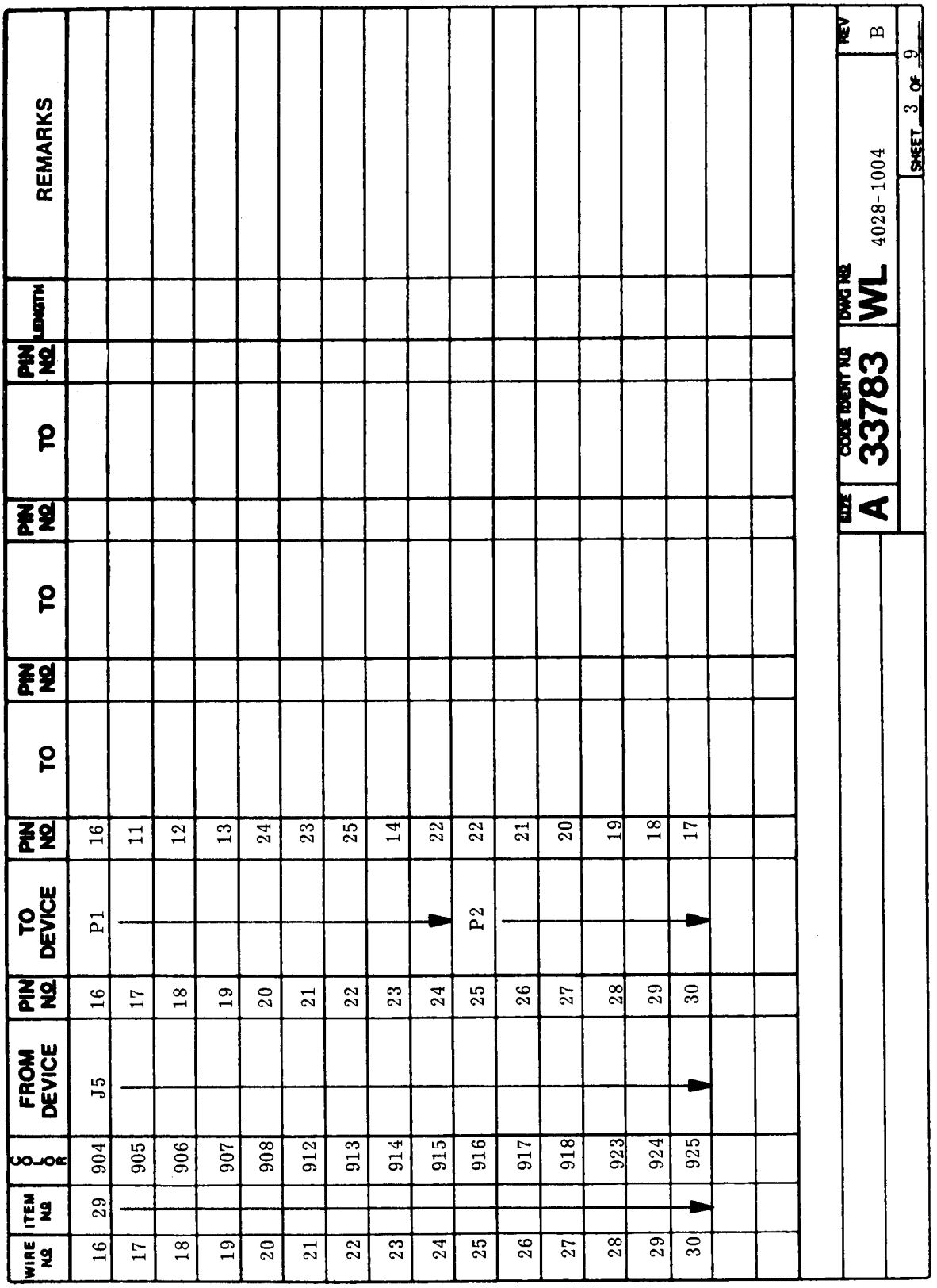
Enclosure Assy (4028-1003) (Sheet 7 of 7) (S/N 400100 and before)

WIRE NO.	ITEM NO.	COLOR	FROM DEVICE	PIN NO.	TO DEVICE	PIN NO.	TO	PIN NO.	TO	PIN NO.	TO	PIN NO.	LENGTH	REMARKS
1	29	90	J5	1	P1	26								
2				2		33								
3				3		34								
4		91		4	P2	28								
5		92		5	P1	19								
6		0		6		18								
7		93		7		17								
8		94		8	P2	23								
9		95		9		24								
10		96		10		13								
11		97		11		14								
12		98		12		10								
13		901		13		11								
14		902		14		12								
15		903		15	P1	15								
15a		90	P2	30	OPEN								31	
15b		91		29									31	
15c		92		25									31	

SIZE	CODE IDENT NO.	DWG NO.	REV
A	33783	WL 4028-1004	B

SHEET 2 OF 9

Rear Panel Assy (4028-1004) (Sheet 1 of 8) (S/N 400100 and before)



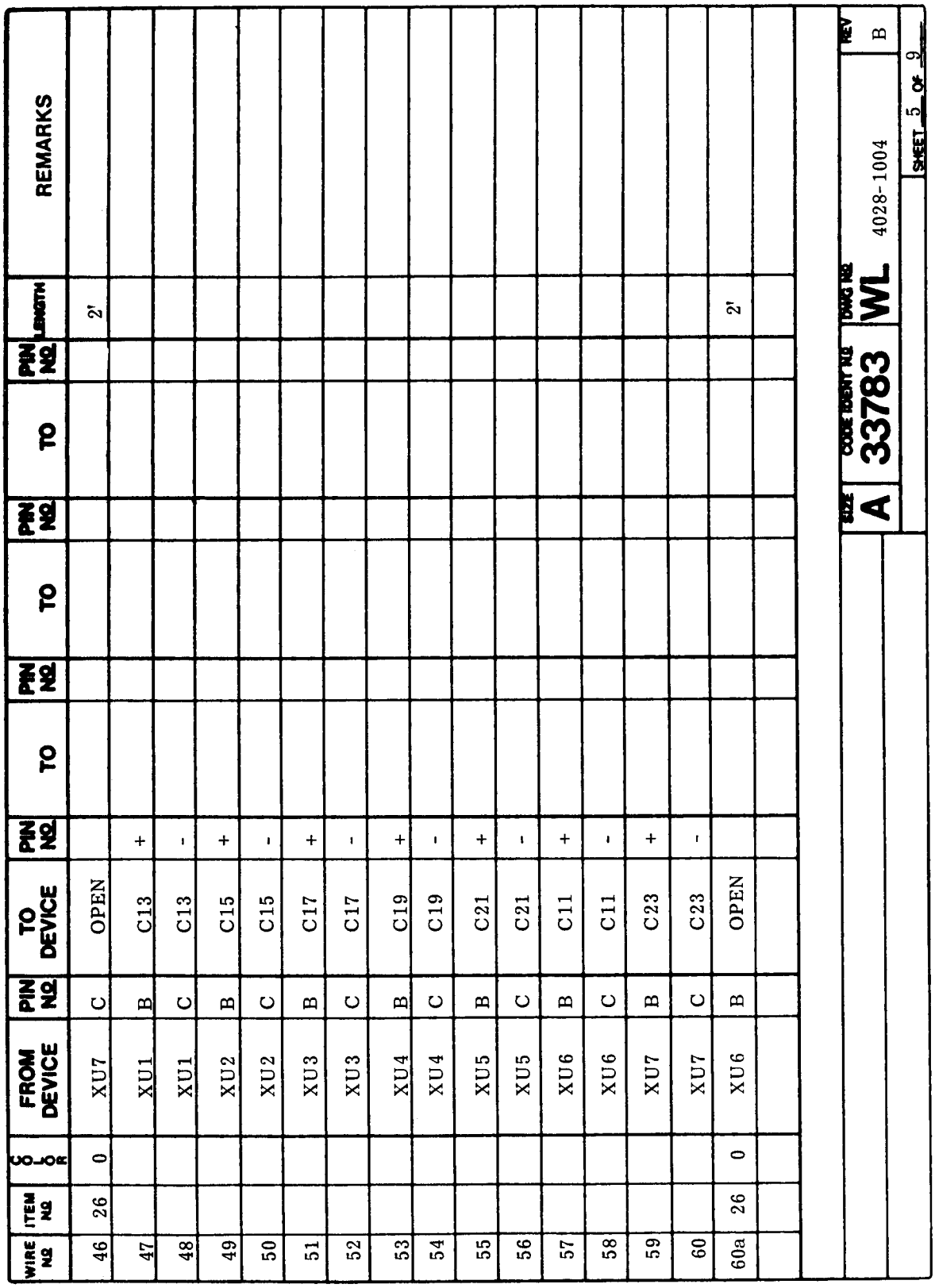
Rear Panel Assy (4028-1004) (Sheet 2 of 8) (S/N 400100 and before)

WIRE NO	ITEM NO	COLOR	FROM DEVICE	PIN NO	TO DEVICE	PIN NO	TO	PIN NO	TO	PIN NO	TO	PIN NO	LENGTH	REMARKS
31	29	926	J5	31	P2	16								
32		927		32		15								
33		928		33	P1	27								
34		90		34		32								
35		92		35	P2	26								
36		0		36		27								
37		93		37	P1	20								
38	28	-	J4		P3								26"	5MHz IN
39		-	J8		P4								26"	
40	29	94	J9		P2	31								
41	25	-	XU1	C	XU2	C								
42	26	0	XU1	C	OPEN								2'	
43	25	-	XU3	C	XU4	C	XU5	C						
44	26	0	XU3	C	OPEN								2'	
45	25	-	XU7	C	XU8	C	XU6	B						
45a	26	0	XU2	C	OPEN								2'	
45b		0	XU5	C	OPEN								2'	

SIZE	CODE IDENT NO	DWG NO	REV
A	33783	WL 4028-1004	B

SHEET 4 OF 9

Rear Panel Assy (4028-1004) (Sheet 3 of 8) (S/N 400100 and before)



WIRE NO	ITEM NO	COLOR	FROM DEVICE	PIN NO	TO DEVICE	PIN NO	TO	PIN NO	TO	PIN NO	LENGTH	REMARKS
46	26	0	XU7	C	OPEN						2'	
47			XU1	B	C13	+						
48			XU1	C	C13	-						
49			XU2	B	C15	+						
50			XU2	C	C15	-						
51			XU3	B	C17	+						
52			XU3	C	C17	-						
53			XU4	B	C19	+						
54			XU4	C	C19	-						
55			XU5	B	C21	+						
56			XU5	C	C21	-						
57			XU6	B	C11	+						
58			XU6	C	C11	-						
59			XU7	B	C23	+						
60			XU7	C	C23	-						
60a	26	0	XU6	B	OPEN						2'	

SIZE A | CODE IDENT NO 33783 | DWG NO WL 4028-1004 | REV B | SHEET 5 OF 9

Rear Panel Assy (4028-1004) (Sheet 4 of 8) (S/N 400100 and before)

WIRE NO.	ITEM NO.	COLOR	FROM DEVICE	PIN NO.	TO DEVICE	PIN NO.	TO	PIN NO.	TO	PIN NO.	TO	PIN NO.	LENGTH	REMARKS
61			XU8	B	C25	+								
62			XU8	C	C25	-								
63	26	209	XU1	B	OPEN								2'	
64	↓	↓	XU2	B	↓								2'	
65		31	XU3	B									2'	
66		↓	XU4	B									2'	
67		↓	XU5	B									2'	
68		609	XU6	C									2'	
69		8	XU7	B									2'	
70		↓	XU8	B	↓								2'	
71		209	J6	D	J6	C	J6	B	J6	A	OPEN		2'	JUMPER & TAIL
72		1	J6	G	J6	F	J6	E	OPEN				2'	↓
73		8	J6	J	J6	H	OPEN						2'	
74		0	J6	L	J6	K	OPEN						2'	
75	↓	0	J6	N	J6	M	OPEN						2'	↓

SIZE	CODE IDENT NO.	DWG NO.	REV
A	33783	WL 4028-1004	B

SHEET 6 OF 9

Rear Panel Assy (4028-1004) (Sheet 5 of 8) (S/N 400100 and before)

WIRE NO	ITEM NO	COLOR	FROM DEVICE	PIN NO	TO DEVICE	PIN NO	TO	PIN NO	TO	PIN NO	TO	PIN NO	LENGTH	REMARKS
76	26	0	J6	Q	J6	P	OPEN						2'	JUMPER & TAIL
77	↓	31	J6	T	J6	S	J6	R	OPEN				2'	
78	↓	609	J6	V	J6	U	OPEN							
79	27	9	J6	X	OPEN								1'	
		0	J6	Y	↓									ONE SHIELDED PAIR
		SHLD	J6	Z	↓									
80	29	0	P1	1	OPEN								3'	
81	↓	↓		2									3'	
82			P2	1									3'	
83		↓		2									3'	
84		2	XU1	E	P1	3								
85			XU2	E	↓	4								
86		3	XU3	E	↓	6								
87		↓	XU4	E	P2	9								+12V
88	↓	↓	XU4	E		5								+12V

SIZE	CODE IDENT NO	DWG NO	REV
A	33783	WL 4028-1004	B

SHEET 7 OF 9

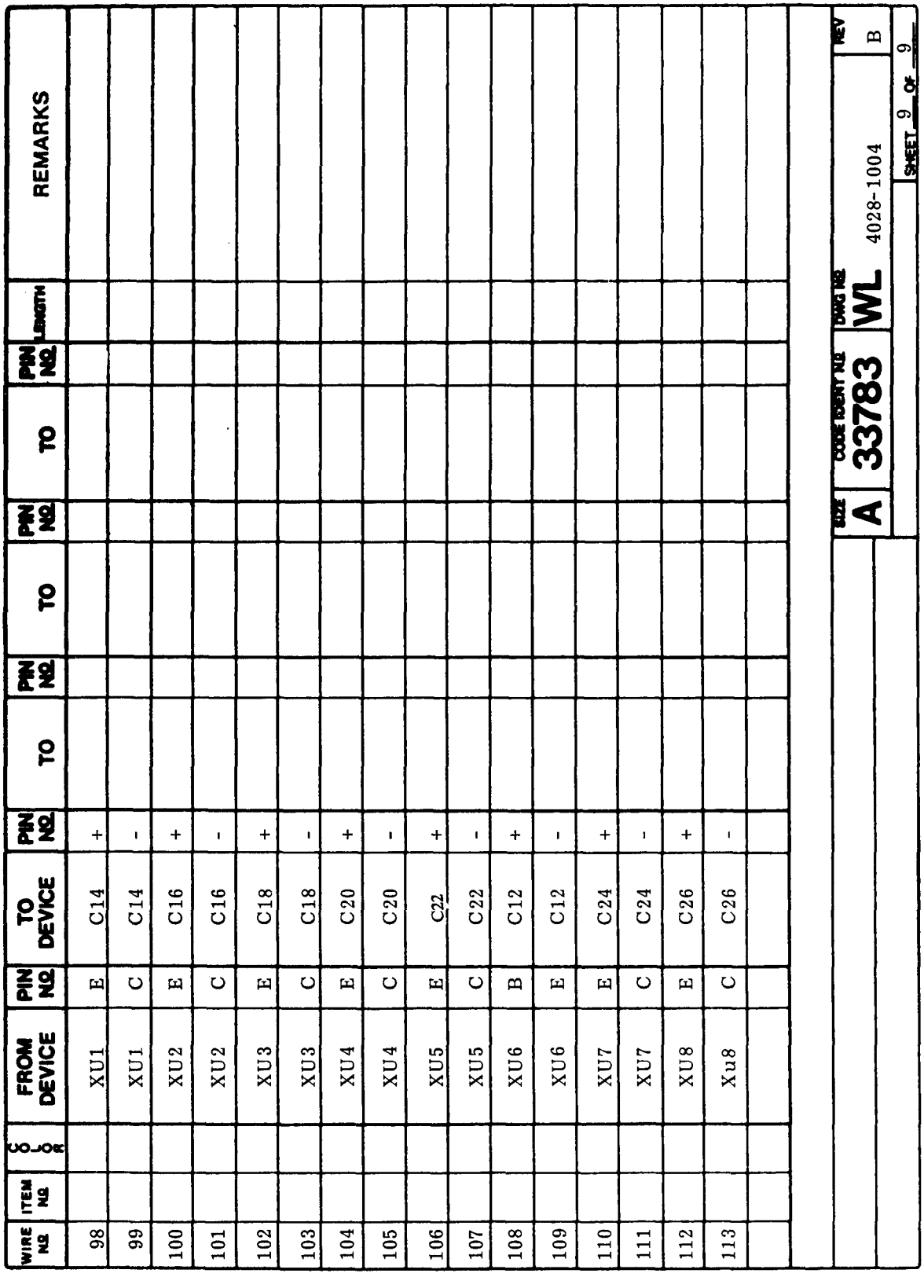
Rear Panel Assy (4028-1004) (Sheet 6 of 8) (S/N 400100 and before)

WIRE NO.	ITEM NO.	COLOR	FROM DEVICE	PIN NO.	TO DEVICE	PIN NO.	TO	PIN NO.	TO	PIN NO.	TO	PIN NO.	LENGTH	REMARKS
89	29	3	XU5	E	P2	6								+12B
90		6	XU6	E	P1	7								
91		6	XU6	E	P2	7								-12V
92		4	XU7	E	P1	8								
93		4	XU8	E	P2	8								+24V
94	26	9	J7	A	F1	1								
95		9	F1	2	OPEN								2'	
96		0	J7	C	OPEN								2'	
97		5	J7	B	OPEN								2'	

SIZE	CODE IDENT NO.	DWG NO.	REV
A	33783	WL 4028-1004	B

SHEET 8 OF 9

Rear Panel Assy (4028-1004) (Sheet 7 of 8) (S/N 400100 and before)



WIRE NO	ITEM NO	COLOR	FROM DEVICE	PIN NO	TO DEVICE	PIN NO	TO	PIN NO	TO	PIN NO	LENGTH	REMARKS
98			XU1	E	C14	+						
99			XU1	C	C14	-						
100			XU2	E	C16	+						
101			XU2	C	C16	-						
102			XU3	E	C18	+						
103			XU3	C	C18	-						
104			XU4	E	C20	+						
105			XU4	C	C20	-						
106			XU5	E	C22	+						
107			XU5	C	C22	-						
108			XU6	B	C12	+						
109			XU6	E	C12	-						
110			XU7	E	C24	+						
111			XU7	C	C24	-						
112			XU8	E	C26	+						
113			Xu8	C	C26	-						

SIZE A | CODE IDENT NO 33783 | DWG NO WL 4028-1004 | REV B | SHEET 9 OF 9

Rear Panel Assy (4028-1004) (Sheet 8 of 8) (S/N 400100 and before)

SECTION 7

FREQUENCY MANAGEMENT OF HF NETS USING AN/TRQ-35(V) EQUIPMENT

7-1. INTRODUCTION

7-2. The TCS-4B Chirpsounder Transmitter, RCS-4B Chirp sounder Receiver, and RSS-4 Spectrum Monitor form a complete equipment set, AN/TRQ-35(V), to manage frequency selection for any HF circuit. Three TCS-4B's can be used with one RCS-4B to manage a 3-circuit network. Experience has shown that one RSS-4 colocated with the RCS-4B provides channel occupancy data adequate for all sites within several hundred kilometers. For long range circuits (greater than 2000 km) , use of separate RSS-4's at each end of the circuit is advisable.

7-3. The following discussion presents a brief summary of the essential elements of HF propagation which need to be understood in order to perform network management. It then covers the basic principles of Chirp sounding, instructions for interpreting the RCS-4B display, and procedures for frequency managing an HF network.

7-4. HF radio energy can propagate for great distances through the interaction of the electromagnetic waves and the free electrons of the earth's ionosphere. This interaction causes the radio energy to be refracted or partially reflected from a straight-line path. The amount of refraction depends on the radio wavelength and the electron density in the ionosphere and can be sufficient to return RF energy to the earth's surface on a "one-hop" basis at ranges up to about 4000 km.

7-5. The ionosphere is defined as that part of the earth's atmosphere in which free electrons exist in sufficient quantities to affect propagation of radio waves, Thus, the ionosphere can be thought of as existing from 40 to 50 km altitude to a height of several earth radii.

7-6. Free electrons are produced primarily by the effects of solar radiation on molecules at ionospheric altitudes. The production of electrons and their subsequent recombination with positive ions or attachment to neutral molecules are dependent, among other factors, on altitude. There are three altitude regions of interest:

Region	Altitude range (approx)
D	50-90 km
E	90-140 km
F	above 140 km

7-7. The D-region is that portion of the ionosphere where electrons, agitated by RF energy, more readily collide with molecules or are more rapidly absorbed by recombination or attachment. This collision and absorption process significantly reduces the RF signal propagation strength and is the primary contributor to signal propagation path loss during daylight hours at lower HF frequencies. Because the probability of electron collision and absorption increases with increas-

ing electron density and RF signal wavelength (or decreasing signal frequency), the electron content in the D-region establishes the lowest propagating frequency for a given transmitter output. D-region absorption peaks around noontime. At night, the natural recombination process depletes the D-region electrons, and lower-frequency signals can propagate virtually unattenuated.

7-8. The E-region is of little interest to HF communicators except for a phenomen which generally occurs near its boundary with the D-region. It is at this altitude (approximately 90 km) that the “sporadic E“ (E_s) layer is observed.

7-9. Sporadic E appears not to be caused directly by the effects of solar radiation, but rather by secondary effects such as wind shears. The result is a layer which is generally extremely thin (perhaps tens or hundreds of meters thick), highly ionized (causing partial reflection of signals at frequencies far higher than the normal ionosphere will support), and spatially dependent (visible on one path, but not present on another). On occasion, E_s can be so strong as to “blanket” the upper ionospheric layers (i.e., prevent radio waves from reaching higher altitudes); while at other times, RF energy easily penetrates the Es and also propagates via normal F-region modes.

7-10. Because of its variability, E_s has been examined largely by statistical means. At mid-latitudes, E_s is observed on at least half of the days for most hours during the summer months becoming less frequent as autumn and winter pass, then increasing again in late spring. It is observed more often in daytime than at night. At high latitudes, seasonal variations are less, and E_s is observed more often at night. There is no firm indication of any correlation of E_s with the 11-year solar cycle, varying correlation statistics related to solar storm activity, and data showing significant year-to-year variation of occurrence over a given location.

7-11. Radio propagation in the F-region is a direct function of the electron content in the region, which continually varies. In general, F-region ionization is a superposition of three cycles: a diurnal cycle, a seasonal cycle, and the 11-year solar activity cycle. Ionization usually builds quickly after dawn in the ionosphere and peaks around midday. It falls off more slowly as the afternoon and evening passes reaching a minimum in the hours after local midnight. Nighttime ionization is higher in summer than winter. However, daytime ionization is often greater in winter than summer - a phenomenon called the “winter anomaly."

7-12. The effect of increasing electron content in the ionosphere is to increase the maximum radio frequency that will propagate to any range. Thus, the maximum propagating frequency, less affected by D-region than lower frequencies, is generally established by the ionosphere and not by transmitter power or antenna characteristics (although these latter factors affect the strength of the signal relative to received noise).

7-13. Figure 7-1 illustrates several important features of HF propagation that should be kept in mind:

a. At lower frequencies, ionization levels in the ionosphere usually permit signal propagation by one-hop or multiple-hop modes. The lowest observed fre-

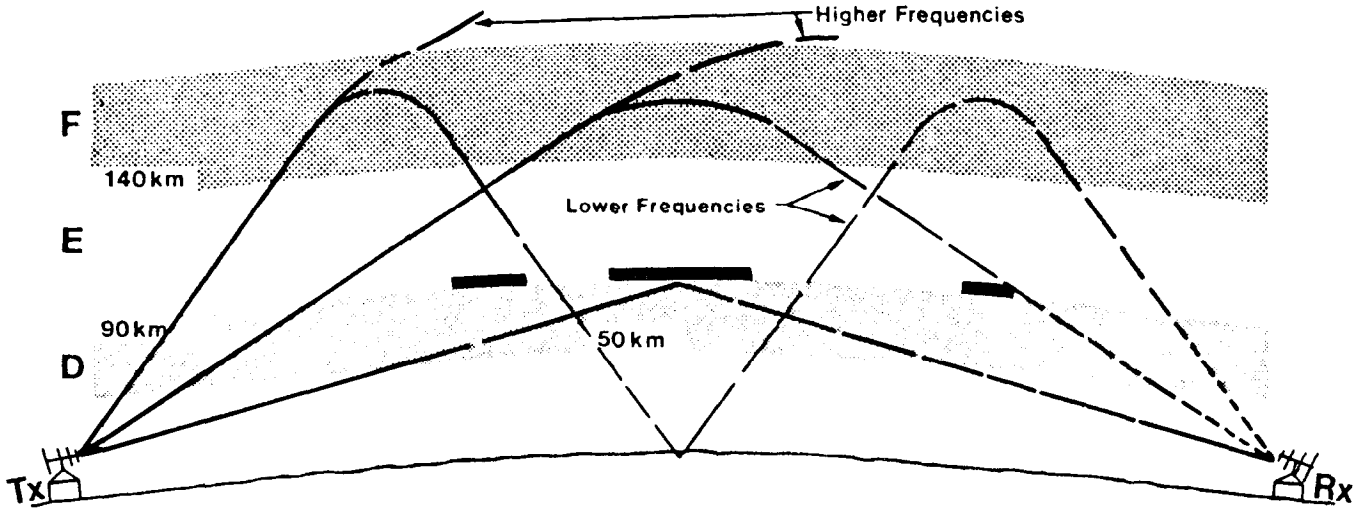


FIGURE 7-1. Simplified Characteristics of HF Propagation.

quency (LOF) is set by signal attenuation caused primarily by D-region absorption. The maximum observed frequency (MOF) is generally set by the electron density in the E_s or F layers.

b. As radio frequency increases, the signal energy propagating via F modes penetrates deeper into the ionosphere. If sufficient refraction occurs to return the signal to earth, the result is generally an increasing propagation time delay with frequency.

c. Signal energy propagating via E_s will always arrive earlier than energy via the F region. In addition, because the Es layer is so thin, propagation time delay is essentially independent of frequency.

d. Sporadic E can vary greatly in spatial extent. Thus, great care must be taken in assuming that, because Es is observed on one path, it must be present on another path.

7-14. In addition to the above items, there are several other propagation factors to remember:

a. The ionosphere is an atmospheric region in near-constant turbulence. Ionization concentration and depletion regions constantly occur creating focusing and defocusing of radio energy. The result is a near-continuous variation of the MOF (usually over small limits) and signal fading on any frequency.

b. The electron concentration in the F-region usually changes slowly. Thus, propagating frequency bands generally vary in time periods measured in many tens of minutes. Sporadic E, on the other hand, can change rather markedly in just a few minutes and must be treated very carefully.

c. Experimental measurements confirm that radio propagation is essentially reciprocal. That is, given identical equipment at both ends of a circuit, frequencies propagating in one direction will propagate in the opposite direction. There are some variable effects created by the earth's magnetic field which primarily affect east - west circuits, but these are secondary in nature.

d. Because of the earth's magnetic field, RF electromagnetic energy undergoes a "splitting" of its electrical and magnetic fields into waves having both clockwise and counterclockwise circular polarization. The result is that the energy in, say, a one-hop F-mode can actually propagate via two different paths with different time delays and show as two traces on the RCS-4B CRT display. The two modes are called "ordinary" and "extraordinary" and are labeled 0-mode and X-mode. The maximum 0-mode frequency is always less than the maximum X-mode frequency.

e. For short-distance circuits (≈35-50 miles over land and up to 200-300 miles over sea water) surface wave propagation is possible. A vertically polarized transmitting antenna couples radio energy best with the earth's surface, and a vertically polarized receive antenna produces the strongest received signal.

f. Propagating frequencies depend on path length with the maximum propagating frequency increasing as path length increases up to the 1-hop limit. Thus, as shown in figure 7-2, the optimum frequency for a short path may be attenuated for a longer path, while the optimum frequency for a long path may penetrate the ionosphere at the higher takeoff angle needed to reach the shorter distance.

7-15. PRINCIPLES OF CHIRPSOUNDING

7-16. A Chirp sounder transmitter emits a continuous "coherent" signal that increases in radio frequency in a linear manner. The result can be thought of as a linear ramp as shown in figure 7-3(a). At a given receiver location, the energy emitted on any given frequency propagates via one or more "modes" with different time delays. Figure 7-3(a) shows examples for four frequencies.

7-17. Because the Chirpsounder transmitter and receiver involve linear frequency sweeps without significant phase discontinuities, a properly synchronized transmitter /receiver combination causes the energy in each mode to produce a tone in the receiver, as indicated by figure 7-3(b). The pitch of each tone is linearly proportional to the time delay of the mode it represents. The receiver output is processed by a spectrum analyzer, and the individual tones are displayed as an "ionogram" such as depicted in the lower right of figure 7-3(b).

7-18. Figure 7-4 shows an example ionogram produced on the CRT of the RCS-4B receiver. The lower part of the display shows propagating signals vs frequency and indicates their relative propagating time delay. The maximum observed frequency (MOF) is at 7.6 MHz; the lowest observed frequency (LOF) is at approxi-

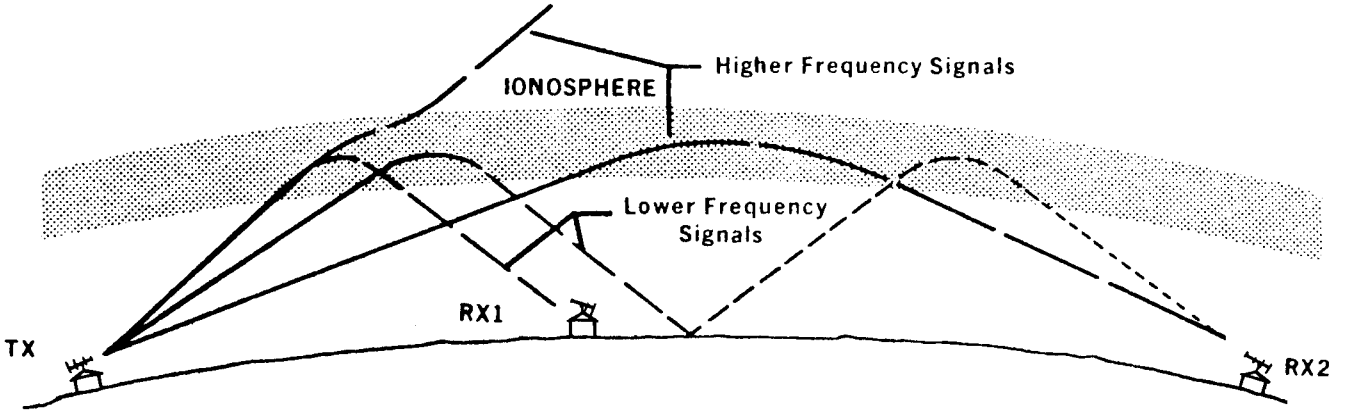


FIGURE 7-2. Effect of Range on HF Propagation.

mately 2.4 MHz. The l-hop mode shows the characteristic splitting of the 0-mode and X-mode. The upper part of the display shows received power vs frequency. It can be used as an indicator of frequencies with greatest received signal strength, however care must be taken in extrapolating such data if the sounder system utilizes different antennas than the communication systems on the circuit.

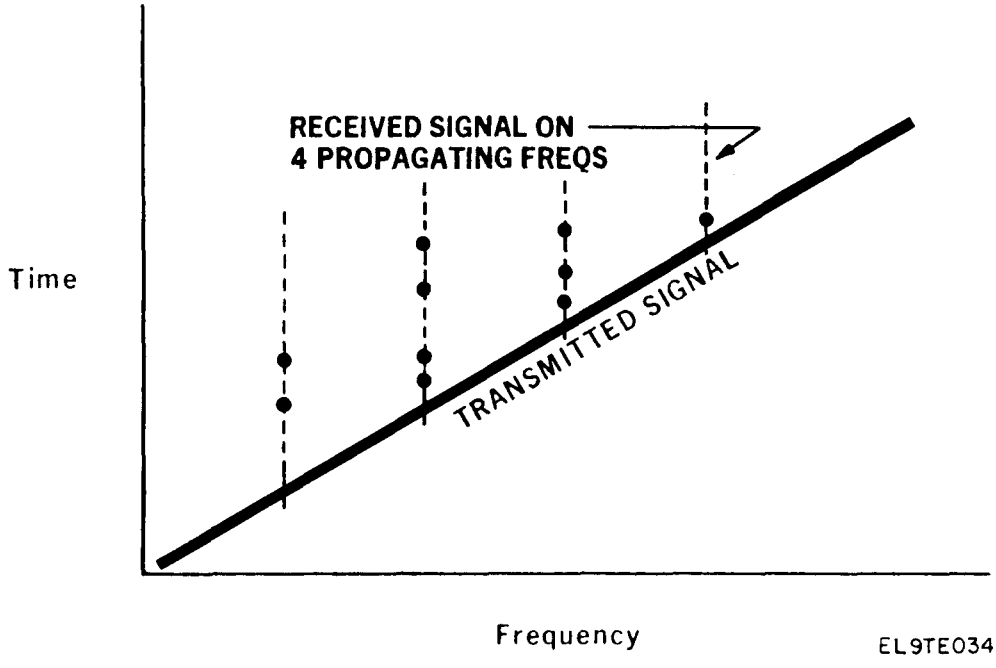
7-19. INTERPRETING THE RCS-4B DISPLAY

7-20. In general, the "best" communication frequencies are those showing the following characteristics (in order of importance):

a. A nearly continuous trace on the CRT throughout the band of interest, preferably near the MOF.

b. Maximum received signal strength on the upper bar graph (some sacrifice in signal strength can sometimes be advisable if use of a much higher frequency is possible).

c. Minimum multipath propagation or total time delay spread.


RECEIVED SIGNAL ON
4 PROPAGATING FREQS
TRANSMITTED SIGNAL
Time
Frequency
EL9TE034

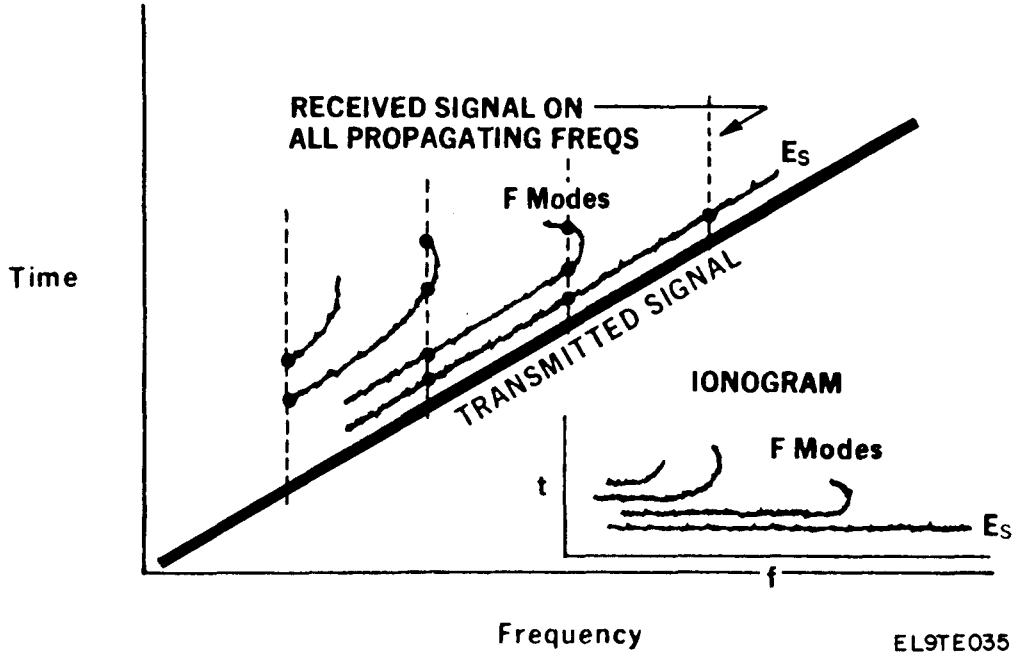

RECEIVED SIGNAL ON
ALL PROPAGATING FREQS
Es
F Modes
TRANSMITTED SIGNAL
IONOGRAM
F Modes
t
Es
f
Time
Frequency
EL9TE035

FIGURE 7-3.

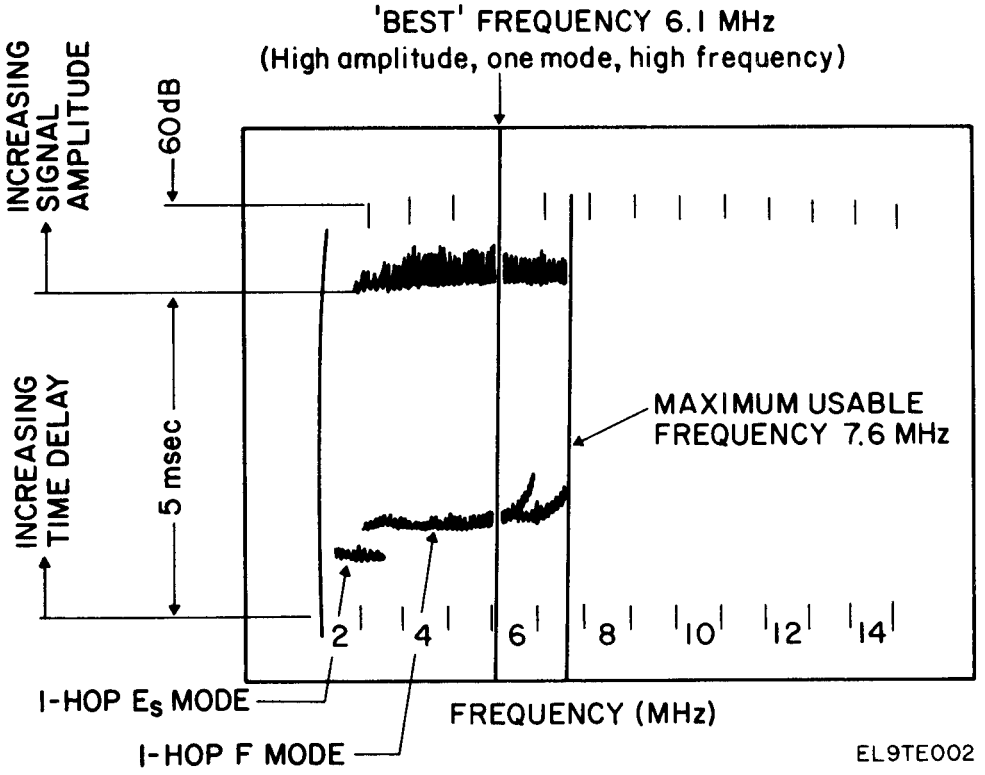


FIGURE 7-4. Example RCS-4B Ionogram and Received Signal Power Display.

Figure 7-4 shows a classic example in the band around 6.1 MHz, although the band from 3.6 to 6.4 MHz satisfies the above criteria and would provide excellent communication,

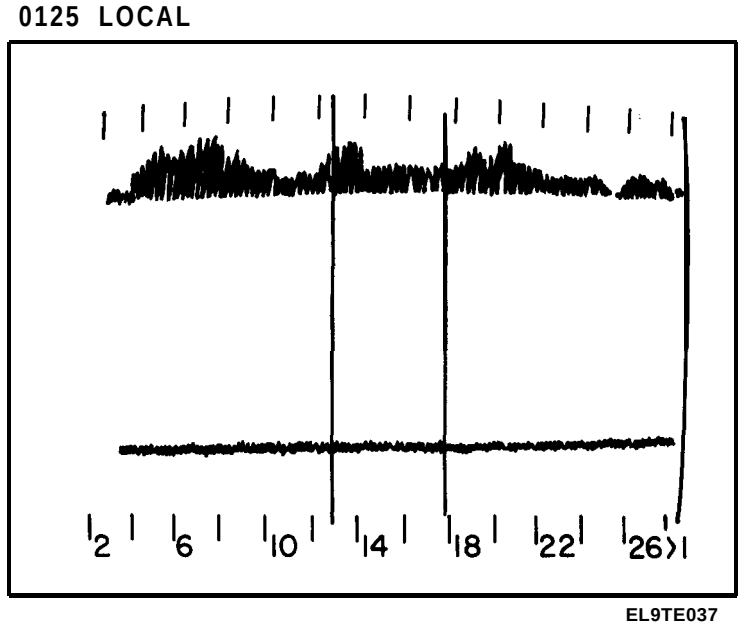
7-21. The most important exception to the above criteria occurs in dealing with sporadic E propagation. In general, sporadic E provides many advantage; for HF communication, particularly for military applications:

a. It often provides strong propagation at frequencies above the F-mode MOF where atmospheric noise is less, interference is less likely, and antenna systems are usually more effective.

b. Because it is non-dispersive, strong E_s propagation can support higher data rate communication than normal F-mode propagation.

c. Operation at frequencies above the expected MOF reduces the probability of signal intercept. In addition, the patchy characteristic of E_s further mitigates against signal intercept or jamming in directions other than the great circle path of the comm circuit. However, the “sporadic” nature of sporadic E must be fully accounted for in its use for an HF communications circuit.

7-22. Figure 7-5 shows an excellent example of the problems one can have with sporadic E. The upper photo shows strong sporadic E to 28 MHz. Note particularly that the band from 18-22 mHz satisfies all criteria of para. 7-20 above. How-



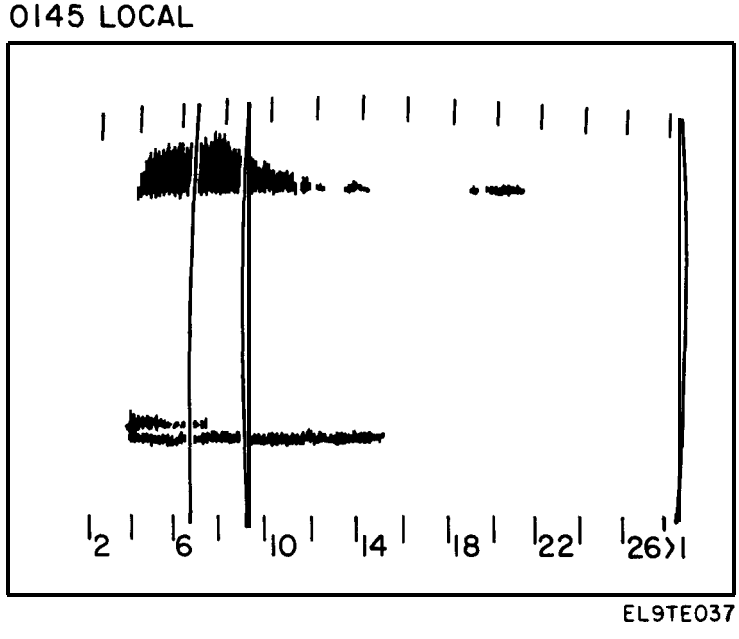


FIGURE 7-5. Example of Rapidly Changing E_s Propagation.

ever, the lower photo shows that 20 minutes later the MOF has dropped to 15 MHz, and propagation in the 18-22 MHz band is nil. Interestingly, in the next 10 minutes, conditions returned to those of 0125 local time.

7-23. Figure 7-5 and 7-6 show very clearly how easy it is to recognize sporadic E propagation on the RCS-4 CRT display. Sporadic E will nearly always (exceptions are very rare) show two important characteristics:

a. E_s will be the earliest arriving skywave mode and will be the lowest trace on the display.

b. The Es trace appears as a straight line with near-constant time delay vs frequency as contrasted with F-mode propagation which will generally show variable time delay particularly near the MOF of each mode.

7-24. For short path lengths, care must be taken to avoid confusion between Es and surface wave propagation as their appearance on the CRT is similar. Figure 7-7 shows ionograms taken on two circuits near local midnight. The upper photo shows 1-hop F and Es propagation; the lower photo shows 1-hop F and surface wave propagation. There is little to separate the surface wave from the Es except for the slightly greater time delay spread between the surface wave and the F-mode propagation and that surface wave propagation shows significantly less variation with time than E_s. For an 80-km circuit, the following typical signal propagation time delays can be expected.

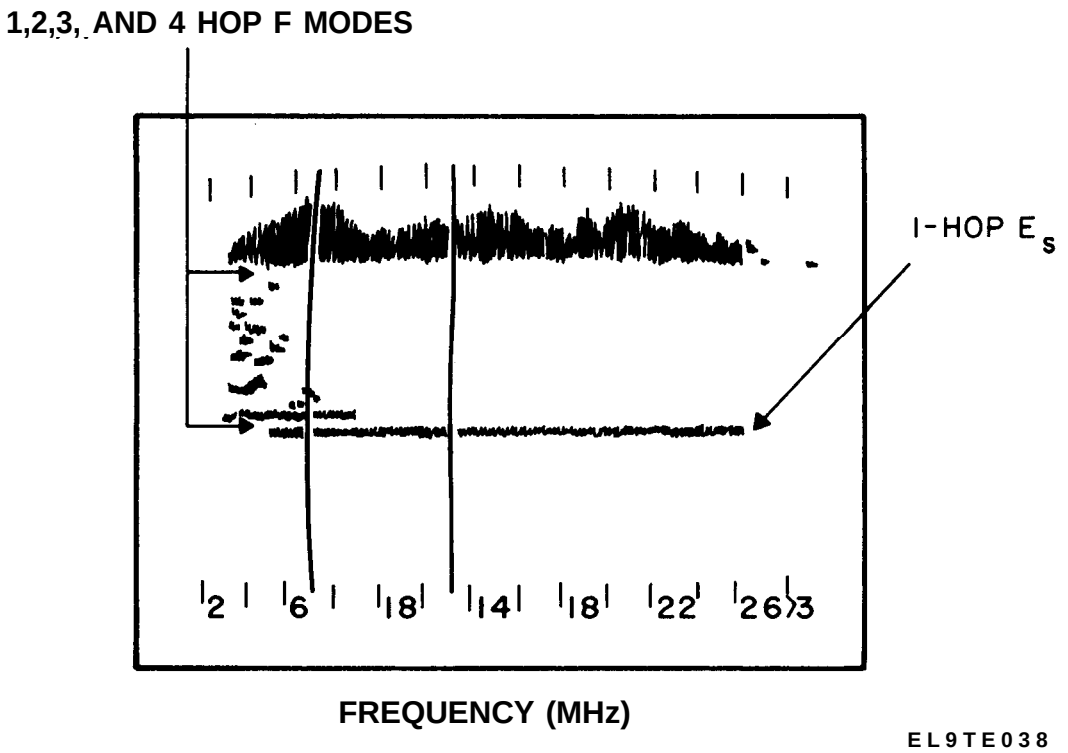
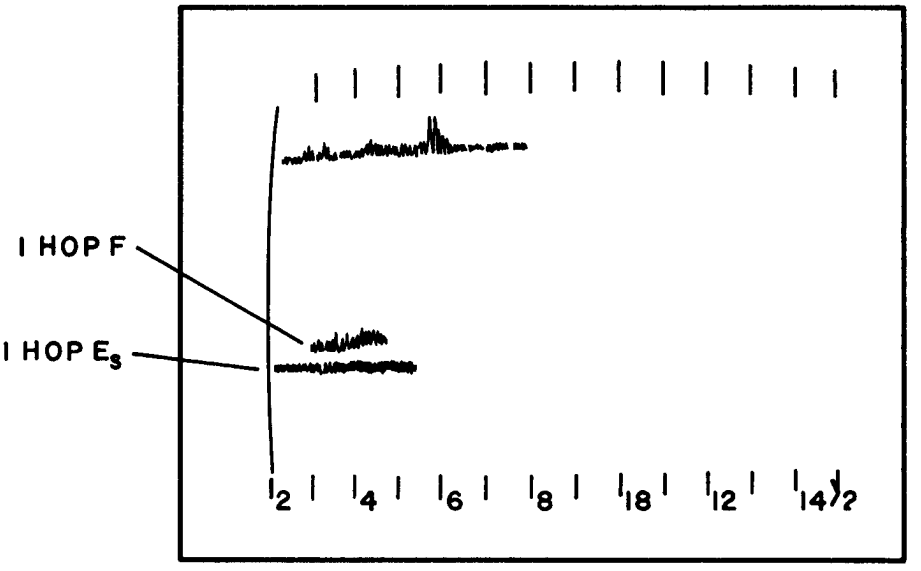


FIGURE 7-6. Example of Strong E_s Propagation extending well past the F-mode MOF.



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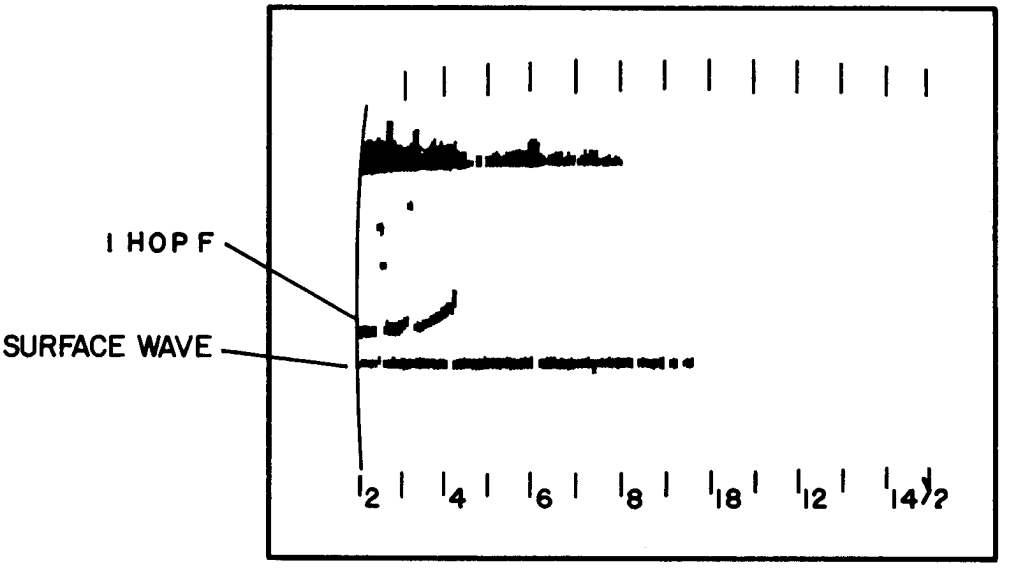

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FIGURE 7-7. Example comparing E_s and Surface Wave Modes.

Mode	Time delay (ms)	Relative time delay (ms)
Surface Wave	.27	0
1-Hop E_s	.60	.33
1-Hop F	1.60	1.33

The relative time delay difference between the surface wave and E_s modes is not very great and diminishes as range increases. Figure 7-4 provides the best solution to the dilemma: an ionogram showing both modes simultaneously.

7-25. Figure 7-7 shows another factor to consider in monitoring the RCS-4B CRT. The bar graph shows received signal power vs frequency which need not always be the received Chirp sounder signal. High atmospheric noise or (as in the case of figure 7-7) the output of nearby transmitters can also affect the bar graph. Strong interfering signals will cause the effects shown in figure 7-7: (1) dots running vertically on the lower part of the display, (2) momentary interruption of the received signal traces, and (3) associated peaks in the signal level bar graph.

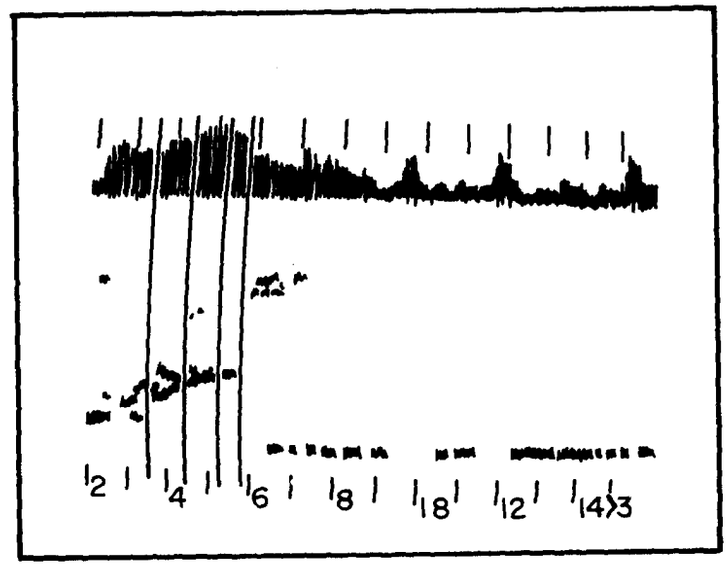
7-26. In summary, then, the following guidelines are offered in the use and interpretation of the RCS-4B CRT display:

a. Before the RCS-4B is synchronized with any transmitter, set the INPUT ATTENUATOR to 0 dB and run several sweeps to survey the local noise environment. If excessive noise appears on the display in the form of dots on the screen and very high signal level indication, add 10 dB to the attenuator before attempting to operate the automatic synchronization feature (to lower the probability that the auto-sync logic will wrongly interpret the dots as received signal).

b. After synchronization has occurred, adjust the INPUT ATTENUATOR to the lowest value that, if possible, permits only the received Chirpsounder signal to cause a display on the signal-level bar graph. For example, the top of figure 7-8 shows an ionogram recorded with the RCS-4B input attenuator set at 0. Note the high noise level showing on the bar graph (the RCS-4B was situated near an active machine shop). The bottom of figure 7-8 shows how the ionogram would probably appear with the input attenuator set at 20 dB . Observe how much simpler the lower display is to interpret.

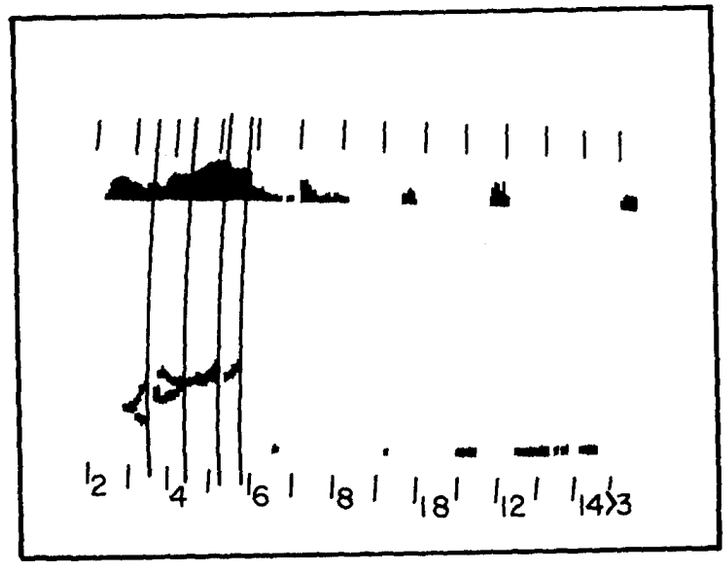
c. From time-to-time, run received sweeps without signal to observe the changing noise level. Remember that in determining the best frequency bands, it is signal-to-noise ratio rather than signal power that is important. Check also for any spikes in the bar graph display caused by interference signals. Remember also that the bar graph is meaningless regarding propagation from the transmitter if no trace is seen on the time-delay portion of the CRT display.

d. Know those frequencies where local interference may cause spurious output on the signal level graph. Running periodic sweeps on a path where a Chirpsounder transmitter is not operating or running a received sweep in the RCS-4B's MANUAL mode (on Path 1) will show the likely trouble spots.



EL9TE040

(a) Ionogram recorded with 0 dB attenuations



EL9TE040

(b) How ionogram (a) would appear with 20 dB attenuation

FIGURE 7-8. Example showing how proper use of the RCS-4B Input Attenuator can simplify display interpretation.

e. Keep close track of the F-mode and E_s MOF's for several days and nights to learn their short term and long term fluctuations. Learn the periods around dawn and sunset when major propagating frequency changes occur. Note the strength and variability of the E_s propagation. (The frequency cursor storage feature of the RCS-4B display can be used to keep track of MOF variations.)

f. Select the best propagating band on the basis of the criteria given in para. 7-20. If more than one band satisfies the criteria, the higher frequency band is generally to be preferred even at some sacrifice of received power.

g. Before judging the suitability of an Es mode, observe its performance for half an hour or so to determine if it is prone to serious short term fluctuations. Watch for signs that the E_s mode may be breaking up (e.g. falling MOF or gaps or dots in the E_s trace). Do not operate closer to the Es MOF than perhaps 30% below the MOF.

7-27. Numerous tests have been run comparing HF communications quality with the corresponding Chirpsounder ionograms. Figures 7-9 through 7-12 show examples. In figure 7-9, one would expect best communication between 12 and 15 MHz. There is a good solid Es mode with no multipath, good received signal power, and with probable low noise levels. There is also good received signal power in the 6-11 MHz band; however, the traces show the presence of multiple modes, hence potential fading problems. It is, therefore, not surprising that comm at 13 MHz rated better than at 9 MHz. Obviously, comm at 28 MHz, well above the MOF, would not be expected.

7-28. Figure 7-10 shows another example of the best frequency band being one utilizing Es propagation. The band from 12 to 16 MHz shows high signal level in a low noise band with a single solid mode displayed. The reported comm on 15 MHz was "excellent. "

7-29. Figure 7-11 shows the result of operating too near the E_s MOF. Note the weakening signal above 13 MHz. It is not surprising that communication was weak but readable. Operation in the 6-9 MHz band would be expected to be excellent.

7-30. A similar situation to figure 7-11 is shown in 7-12. Communication on 11228 kHz, near the E_s MOF, would be expected to be weak, while use of frequencies in 7-10 MHz band would produce excellent results with signal levels 30-40 dB higher than at 11 MHz.

7-31. Figure 7-13 shows another type of situation which can occur. Propagation is via F-mode in an ionosphere where the electron content is quite inhomogeneous. This phenomenon is termed "spread F" and can yield a weak, sometimes fast-fading signal. The frequency band from 4 to 7 MHz is obviously the best available, but, as the report at 6 MHz shows, the best leaves something to be desired.

7-32. MANAGING HF CIRCUITS USING CHIRPSOUNDERS

7-33. Efficient frequency management of a set of HF circuits using Chirp sounders, particularly in a tactical military operation can be demanding but yields results

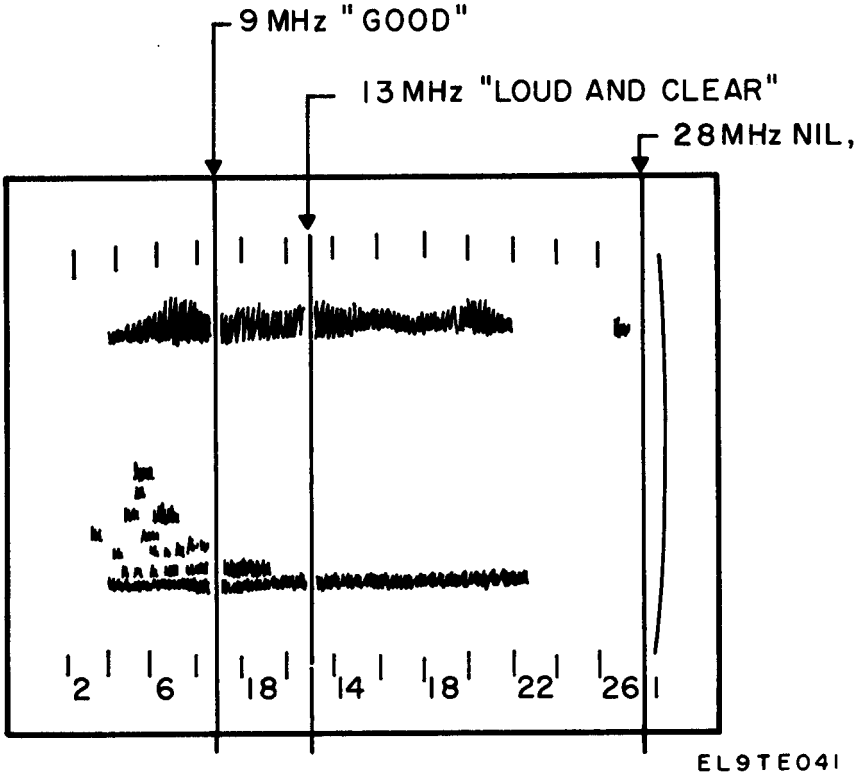


FIGURE 7-9. Example correlating communication quality with Chirpsounder Display.

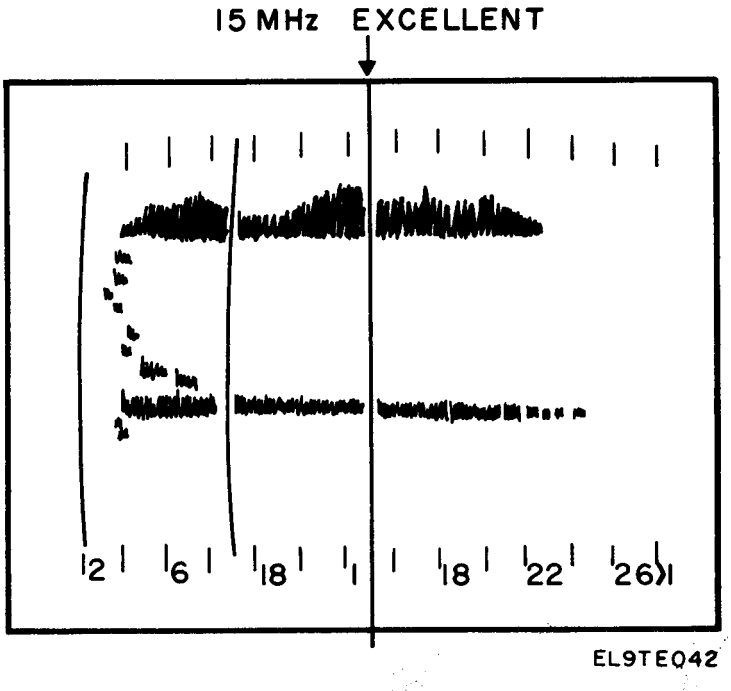


FIGURE 7-10. Example of excellent communication using strong E_s propagation.

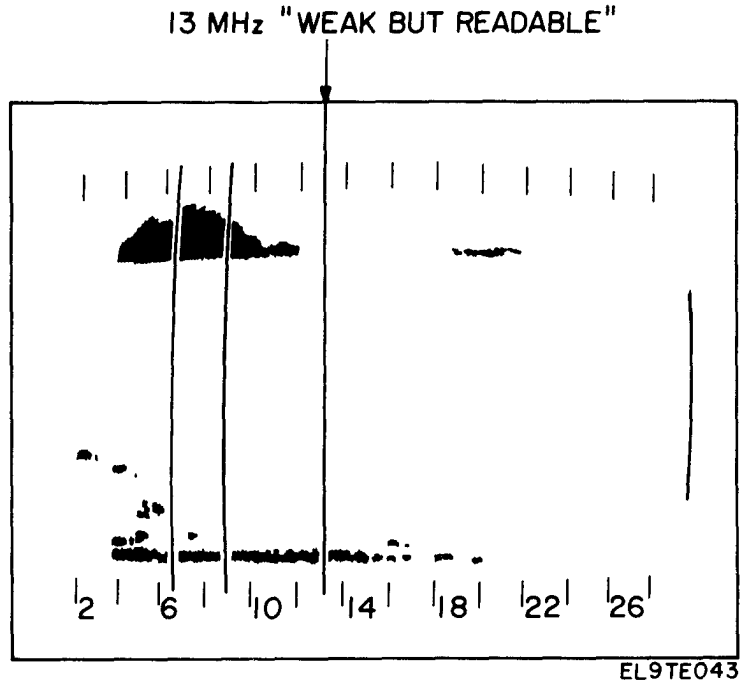


FIGURE 7-11. Example of poor communication using weak E_s propagation.

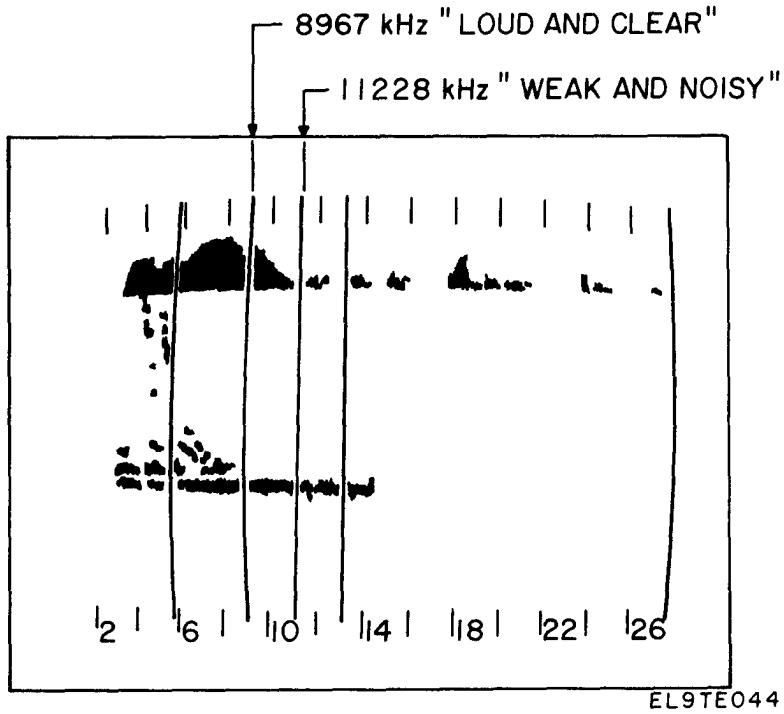


FIGURE 7-12. Example showing correlation of communication quality with Chirpsounder Display.

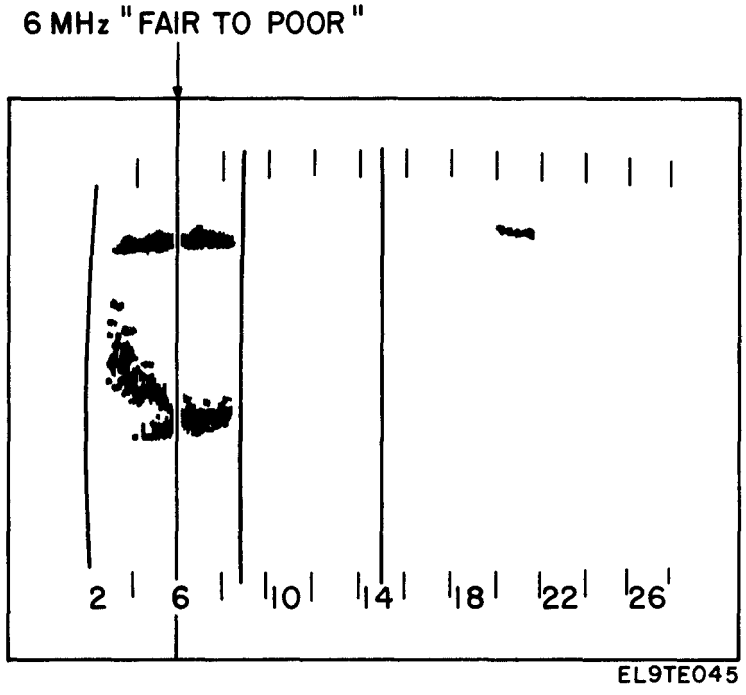


FIGURE 7-13. Example of Communications via Fading Spread F Multipath.

far better than use of traditional methods. It can be limited more by factors such as personnel motivation, communications equipment characteristics, and the complement of assigned frequencies than any frequency management procedures. Such procedures must be tailored to each application, however the following guidelines have been shown by years of field experience to be effective in a variety of situations:

a. The Chirpsounder receiver should be placed at the center of communications control. Up to three paths can be sounded using a single receiver. The (up to) three Chirpsounder transmitters should be colocated with the communications transmitters at the remote sites, and the diplexer feature considered to reduce antenna requirements and to factor antenna patterns into the Chirp sounder measurements.

b. If the RSS-4 Spectrum Monitor is used, it should be colocated with the Chripsounder receiver. If a remote site is over 2000 km away, it is advisable to place an RSS-4 there, also.

c. If more paths are to be frequency-managed than there are Chirpsounder systems available, the sounded paths must be chosen carefully. Experience has shown that propagation conditions from location 1 to locations 2 and 3 are virtually identical (except occasionally for E_s) where 2 and 3 are within 100 km radius of location 1 provided both paths are over land or over sea water. For paths of longer length, azimuth and potential propagation differences become major factors. For example, assume the situation of managing the HF circuits to the six locations surrounding R as shown in figure 7-14 with only 3 Chirpsounder transmitters. Propagation on paths to 1, 2 or 3 should be virtually identical. Circuits to 4 and 5

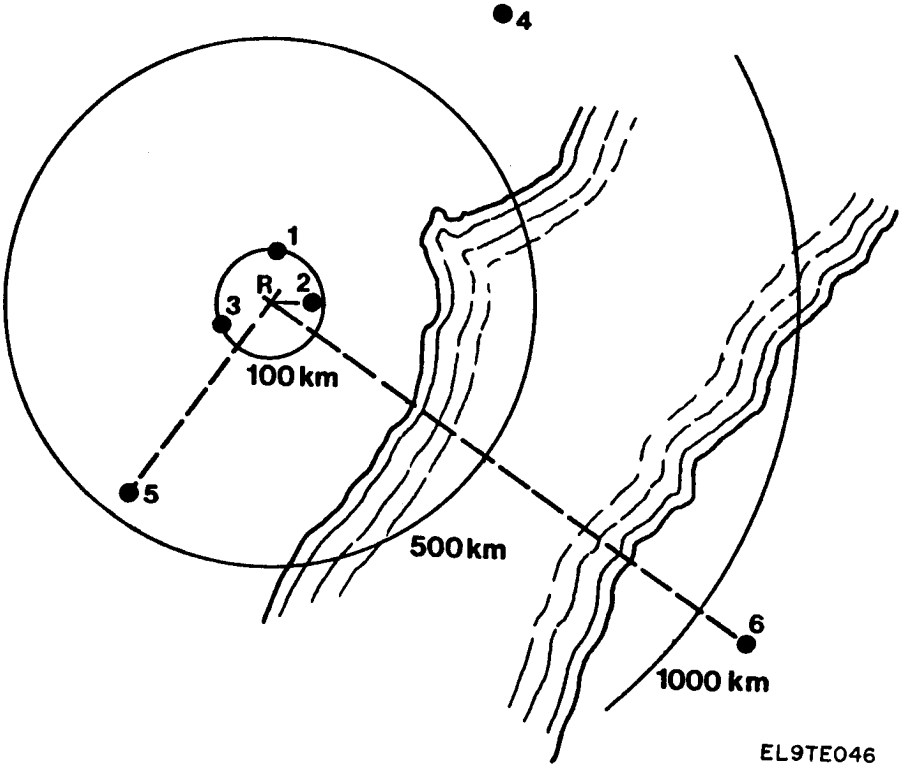


FIGURE 7-14. Hypothetical Six-circuit Network Controlled by Three Sounded Paths.

represent over-land paths, but because path 5-R is slightly shorter, F-mode frequencies propagating well on that path should also be propagating well on 4-R most hours of the day. Path 6-R should also provide an upper bound on F-mode frequencies for 4-R. E_s conditions on 4-R, 5-R, and 6-R can vary substantially, however.

d. Establish the time reference of the Chirp sounder network carefully. Decide which path will be "Path 1" on the RCS-4B, and establish its Chirp sounder sweep start time (e.g. on-the-hour, 1 minute after the hour, etc) relative to an agreed time reference (e.g. a time standard or synchronized watches). There will be less confusion if Paths 2 and 3 are set for sweep start times after Path 1. The start times should be separated by at least 5 seconds, but all should begin within a 20-second interval. When setting up the RCS-4B, it is advisable to start the Path 1 clock as soon as possible as it should then provide the most accurate time reference for synchronization.

e. Automatic Chirpsounder synchronization will be accomplished the easiest by using the full 100-watt output power of the TCS-4B and attempting synchronization during daylight hours. If all path lengths are under 200 km, setting sweep limits of 2-16 MHz should also increase probability of successful automatic signal acquisition and synchronization. Remember that all TCS-4B's being received by one RCS-4B must use the same sweep limits.

f. In setting up network operations, establish procedures for simultaneous changing of sounder sweep limits of the RCS-4B and its associated TCS-4B's if such becomes necessary. often, particularly during daytime or the occurrence of strong E_s, operation of 2-30 MHz sweeps will be desired. However, best nighttime sweep limits will generally be 2-16 MHz.

g. Before setting up the network, all operators should agree on several frequencies (say one in each MHz band from 2-7 MHz for path lengths under 2000 km) which will serve as emergency fallback frequencies in the event of any comm loss of outage in the network. All should agree on a pattern for monitoring these frequencies when required (e.g. monitor the 2-MHz frequency for the first minute of a 5-minute period, the 3-MHz frequency for the second minute, etc). These frequencies should be used under the following conditions:

(1) For any communication within the network before the frequency management system is operational; or

(2) To "bootstrap" the network. (After initial synchronization or an unexpected outage, the RCS-4B site operators transmit the frequency change instructions to start normal network operations on the best propagating emergency channel.)

h. Set up a procedure for regular network contact or "radio checks" even if no traffic is being passed. This can often alert network operators of equipment problems before the equipment fails to pass operational traffic.

i. In setting up operating frequencies for each circuit, the RCS-4B operator should select a primary and an alternate. The alternate channel should be lower in frequency than the primary. The alternate is used if (a) equipment problems preclude tuning to the primary frequency, (b) sudden interference or jamming renders the primary frequency unusable, or (c) a sudden outage catches the network by surprise.

j. When a circuit is operating via the E_s mode, operators at both ends of the circuit should be aware of the situation, an the alternate frequency should be selected from the bank of frequencies propagating via F-mode. Avoid operation within 30% of the E_s MOF.

k. In setting up a duplex circuit, the transmit frequency from the RCS-4B site should always be lower than the receive frequency. In this way, frequency change instructions can be transmitted even with outage in the higher frequency channel.

l. To avoid unnecessary confusion, all operators should agree on a procedure for frequency changing that accounts for possible tuning problems. For example, allow a set maximum time limit to establish contact on a new frequency. If contact is not made, agree to return to the old frequency to assess the situation. If contact cannot be re-established on the old frequency after another set period of time, agree to go to the alternate frequency. If that fails also, then a pattern for monitoring the emergency frequencies should be used.

m. If the RCS-4B shows a frequency to be propagating and no contact can be made, the cause will nearly always be found to be a comm equipment problem or improper tuning. Remember that the Chirpsounder transmitter and receiver represent a separate propagation "test set." If the sounder system operates on different antennas than the communications system, there will be some disparity in path loss between the two systems, but this will invariably be insufficient to cause a misreading as to which assigned frequencies are propagating. (In fact, the opposite is generally true: the usually higher power communications systems can operate marginally over a greater frequency range than the sounder system indicates.)

n. The RCS-4B operator should anticipate potential frequency changes well before they become necessary. This is particularly true if an RSS-4 Spectrum Monitor is unavailable for clear channel search. Candidate new frequencies should be monitored as long as possible to determine if potential interference exists. Frequency changes should be made in advance of potential outages and not just before total outage is imminent.

o. Care should be taken in extrapolating propagation conditions on a sounded circuit to an unsounded one. The differences in path length and azimuth (particularly east vs west), and the potential propagation differences that result, must be taken into account. Figure 7-15 can be used as a guide for extrapolating the effects of range on the 1-hop F-mode MOF by taking the ratio of factors shown for ranges of interest. For example, a daytime MOF on a 600-km circuit is measured at 9 MHz, and it is desired to estimate the MOF for a 900-km circuit. From figure 7-15, the extrapolation factors are 1.5 for 600 km and 2.0 for 900 km. The resulting estimated MOF is $\frac{2.0}{1.5}$ x 9 or 12 MHz. In making such estimates keep in mind MOF's for circuits to the west of the RCS-4B site will lag behind those observed to the east. Also, avoid extrapolating Es conditions from sounded paths to unsounded paths unless (a) the Es is clearly widespread and strongly established and (b) good fallback procedures exist in case of sudden outage. In such cases, the upper curve in figure 7-15 can be used as a conservative guide for estimating E_s MOF extrapolations.

7-34. Experience has shown that successful frequency management of a large number of HF circuits is rather easily attained provided:

a. As many of the circuits are sounded as possible, and the sounded circuits are carefully selected;

b. Care is taken in spectrum monitoring for clear channels by using the RSS-4 Spectrum Monitor;

c. A sufficiently large list of potentially usable channels exist (the more, the better); and

d. Procedures for coping with frequency changes and unexpected loss of communication are clearly understood and followed.

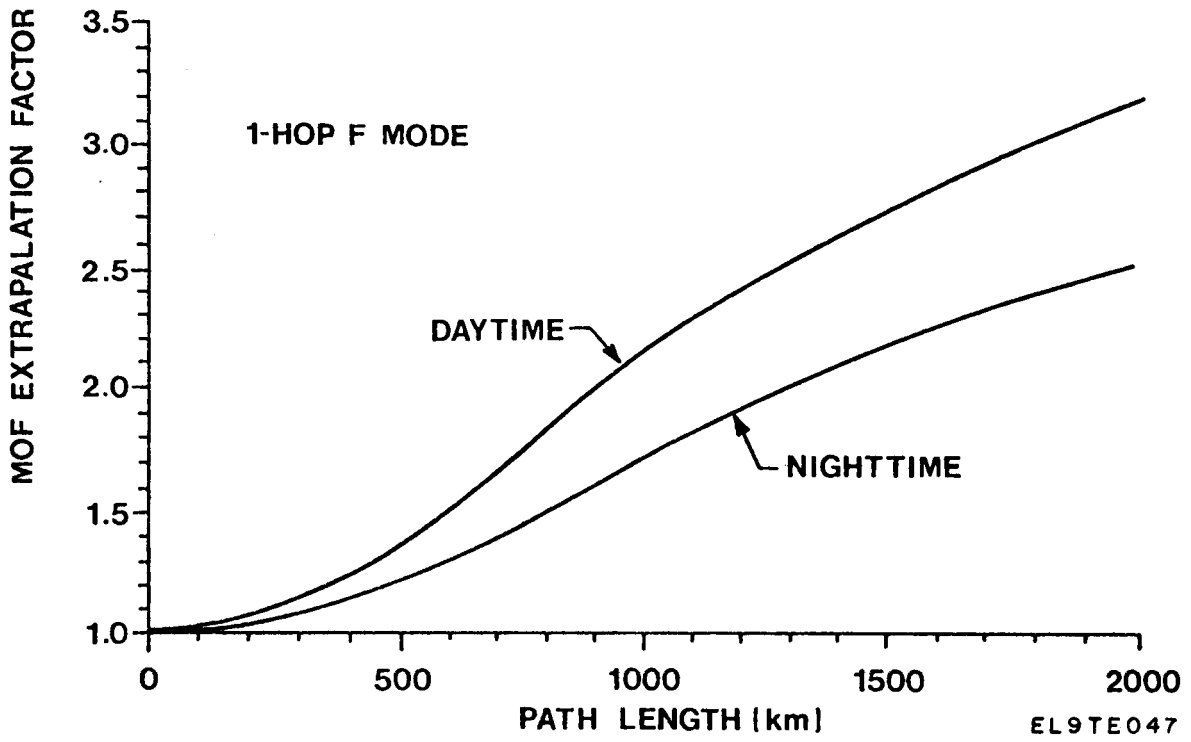


FIGURE 7-15. Factors for Extrapolating Maximum Observed One-hop F-mode Frequencies.

APPENDIX A
REFERENCES

DA Pam 310-1	Consolidated Index of Army Publications and Blank Forms.
DA Pam 738-750	The Army Maintenance Management System (TAMMS).
TB SIG 291	Safety Measures to be Observed When Installing and Using Whip Antennas, Field Type Masts, Towers, Antennas and Metal poles that are used with Communications Radar and Direction-Finder Equipment.
TM 11-5820-884-13	Operator's, Organizational, and Direct Support Maintenance Manual for Spectrum Monitor Model RSS-4, Radio Receiver R-2093/TRQ-35(V) (NSN 5820-01-038-9119) .
TM 11-5820-884-23P	Organizational and Direct Support Maintenance Repair Parts and Special Tools List for Spectrum Monitor Model RSS-4 (Radio Receiver R-2093/TRQ-35(V)) (NSN 5820-01-038-9119).
TM 11-5820-918-13	Operator's, Organizational, and Direct Support Maintenance Manual for Radio Transmitter (T-1373/TRQ-35(v)) Model TSC-4B (NSN 5820-01-005-4248).
TM 11-5820-917-23P	Organizational and Direct Support Maintenance Repair Parts and Special Tools List for Radio Receiver Model RCS-4B (R-2081/TRQ-35(V)) (NSN 5820-01-005-4247).
TM 11-5820-918-23P	Organizational and Direct Support Maintenance Repair Parts and Special Tools List for Radio Transmitter Model TSC-4B (T-1373/TRQ-35(V)) (NSN 5820-01-005-4248).
TM 11-5985-371-12HR	Hand Receipt Manual Covering Contents of Components of End Item (COEI) and Additional Authorization List (AAL) for Antenna AS-3577/GRC (NSN 5985-01-148-1778).
TM 11-5985-371-12&P	Operator's and Organizational Maintenance Manual (Including Repair Parts and Special Tools List) for Antenna AS-3577/GRC (NSN 5985-01-148-1778).

TM 11-6625-2952-24P	Organizational, Direct Support and General Support Maintenance Repair Parts and Special Tools List for Signal Generator SG-1171/U (NSN 6625-01-133-6160).
TM 11-6625-3051-12	Operator's and Organizational Maintenance for Signal Generator SG-1171/U (NSN 6625-01-133-6160).
TM 11-6625-3051-40	General Support Maintenance for Signal Generator SG-1171/U (NSN 6625-01-133-6160).
TM 11-6625-3136-12	Operator's and Organizational Maintenance for Spectrum Analyzer AN/USM-489(V)1 (NSN 6625-01-079-9495).
TM 11-6625-3136-24P	Organizational, Direct Support and General Support Maintenance Repair Parts and Special Tools List for Spectrum Analyzer AN/USM-489(V)1 (NSN 6625-01-079-9495).
TM 11-6625-3136-40	General Support Maintenance for Spectrum Analyzer AN/USM-489(V)1 (NSN 6625-01-079-9495).
TM 750-244-2	Procedures for Destruction of Electronics Materiel to Prevent Enemy Use (Electronics Command).

APPENDIX B
MAINTENANCE ALLOCATION

Section I. INTRODUCTION

B-1 General

This appendix provides a summary of the maintenance operations for the R-2081/TRQ-35(V). It authorizes categories of maintenance for specific maintenance functions on repairable items and components and the tools and equipment required to perform each function. This appendix may be used as an aid in planning maintenance operations.

B-2 Maintenance Function

Maintenance functions will be limited to and defined as follows:

a. Inspect. To determine the serviceability of an item by comparing its–physical, mechanical, and/or electrical characteristics with established standards through examination.

b. Test. To verify serviceability and to detect incipient failure by measuring mechanical or electrical characteristics of. an item and comparing those characteristics with prescribed standards.

c. Service. Operations required periodically to keep an item in proper operating condition, i.e., to clean (decontaminate), to preserve, to drain, to paint, or to replenish fuel, lubricants, hydraulic fluids, or compressed air supplies.

d. Adjust. To maintain, within prescribed limits, by bringing into proper or exact position, or by setting the operating characteristics to the specified parameters.

e. Align. To adjust specified variable elements of an item to bring about optimum or desired performance.

f. Calibrate. To determine and cause corrections to be made or to be adjusted on instruments or test measuring and diagnostic equipments used in precision measurement. Consists of comparisons of two instruments, one of which is a certified standard of known accuracy, to detect and adjust any discrepancy in the accuracy of the instrument being compared.

g. Install. The act of emplacing, seating, or fixing into position an item, part, module (component or assembly) in a manner to allow the proper functioning of the equipment or system.

h. Replace. The act of substituting a serviceable like type part, subassembly, or module (component or assembly) for an unserviceable counterpart.

i. Repair. The application of maintenance services (inspect, test, service, adjust, align, calibrate, replace) or other maintenance actions (welding, grinding, riveting, straightening, facing, remachining, or re-surfacing) to restore serviceability to an item by correcting specific damage, fault, malfunction, or failure in a part, subassembly, module (component or assembly), end iterm, or system.

j. Overhaul. That maintenance effort (service/action) necessary to restore an item to a completely serviceable/operational condition as prescribed by maintenance standards (i.e., DMWR) in appropriate technical publications. Overhaul is normally the highest degree of maintenance performed by the Army. Overhaul does not normally return an item to like new condition.

k. Rebuild. Consists of those services/actions necessary for the restoration of unserviceable equipment to a like new condition in accordance with original manufacturing standards. Rebuild is the highest degree of materiel maintenance applied to Army equipment. The rebuild operation includes the act of returning to zero those age measurements (hours, miles, etc.) considered in classifying Army equipments/components.

B-3 Column Entries

a. Column 1, Group Number. Column 1 lists group numbers, the purpose of which is to identify components, assemblies, subassemblies, and modules with the next higher assembly.

b. Column 2, Component/Assembly. Column 2 contains the noun names of components, assemblies, subassemblies, and modules for which maintenance is authorized.

c. Column 3, Maintenance Functions. Column 3 lists the functions to be performed on the item listed in column 2. When items are listed without maintenance functions, it is solely for purpose of having the group numbers in the MAC and RPSTL coincide,

d. Column 4, Maintenance Category. Column 4 specifies, by the listing–of a “work time” figure in the appropriate subcolumn(s), the lowest level of maintenance authorized to perform the function listed in column 3. This figure represents the active time required to perform that maintenance function at the indicated category of maintenance. If the number or complexity of the tasks within the listed maintenance function vary at different maintenance categories, appropriate “work time” figures will be shown for each category. The number of task-hours specified by the ’’work time” figure represents the average time required to restore an item (assembly, subassembly, component, module, end item or system) to a serviceable condition under typical field operating conditions. This time includes preparation time, troubleshooting time, and quality assurance/quality control time in addition to the time required to perform the specific tasks identified for the maintenance functions authorized in the maintenance allocation chart. Subcolumns of column 4 are as follows:

C- Operator/Crew

O- Organizational

F - Direct Support

H - General Support

D - Depot

e. Column 5, Tools and Equipment. Column 5 specifies by code, those common tool sets not individual tools) and special tools, test, and support equipment required to perform the designated function.

f. Column 6, Remarks. Column 6 contains an alphabetic code which leads to the remark in section IV, Remarks, which is pertinent to the item opposite the particular code.

B-4. Tool and Test Equipment Requirements (Sect. III)

a. Tool or Test Equipment Reference Code. The numbers in this column coincide with the numbers used in the tools and equipment column of the MAC. The numbers indicate the applicable tool or test equipment for the maintenance functions.

b. Maintenance Category. The codes in this column indicate the maintenance category allocated the tool or test equipment.

c. Nomenclature. This column lists the noun name and nomenclature of the tools and test equipment required to perform the maintenance functions.

d. National/NATO Stock Number. This column lists the National/NATO stock number of the specific tool or test equipment.

e. Tool Number. This column lists the manufacturer's part number of the tool followed by the Federal Supply Code for manufacturers (5-digit) in parentheses.

B-5. Remarks (Sect. IV)

a. Reference Code. This code refers to the appropriate item in section II, column 6.

b. Remarks. This column provides the required explanatory information necessary to clarify items appearing in section II.

(Next printed page is B-4)

SECTION II MAINTENANCE ALLOCATION CHART
FOR
RADIO, RECEIVER R-2081/TRQ-35(V)

(1) GROUP NUMBER	(2) COMPONENT/ASSEMBLY	(3) MAINTENANCE FUNCTION	(4) MAINTENANCE CATEGORY C	O	F	H	D	(5) TOOLS AND EQPT.	(6) REMARKS
00	RADIO, RECEIVER R-2081 /TRQ-35(V)	Inspect		0.2				1	B
		Test			2.0			2,3,4,5	
		Repair			2.0				
		Adjust					3.0	2 thru 14	
01	RECEIVER, CHIRPSOUNDER RCS-4B P/N 9125-1100	Inspect		0.2				1	
		Repair			2.5			2,3	
0101	CONTROL/DISPLAY P/N 6025-1000	Inspect			0.1				
		Repair			1.5			2,3	
010101	SPECTRUM ANALYZER ASSY P/N 6025-1001	Inspect			0.2			2,3	
		Repl			1.0			2,3	
		Repair					4.0		A
010102	DISPLAY LOGIC ASSY P/N 6025-1002	Inspect			0.2			2,3	
		Replace			1.0			2,3	
		Repair					4.0		A
010103	DISPLAY MEMORY ASSY P/N 6025-1003	Inspect			0.2			2,3	
		Replace			1.0			2,3	
		Repair					4.0		A
010104	THREE PATH CONTROLLER ASSY P/N 6025-1004	Inspect			0.2			2,3	
		Replace			1.0			2,3	
		Repair					4.0		A
010105	AUTO SYNC/TEST ASSY P/N 6025-1005	Inspect			0.2			2,3	
		Replace			1.0			2,3	
		Repair					4.0		A
010106	FREQUENCY STANDARD ASSY P/N 6025-1006	Inspect			0.2			2,3	
		Replace			1.0			2,3	
		Repair					4.0		A
010107	CRT DISPLAY ASSY P/N 6025-1007	Inspect			0.2			2,3	
		Replace			1.0			2,3	
		Repair					4.0		A
010108	BATTERY SUPPLY ASSY P/N 6025-1008	Inspect			0.2			2,3	
		Replace			1.0			2,3	
		Repair					4.0		A
010109	NUMERIC DISPLAY ASSY P/N 6025-1009	Inspect			0.2			2,3	
		Replace			1.0			2,3	
		Repair					4.0		A
010110	SUB PANEL CONTROLL ASSY P/N 6025-1010	Inspect			0.2			2,3	
		Repair			1.5			2,3	
010111	ENCLOSURE ASSY P/N 6025-1011	Inspect			0.2			2,3	
		Repair			1.5			2,3	C
0102	HF RECEIVER P/N 4028-1100	Inspect			0.2			2,3	
		Repair			2.0			2,3	
010201	SWEEP SYNTHESIZER ASSY P/N 5030-1101	Inspect			0.2			2,3	
		Replace			1.0			2,3	
		Repair					4.0		A
010202	RECEIVER ASSY P/N 4028-1002	Inspect			0.2			2,3	
		Replace			1.0			2,3	
		Repair					4.0		A
010203	40-70 MHZ ASSY P/N 4028-1007	Inspect			0.2			2,3,4	
		Replace			1.0			2,3	
		Repair					4.0		A
010204	ENCLOSURE ASSY P/N 4028-1003	Inspect			0.2			2,3,4	
		Repair			2.5			2,3	C
02	POWER DIVIDER P/N 6043-1000	Inspect			0.2			2,3,4	
		Repair			1.5			2,3	
03	ENCLOSURE ASSY P/N 6000-3110-01	Inspect			0.2			2,3,4	C
		Repair			1.0			2,3	
04	CABLE ASSEMBLIES	Inspect			0.2			2,3,4	
		Repair			2.0			2,3	

SECTION III TOOL AND TEST EQUIPMENT REQUIREMENTS
FOR

RADIO, RECEIVER R-2081/TRQ-35(V)

TOOL OR TEST EQUIPMENT REF CODE	MAINTENANCE CATEGORY	NOMENCLATURE	NATIONAL/NATO STOCK NUMBER	TOOL NUMBER
1	O	TOOL KIT, ELECTRICAL EQUIPMENT TK-101/G	5180-00-064-5178	
2	F,D	TOOL KIT, ELECTRICAL EQUIPMENT TK-100/G	5180-00-605-0079	
3	F,D	TOOL KIT, ELECTRICAL EQUIPMENT TK-105/G	5180-00-610-8177	
4	F,D	MULTIMETER, DIGITAL AN/PSM-45	6625-01-139-2512	
5	F,D	OSCILLOSCOPE OS-261C(V)1/U	6625-01-119-7314	
6	D	ELECTRONIC COUNTER AN/USM-459	6625-01-061-8928	
7	D	SPECTRUM ANALYZER IP-1216(P)	6625-00-424-4370	
8	D	PLUG IN PL-1388/U } OR	6625-00-431-9339	
9	D	PLUG IN PL-1399/U	6625-00-432-5055	
	D	SPECTRUM ANALYZER AN/USM-489(V)	6625-01-079-9495	
10	D	TEST OSCILLATOR SG-1128/U } OR	6625-00-450-7590	
	D	GENERATOR, SIGNAL FUNCTION SG-1171( )/U	6625-01-133-6160	
11	D	ATTENUATOR, VARIABLE	5820-00-251-6924	
12	D	MIXER (WATKINS JOHNSON)	5985-00-087-2547	
13	D	ATTENUATOR	5985-00-572-7428	
14	D	TERMINATION	5985-00-968-3231	

SECTION IV. REMARKS

RADIO, RECEIVER R-2081/TRQ-35(V)

REFERENCE CODE	REMARKS
A	ASSEMBLIES RETURNED TO THE AIR FORCE FOR REPAIR.
B	OPERATIONAL TEST USING BUILT-IN TEST FUNCTION.
C	REPAIR BY REPLACEMENT OF CONNECTORS, LAMPS, FUSES, ETC.

APPENDIX C

COMPONENTS OF END ITEM LIST

Section I. INTRODUCTION

C-1. Scope

This appendix lists integral components of and basic issue items for the R-2081/TRQ-35(V) to help you inventory items required for safe and efficient operation.

C-2. General

This Components of End Item List is divided into the following sections:

a. Section II. Integral Components of the End Item. These items, when assembled, comprise the R-2081/TRQ-35(V) and must accompany it whenever it is transferred or turned in. The illustrations will help you identify these items.

b. Section III. Basic Issue Items. Not applicable.

C-3. Explanation of Columns

a. Illustration. This column is divided as follows:

(1) Figure number. Indicates the figure number of the illustration on which the item is shown.

(2) Item number. The number used to identify item called out in the illustration.

b. National Stock Number. Indicates the National stock number assigned to the item and which will be used for requisitioning.

c. Part Number. Indicates the primary number used by the manufacturer, which controls the design and characteristics of the item by means of its engineering drawings, specifications, standards, and inspection requirements to identify an item or range of items. Following the part number, the Federal Supply Code for Manufacturers (FSCM) is shown in parentheses.

d. Description. Indicates the Federal item name and, if required, a minimum description to identify the item.

e. Location. The physical location of each item listed is given in this column. The lists are designed to inventory all items in one area of the major item before moving on to an adjacent area.

f. Usable on Code. Not applicable.

g. Quantity Required (Qty Reqd). This column lists the quantity of each item required for a complete major item.

h. Quantity. This column is left blank for use during an inventory. Under the Rcvd column, list the quantity you actually receive on your major item. The Date columns are for your use when you inventory the major item at a later date; such as for shipment to another site.

(Next printed page is C-3)

SECTION II INTEGRAL COMPONENTS OF END ITEM

(A) FIG NO.	(B) ITEM NO.	(2) NATIONAL STOCK NUMBER	(3) DESCRIPTION PART NUMBER (FSCM)	(4) LOCATION	(5) USABLE ON CODE	(6) QTY REQD	(7) QUANTITY RCVD	DATE
	1	5820-01-005-4247	RADIO RECEIVER			1		

APPENDIX D

ADDITIONAL AUTHORIZATION LIST

Section I. INTRODUCTION

D-1. Scope

This appendix lists additional items you are authorized for the support of the R-2081/TRQ-35(V).

D-2. General

This list identifies items that do not have to accompany the R-2081/TRQ35(V) and that do not have to be turned in with it. These items are all authorized to you by CTA, MTOE, TDA, or JTA.

D-3. Explanation of Listing

National stock numbers, descriptions, and quantities are provided to help you identify and request the additional items you require to support this equipment. The items are listed in alphabetical sequence by item name under the type document (i.e., CTA, MTOE, TDA, or JTA) which authorizes the item(s) to you.

(Next printed page is D-2)

SECTION II ADDITIONAL AUTHORIZATION LIST

(1) NATIONAL STOCK NUMBER	(2) DESCRIPTION PART NUMBER AND FSCM	USABLE ON CODE	(3) UNIT OF MEAS	(4) QTY AUTH
5985-01-148-1778	ANTENNA AS-3577/GRC		EA	1
5820-01-038-9119	SPECTRUM MONITOR (RADIO RECEIVER), R-2093/TRQ-35(V)		EA	1
5820-01-005-4248	RADIO TRANSMITTER, T-1373		EA	1

RECOMMENDED CHANGES TO EQUIPMENT TECHNICAL PUBLICATIONS

SOMETHING WRONG WITH THIS PUBLICATION?

FROM: (PRINT YOUR UNIT'S COMPLETE ADDRESS)
Commander
Stateside Army Depot
ATTN: AMSTA-US
Stateside, N.J. 07703-5007

DATE SENT
10 July 1975

PUBLICATION NUMBER	PUBLICATION DATE	PUBLICATION TITLE
TM 11-5840-340-12	23 Jan 74	Radar Set AN/PRC-76

BE EXACT. . .PIN-POINT WHERE IT IS

PAGE NO	PARA-GRAPH	FIGURE NO	TABLE NO	IN THIS SPACE TELL WHAT IS WRONG AND WHAT SHOULD BE DONE ABOUT IT:
2-25	2-28			Recommend that the installation antenna alignment procedure be changed throughout to specify a 2° IFF antenna lag rather than 1°. REASON: Experience has shown that with only a 1° lag, the antenna servo system is too sensitive to wind gusting in excess of 25 knots, and has a tendency to rapidly accelerate and decelerate as it hunts, causing strain to the drive train. Hunting is minimized by adjusting the lag to 2° without degradation of operation.
3-10	3-3		3-1	Item 5, Function column. Change "2 db" to "3db." REASON: The adjustment procedure for the TRANS POWER FAULT indicator calls for a 3 db (500 watts) adjustment to light the TRANS POWER FAULT indicator.
5-6	5-8			Add new step f.1 to read, "Replace cover plate removed in step e.1, above." REASON: To replace the cover plate.
		FO3		Zone C 3. On J1-2, change "+24 VDC to "+5 VDC." REASON: This is the output line of the 5 VDC power supply. +24 VDC is the input voltage.

SAMPLE

PRINTED NAME, GRADE OR TITLE, AND TELEPHONE NUMBER
SSG I. M. DeSpiritof 999-1776

SIGN HERE
I. M. DeSpiritof

DA FORM 1 JUL 79 2028-2

PREVIOUS EDITIONS ARE OBSOLETE.

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US Army Communications-Electronics Command
and Fort Monmouth
ATTN: AMSEL-ME-MP
Fort Monmouth, New Jersey 07703-5007

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DATE SENT

PUBLICATION NUMBER	PUBLICATION DATE	PUBLICATION TITLE
TM 11-5820-917-13	30 Aug 1985	Radio Receiver R-2081/TRQ-35(V)

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PAGE NO.	PARA-GRAPH	FIGURE NO.	TABLE NO.

IN THIS SPACE TELL WHAT IS WRONG AND WHAT SHOULD BE DONE ABOUT IT:

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TM 11-5820-917-13	30 Aug 1985	Radio Receiver R-2081/TRQ-35(V)

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FROM: (PRINT YOUR UNIT'S COMPLETE ADDRESS

DATE SENT

PUBLICATION NUMBER	PUBLICATION DATE	PUBLICATION TITLE
TM 11-5820-917-13	30 Aug 85	Radio Receiver R-2081/TRQ-35(V)

BE EXACT PIN-POINT WHERE IT IS

PAGE NO.	PARAGRAPH	FIGURE NO.	TABLE NO.

IN THIS SPACE TELL WHAT IS WRONG AND WHAT SHOULD BE DONE ABOUT IT:

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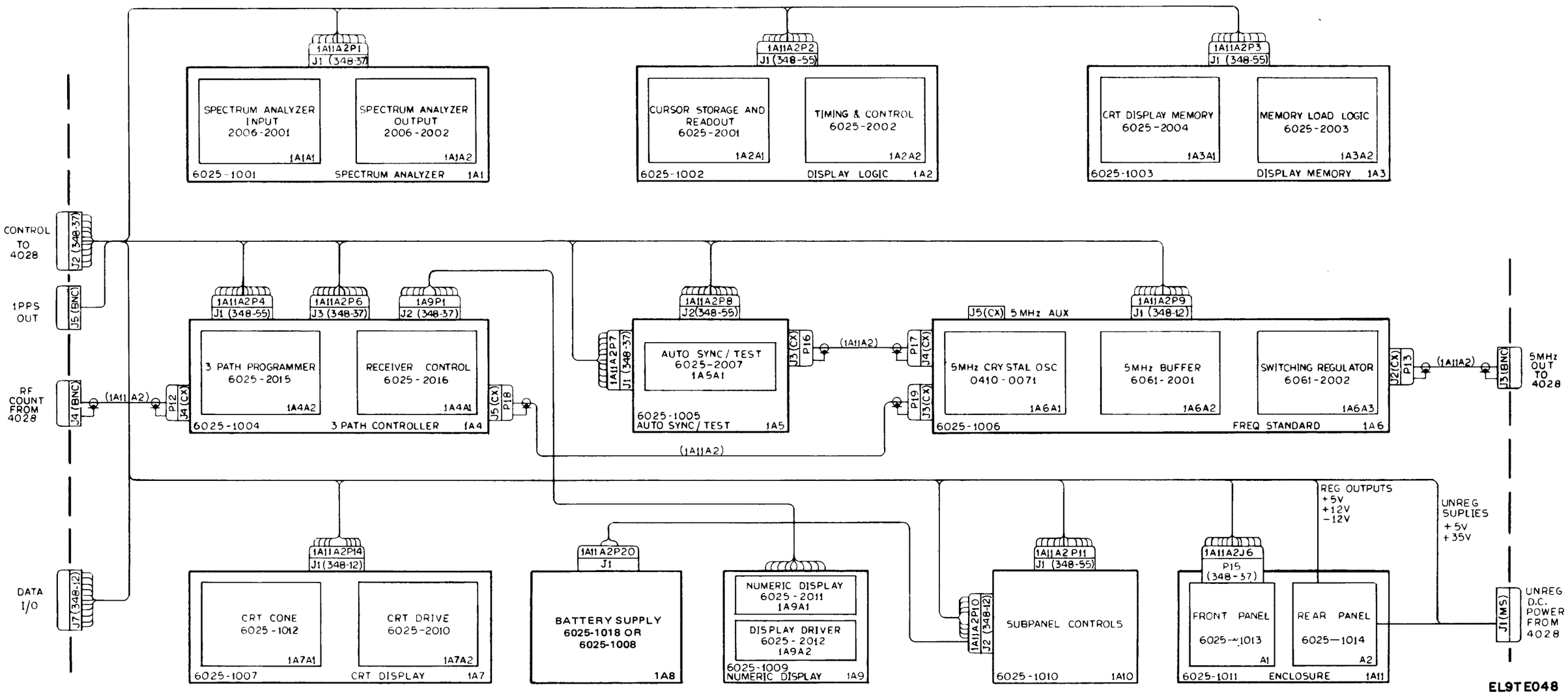
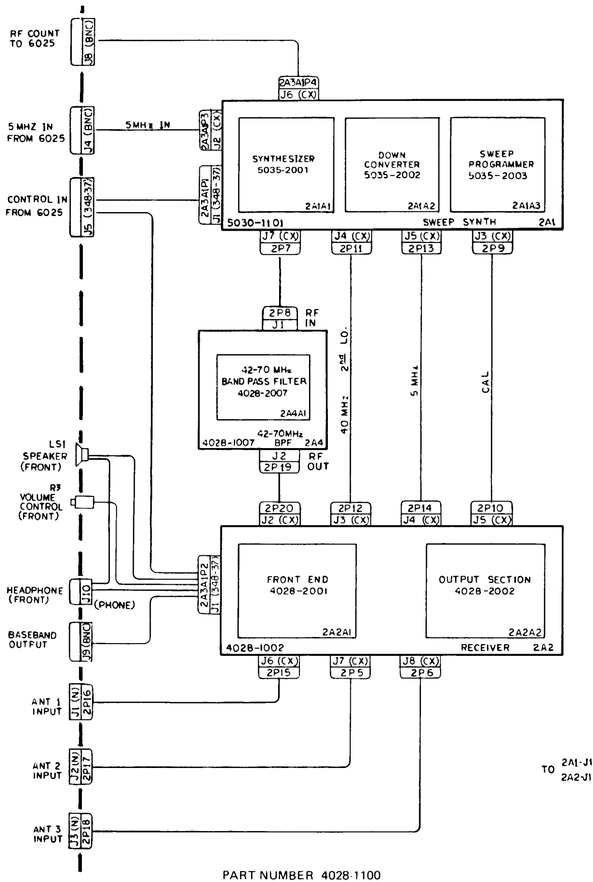
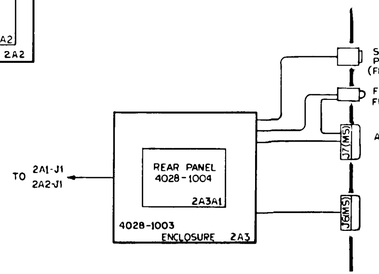


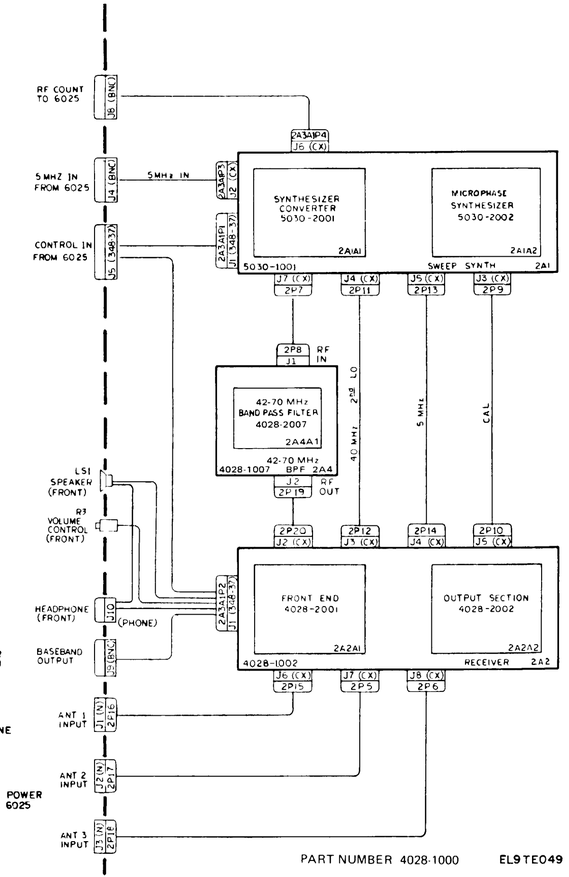
FIGURE FO-1. Block Diagram, 6025 Unit 1.



PART NUMBER 4028-1100



PART NUMBERS 4028-1000 and 4028-1100



PART NUMBER 4028-1000 EL9TE049

FIGURE FO-2. Block Diagram, 4028 Unit 2 (P/N 4028-1000 or 4028-1100).

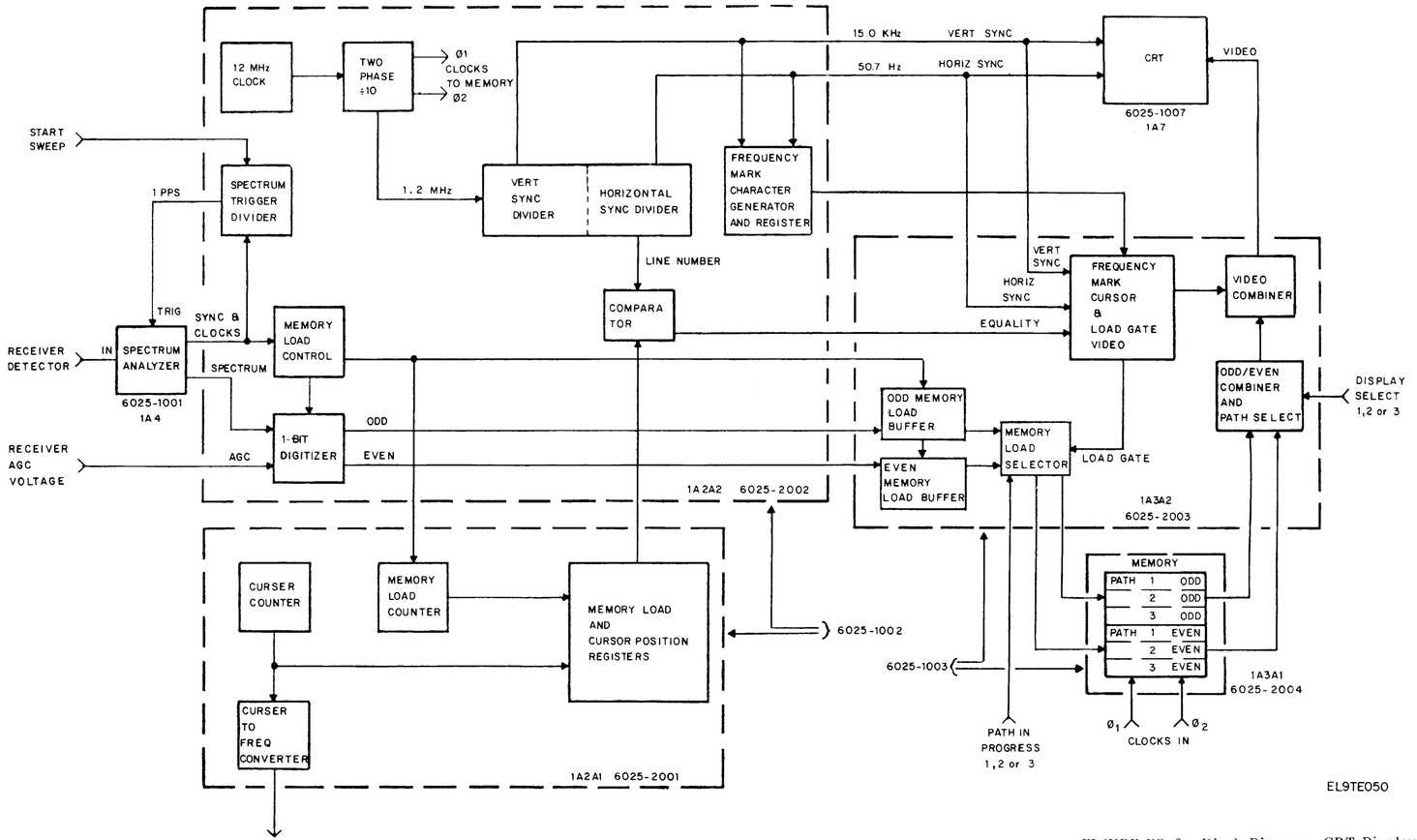


FIGURE FO-3. Block Diagram, CRT Display.

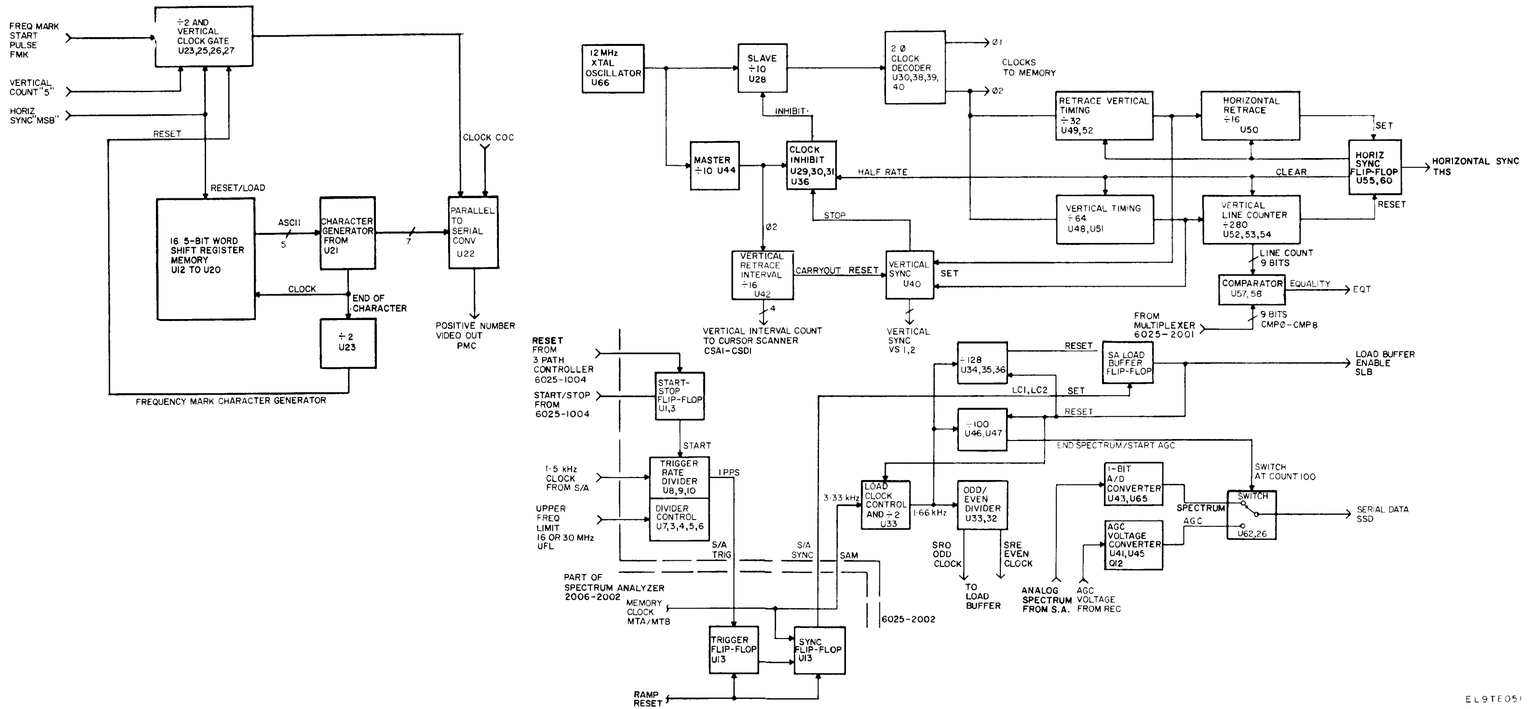


FIGURE FO-4. Block Diagram, Timing and Control 1A2A2.

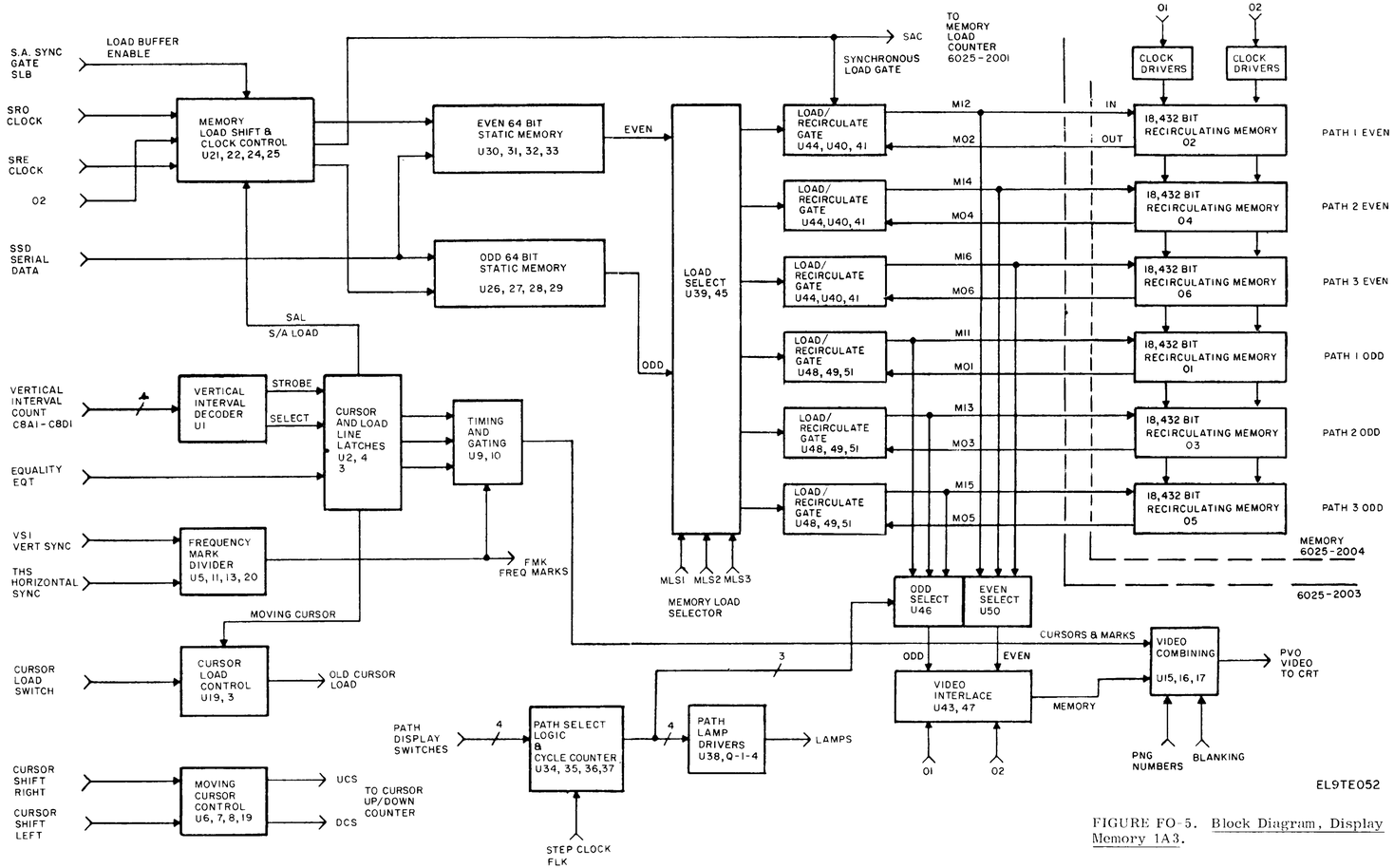
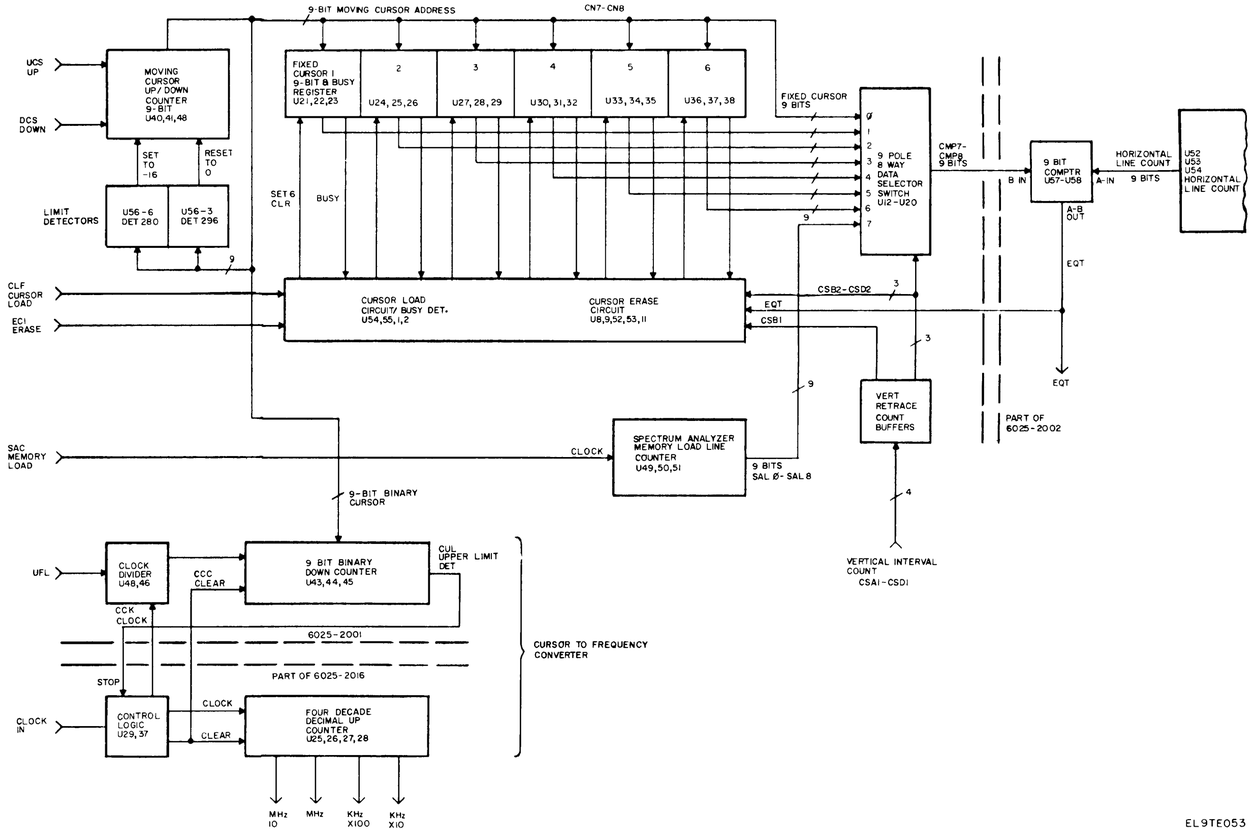
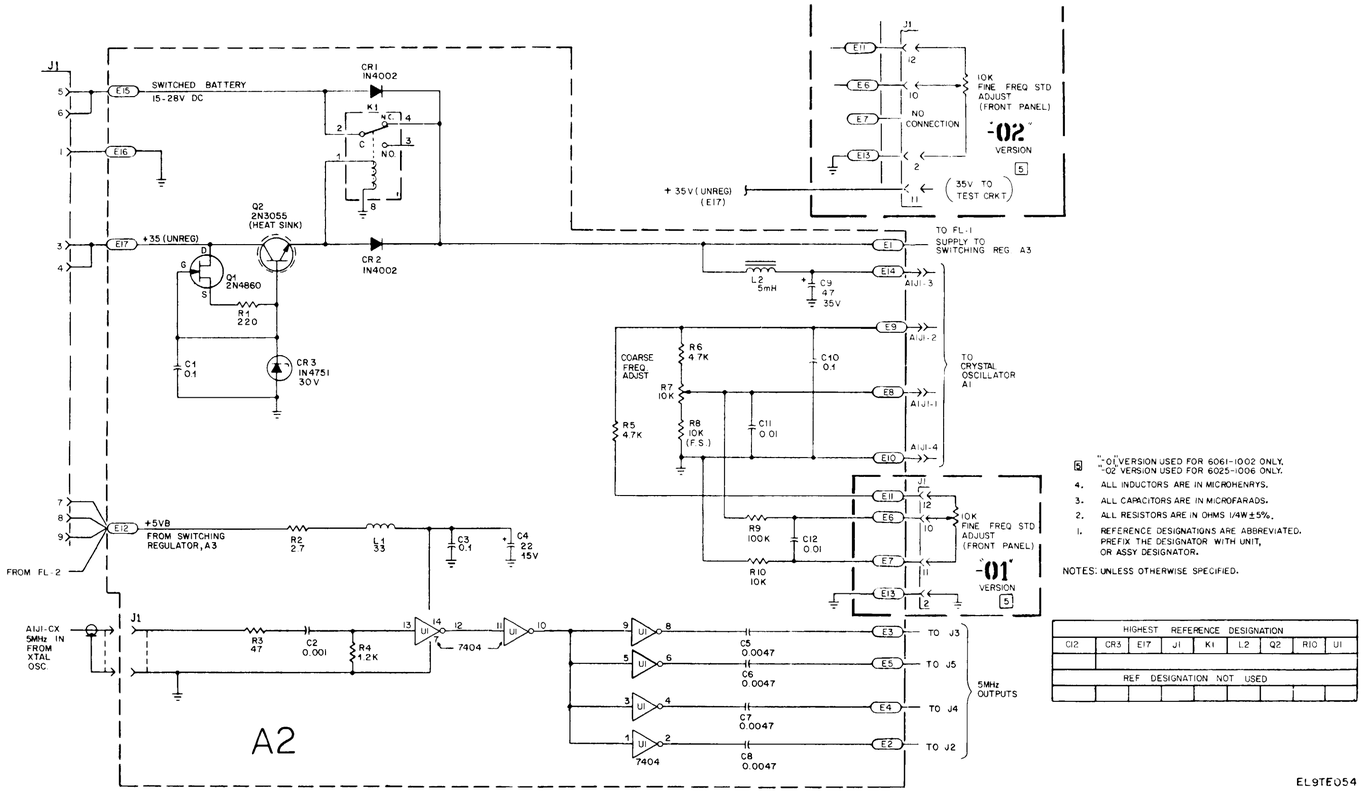


FIGURE FO-5. Block Diagram, Display Memory 1A3.



EL9TE053

FIGURE FO-6. Block Diagram, Cursor Storage and Readout 1A2A1.



HIGHEST REFERENCE DESIGNATION								
C12	CR3	E17	J1	K1	L2	Q2	R10	U1
REF DESIGNATION NOT USED								

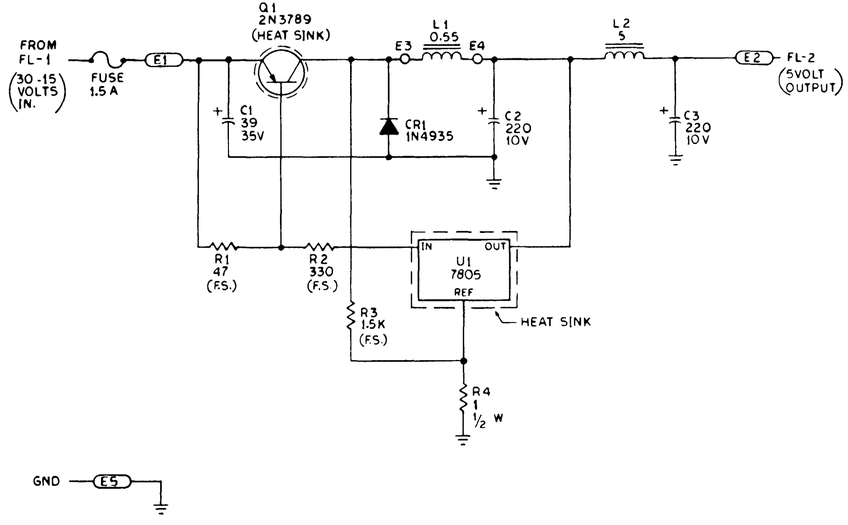
[2] "-01" VERSION USED FOR 6061-1002 ONLY.
"-02" VERSION USED FOR 6025-1006 ONLY.

4. ALL INDUCTORS ARE IN MICROHENRYS.
3. ALL CAPACITORS ARE IN MICROFARADS.
2. ALL RESISTORS ARE IN OHMS 1/4W±5%.
1. REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX THE DESIGNATOR WITH UNIT, OR ASSY DESIGNATOR.

NOTES: UNLESS OTHERWISE SPECIFIED.

EL9TE054

FIGURE FO-7. Schematic Diagram, 5 MHz Buffer (6061-2001) (S/N 400101 and on).



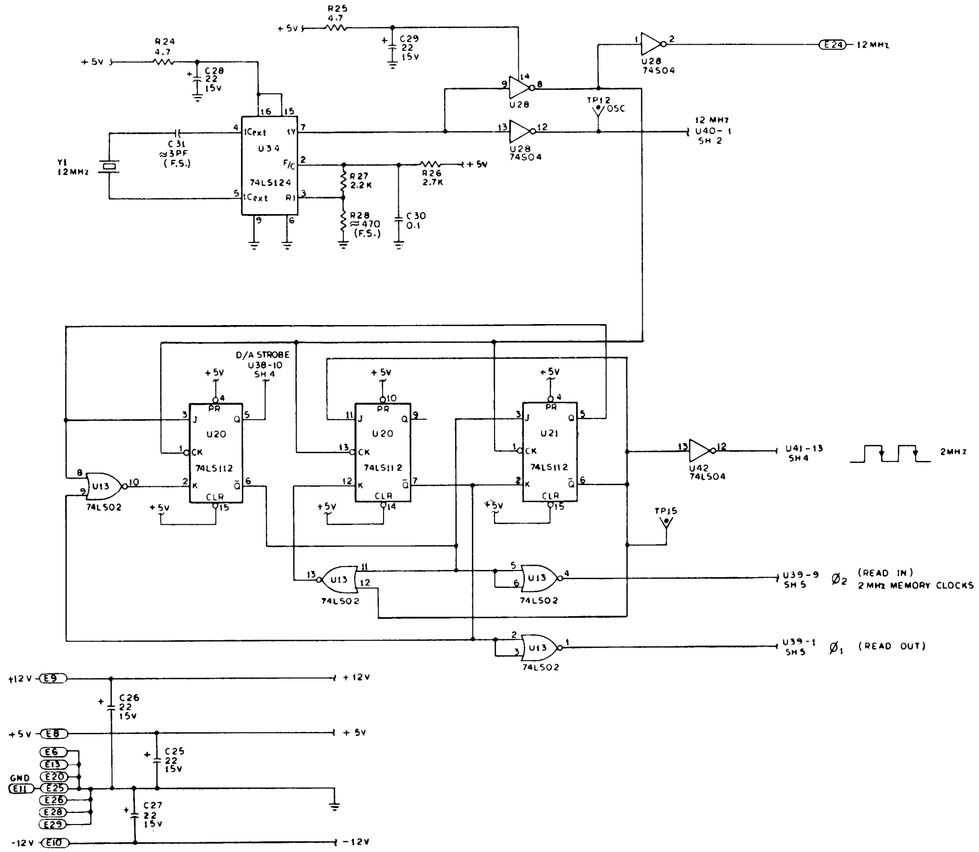
4. ALL INDUCTORS ARE IN MILLIHENRYS.
3. ALL CAPACITORS ARE IN MICROFARADS.
2. ALL RESISTORS ARE IN OHMS 1/4W ±5%.
1. REFERENC DESIGNATIONS ARE ABBREVIATED PREFIX THE DESIGNATOR WITH UNIT, OR ASSY DESIGNATOR.

NOTES: UNLESS OTHERWISE SPECIFIED.

HIGHEST REFERENCE DESIGNATION							
C3	CR1	E5	L2	Q1	R4	U1	
REF DESIGNATION NOT USED							

EL9TE055

FIGURE FO-8. Schematic Diagram, Switch Regulator (6061-2002) (S/N 400101 and on).



POWER DISTRIBUTION		
DEVICE	+5V	GND
74(LS)00	14	7
74LS02	14	7
74LS03	14	7
74(LS)04	14	7
74LS20	14	7
74LS26	14	7
74(LS)74	14	7
74LS112	16	8
74LS124	16	8
74LS164	14	7
74(LS)175	16	8
74LS192	16	8
74LS196	14	7
9601	14	7
96L02	16	8
93L28	16	8

(4) Q8 THRU Q19 ARE 2N2369.

3. ALL CAPACITORS ARE IN MICROFARADS.

2. ALL RESISTORS ARE IN OHMS 1/4W, ±5%.

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSY DESIGNATION.

NOTES: UNLESS OTHERWISE SPECIFIED.

HIGHEST REFERENCE DESIGNATION									
A1	C77	CR24	E29	L1	Q19	R141	TP27	U72	Y1
REF DESIGNATION NOT USED									

ELSTE056

FIGURE FO-9. Schematic Diagram, Spectrum Analyzer Assy (Input Section) (2006-2001) (Sheet 1 of 6).

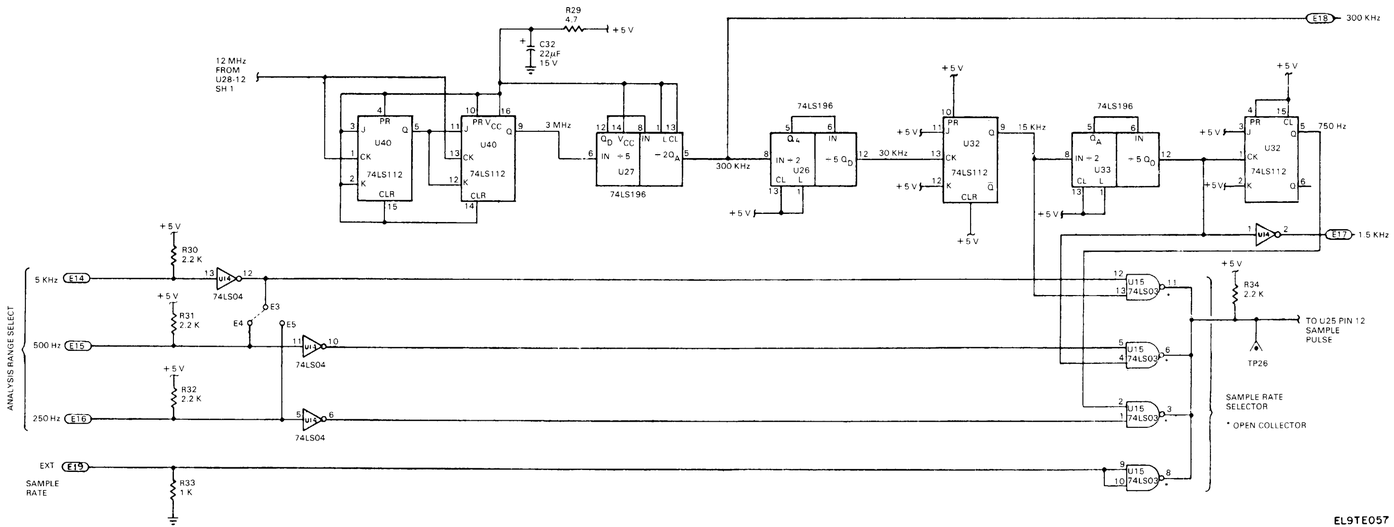


FIGURE FO-9. Schematic Diagram, Spectrum Analyzer Assy (Input Section) (2006-2001) (Sheet 2 of 6).

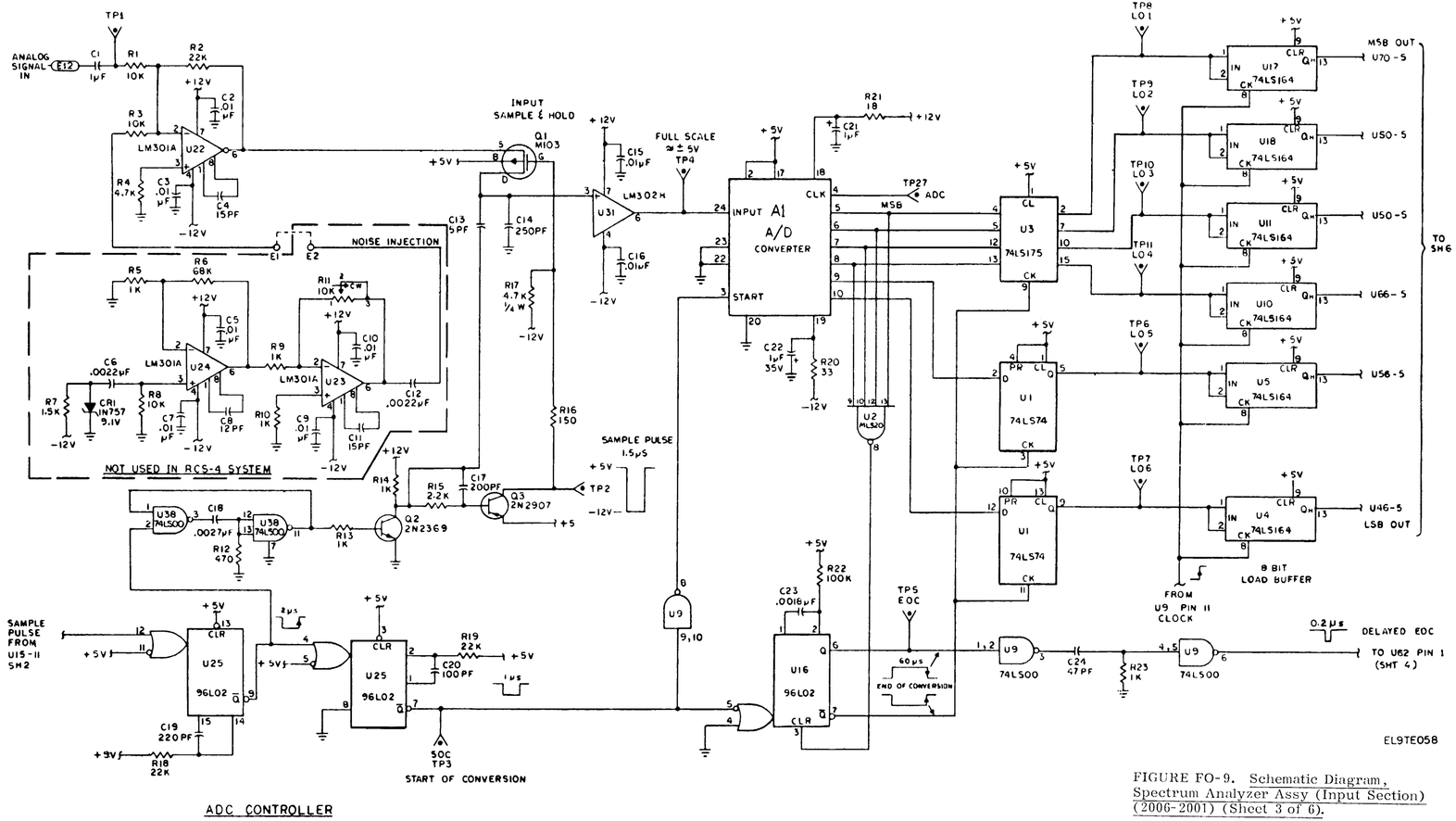


FIGURE FO-9. Schematic Diagram, Spectrum Analyzer Assy (Input Section) (2006-2001) (Sheet 3 of 6).

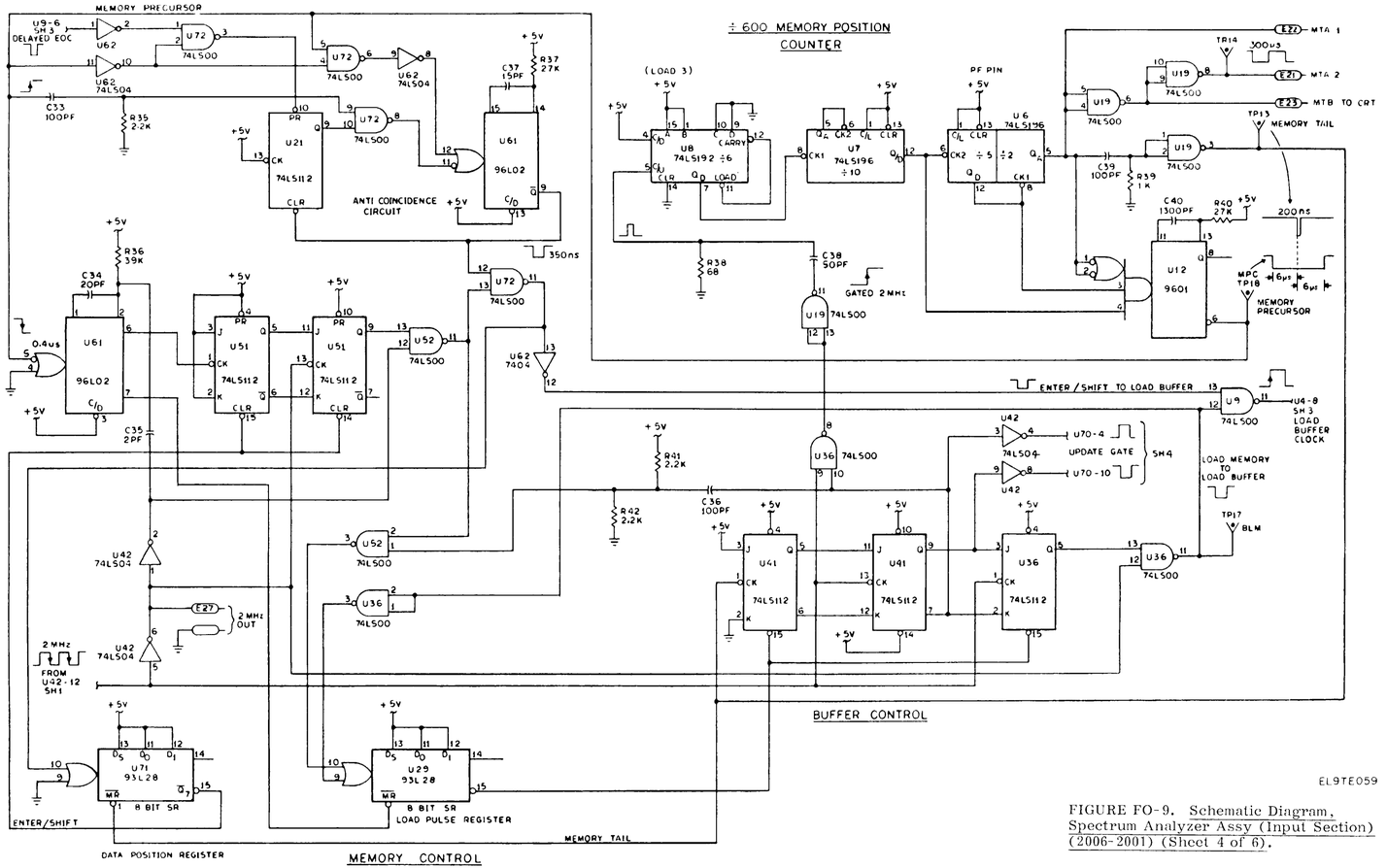


FIGURE FO-9. Schematic Diagram, Spectrum Analyzer Assy (Input Section) (2006-2001) (Sheet 4 of 6).

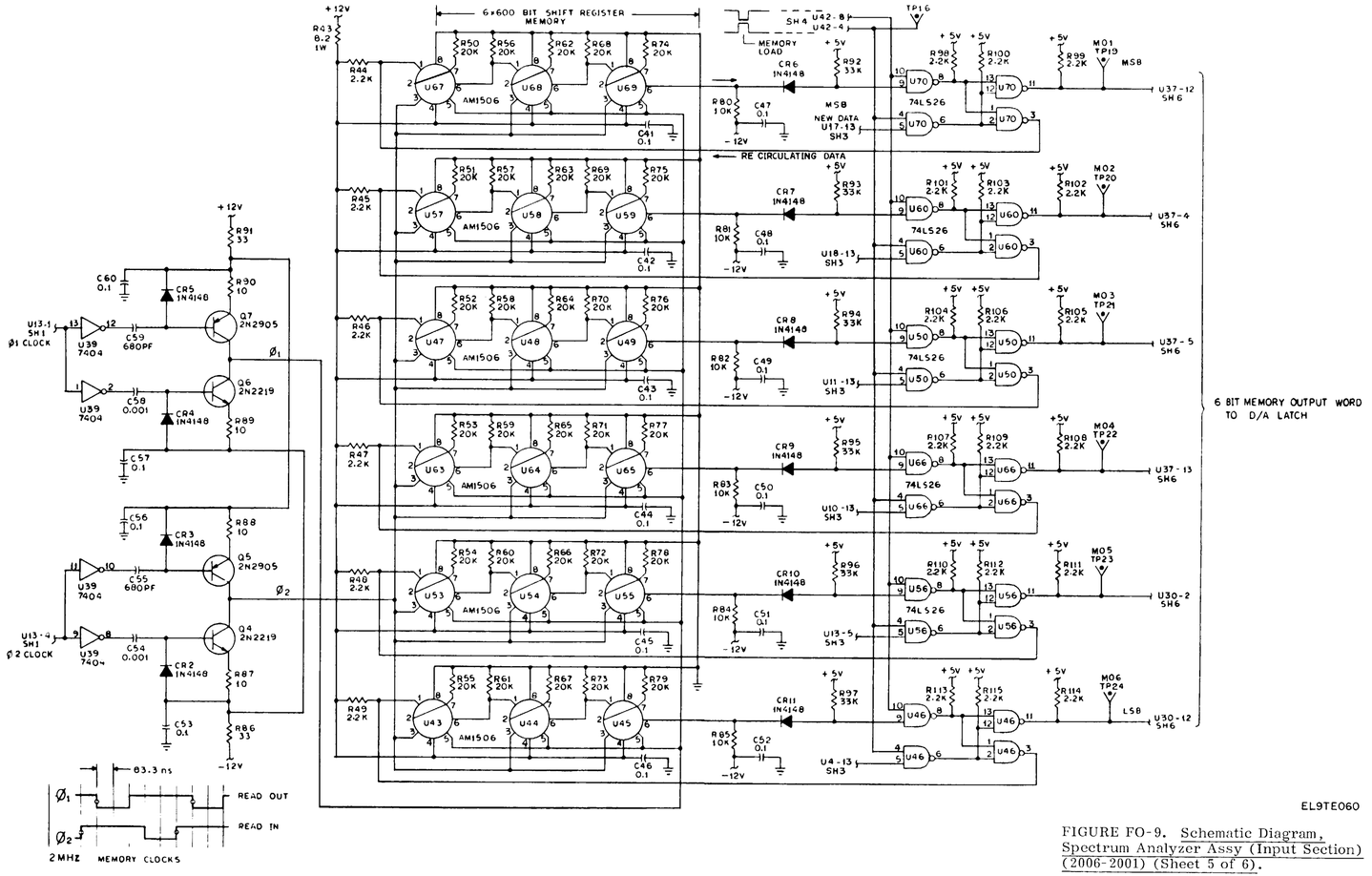
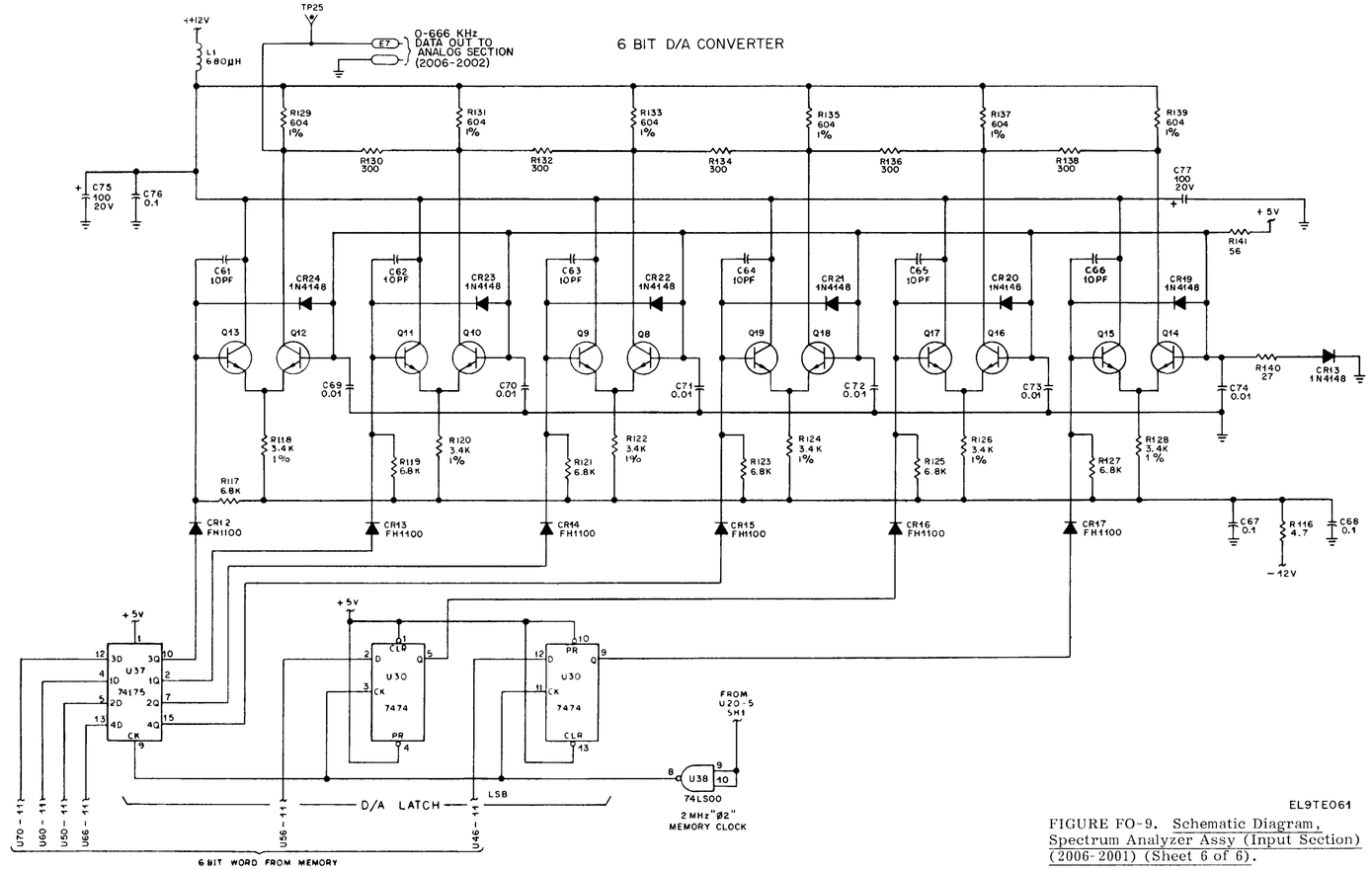
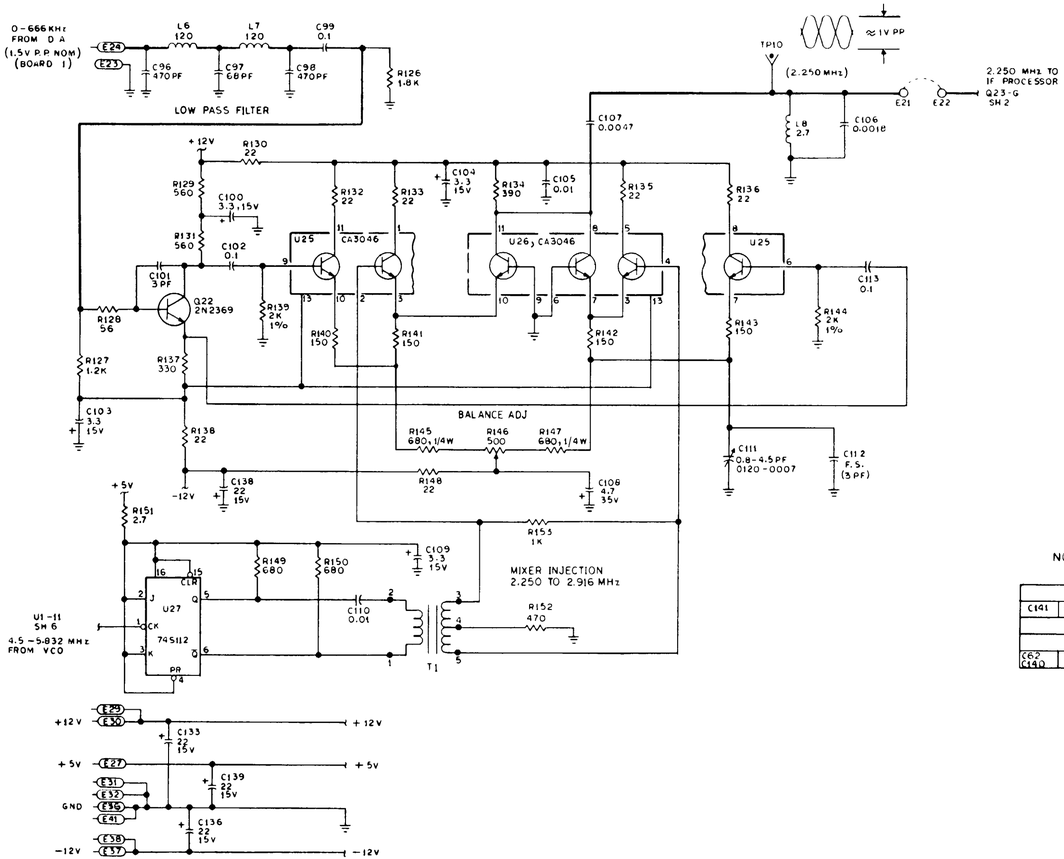


FIGURE FO-9. Schematic Diagram, Spectrum Analyzer Assy (Input Section) (2006-2001) (Sheet 5 of 6).



EL9TE061

FIGURE FO-9. Schematic Diagram, Spectrum Analyzer Assy (Input Section) (2006-2001) (Sheet 6 of 6).



POWER DISTRIBUTION		
DEVICE	+5V	GND
74LS00	14	7
74LS10	14	7
74LS112	16	8
74LS196	14	7
96L02	16	8

4. ALL INDUCTORS ARE IN MICROHENRYS.
3. ALL CAPACITORS ARE IN MICROFARADS.
2. ALL RESISTORS ARE IN OHMS 1/4W, ±5%.
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSY DESIGNATION.

NOTES: UNLESS OTHERWISE SPECIFIED.

HIGHEST REFERENCE DESIGNATION									
C141	CR5	E44	L14	Q32	R192	T1	TP16	U27	
REF DESIGNATION NOT USED									
C62 C140					R17 R185				

EL9TE062

FIGURE FO-10. Schematic Diagram, Spectrum Analyzer Assy (Output Section) (2006-2002) (Sheet 1 of 6).

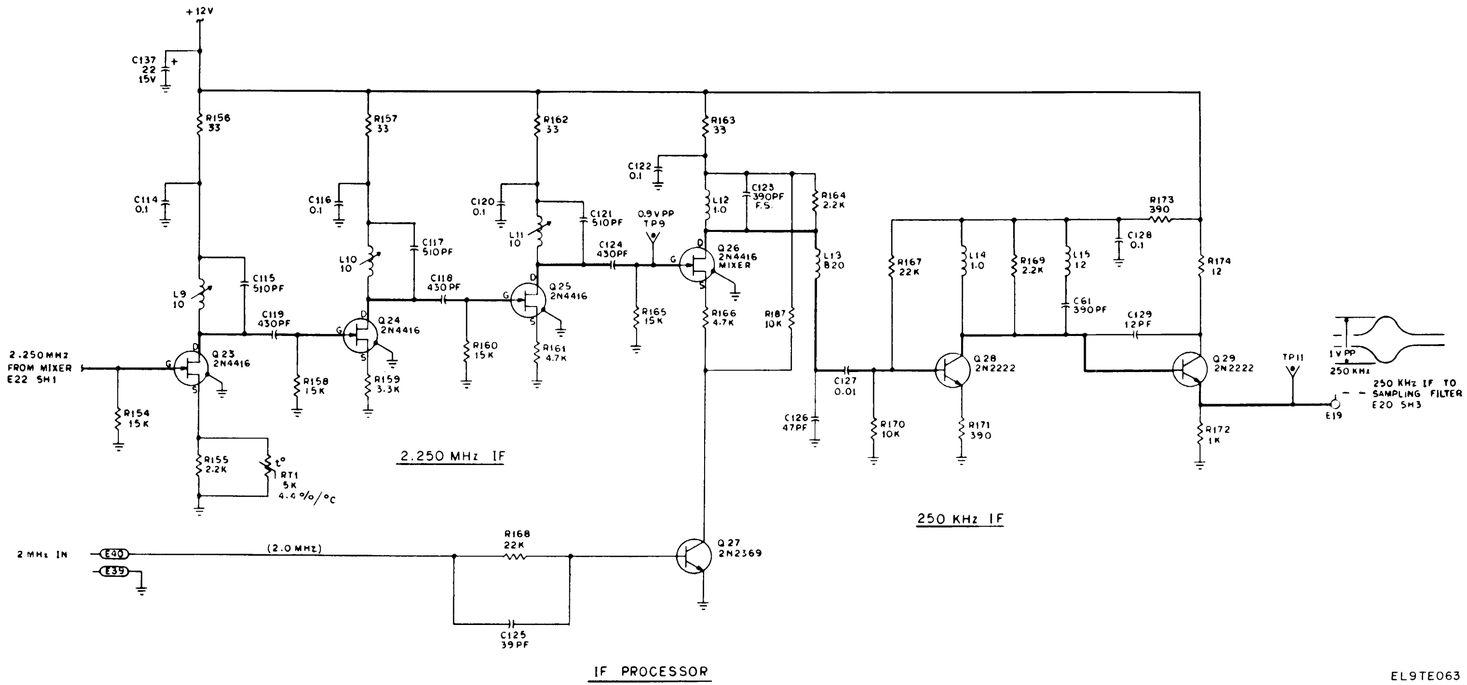


FIGURE FO-10. Schematic Diagram, Spectrum Analyzer Assy (Output Section) (2006-2002) (Sheet 2 of 6).

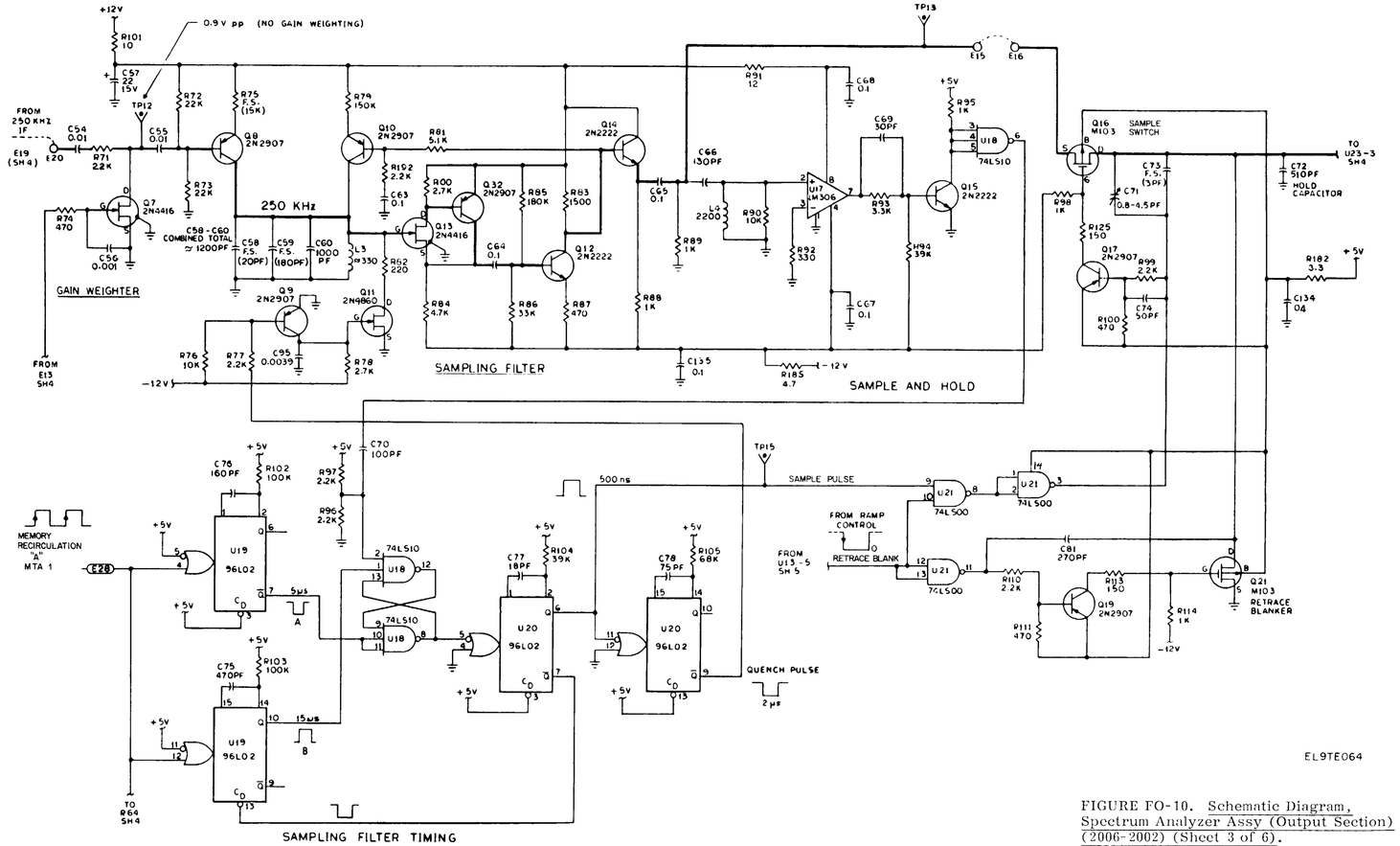
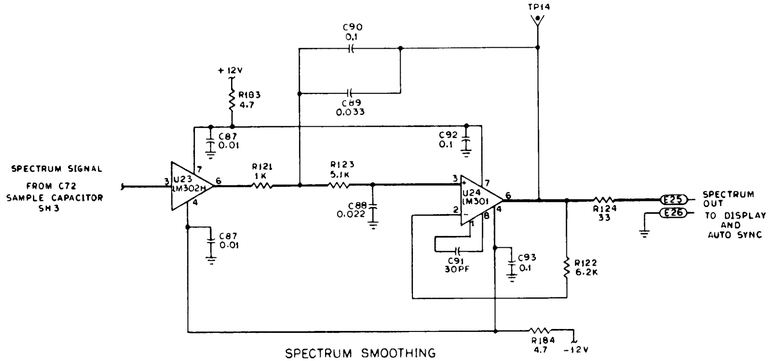
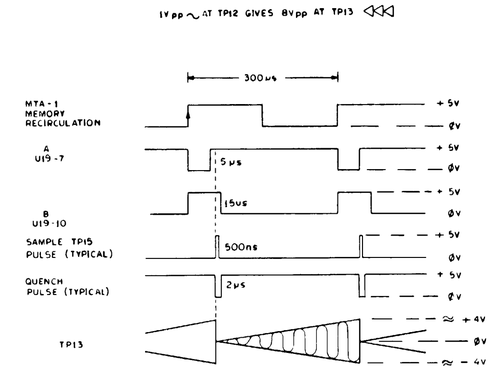


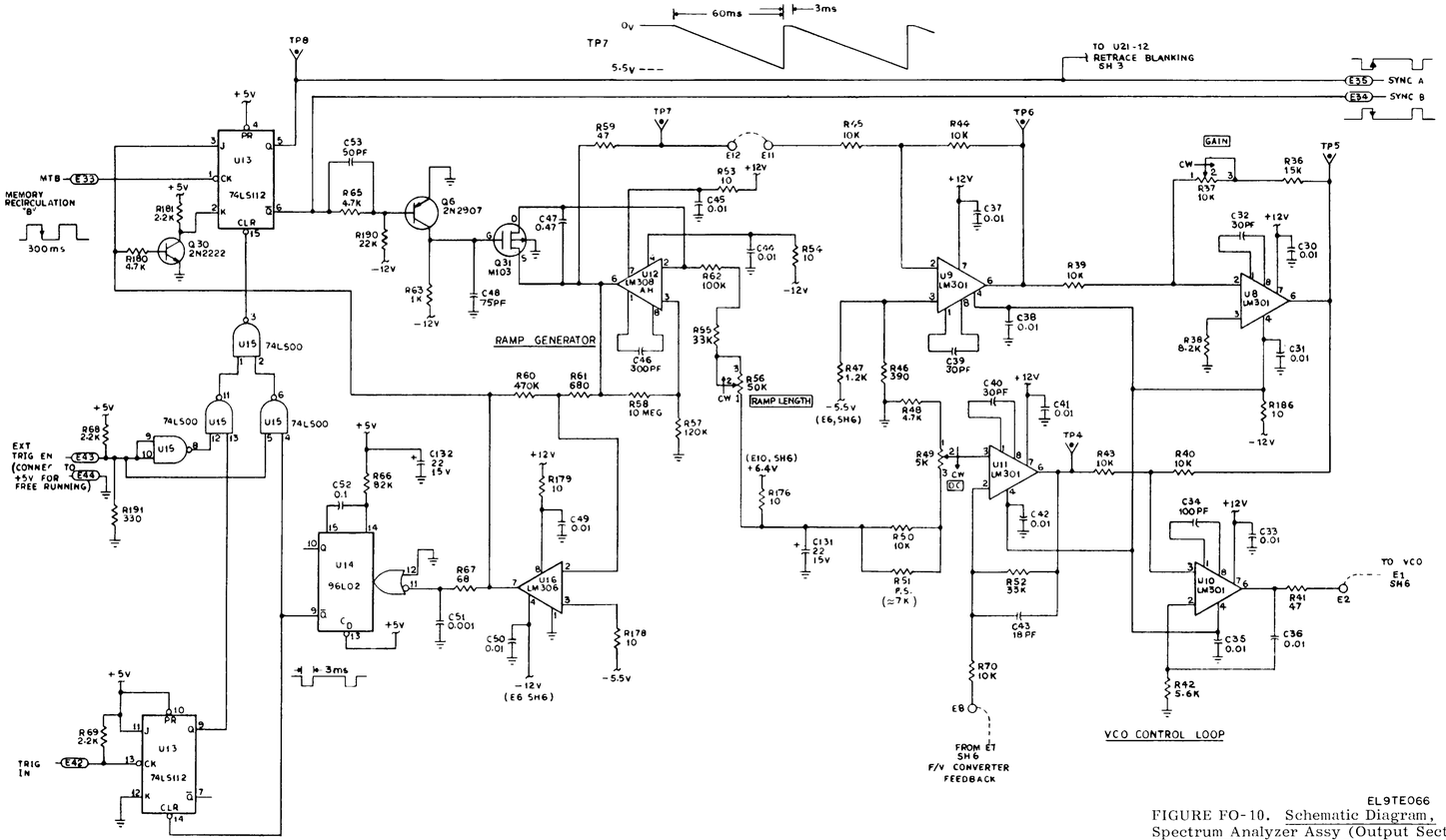
FIGURE FO-10. Schematic Diagram, Spectrum Analyzer Assy (Output Section) (2006-2002) (Sheet 3 of 6).





EL9TE065

FIGURE FO-10. Schematic Diagram, Spectrum Analyzer Assy (Output Section) (2006-2002) (Sheet 4 of 6).



EL9TE066

FIGURE FO-10. Schematic Diagram, Spectrum Analyzer Assy (Output Section) (2006-2002) (Sheet 5 of 6).

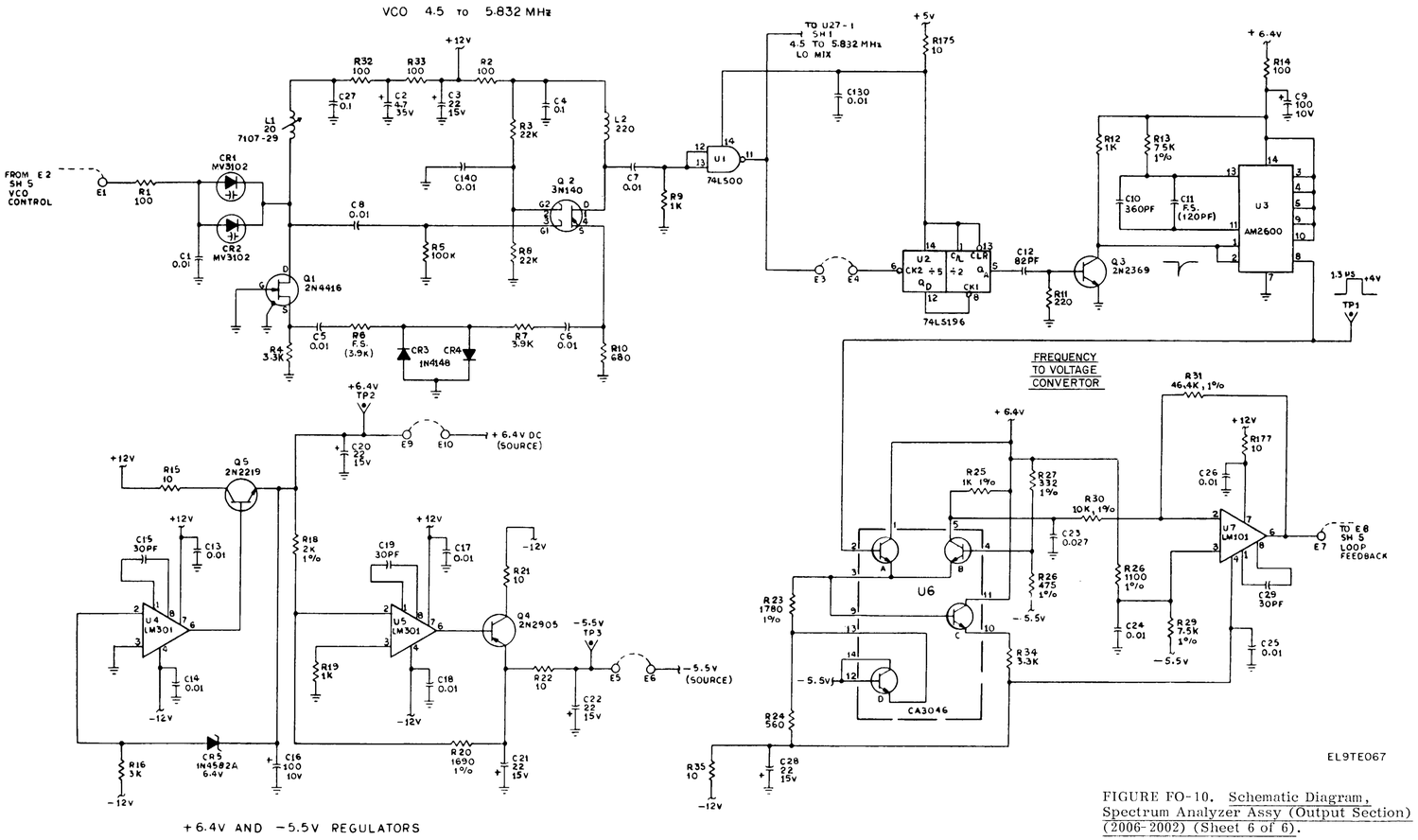


FIGURE FO-10. Schematic Diagram, Spectrum Analyzer Assy (Output Section) (2006-2002) (Sheet 6 of 6).

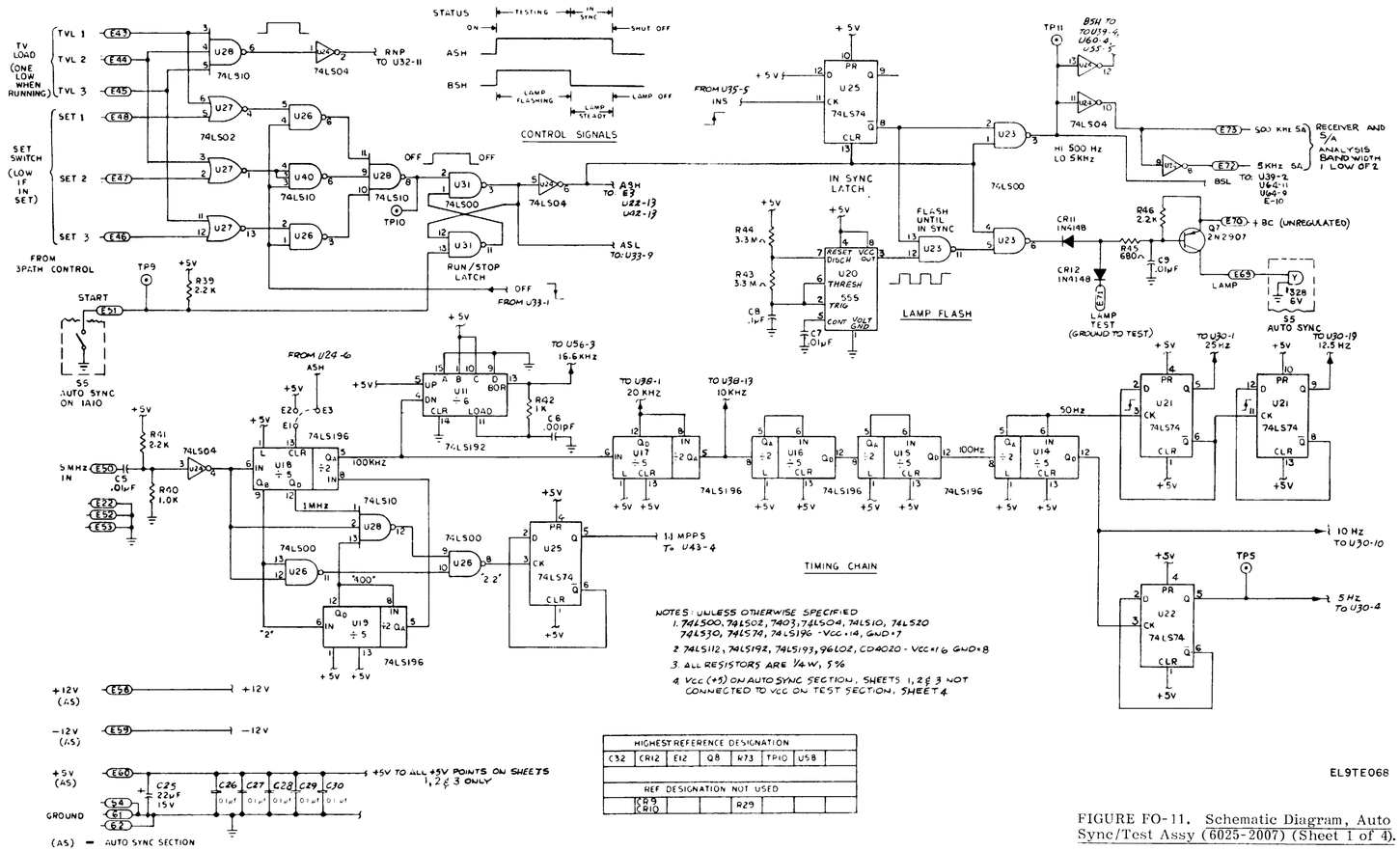
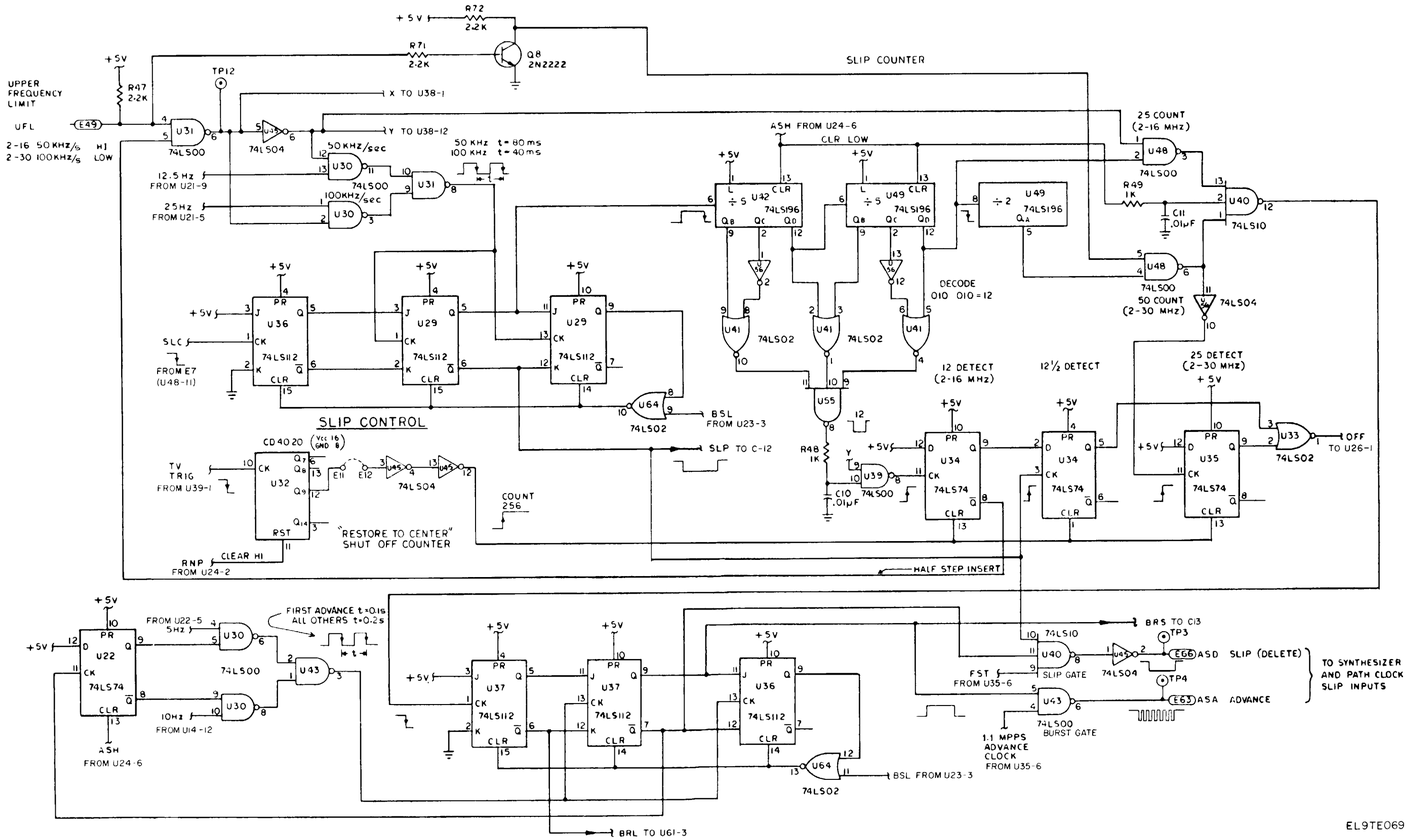
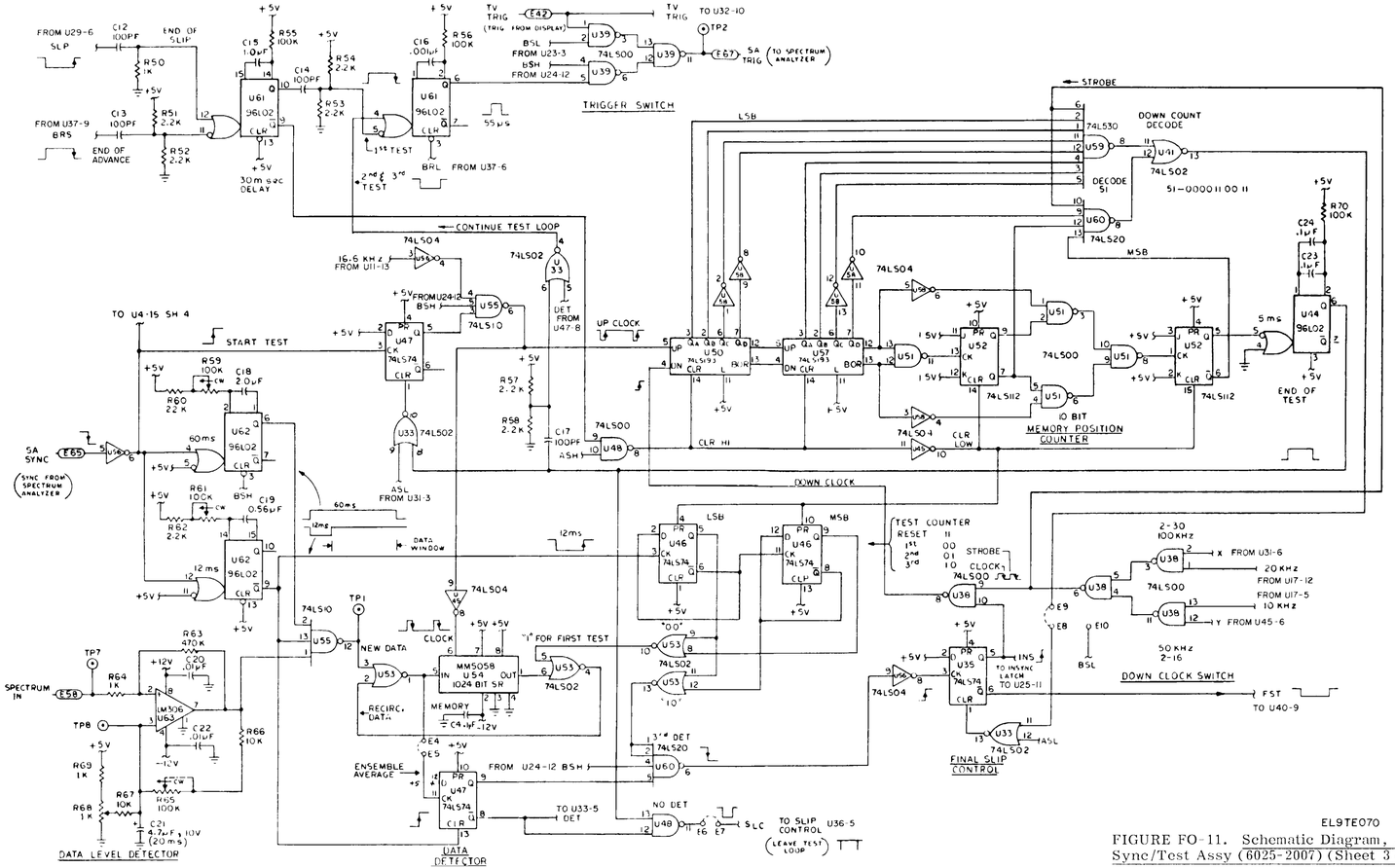


FIGURE FO-11. Schematic Diagram, Auto Sync/Test Assy (6025-2007) (Sheet 1 of 4).



EL9TE069

FIGURE FO-11. Schematic Diagram, Auto Sync/Test Assy (6025-2007) (Sheet 2 of 4).



EL9TE070

FIGURE FO-11. Schematic Diagram, Auto Sync/Test Assy (6025-2007) (Sheet 3 of 4).

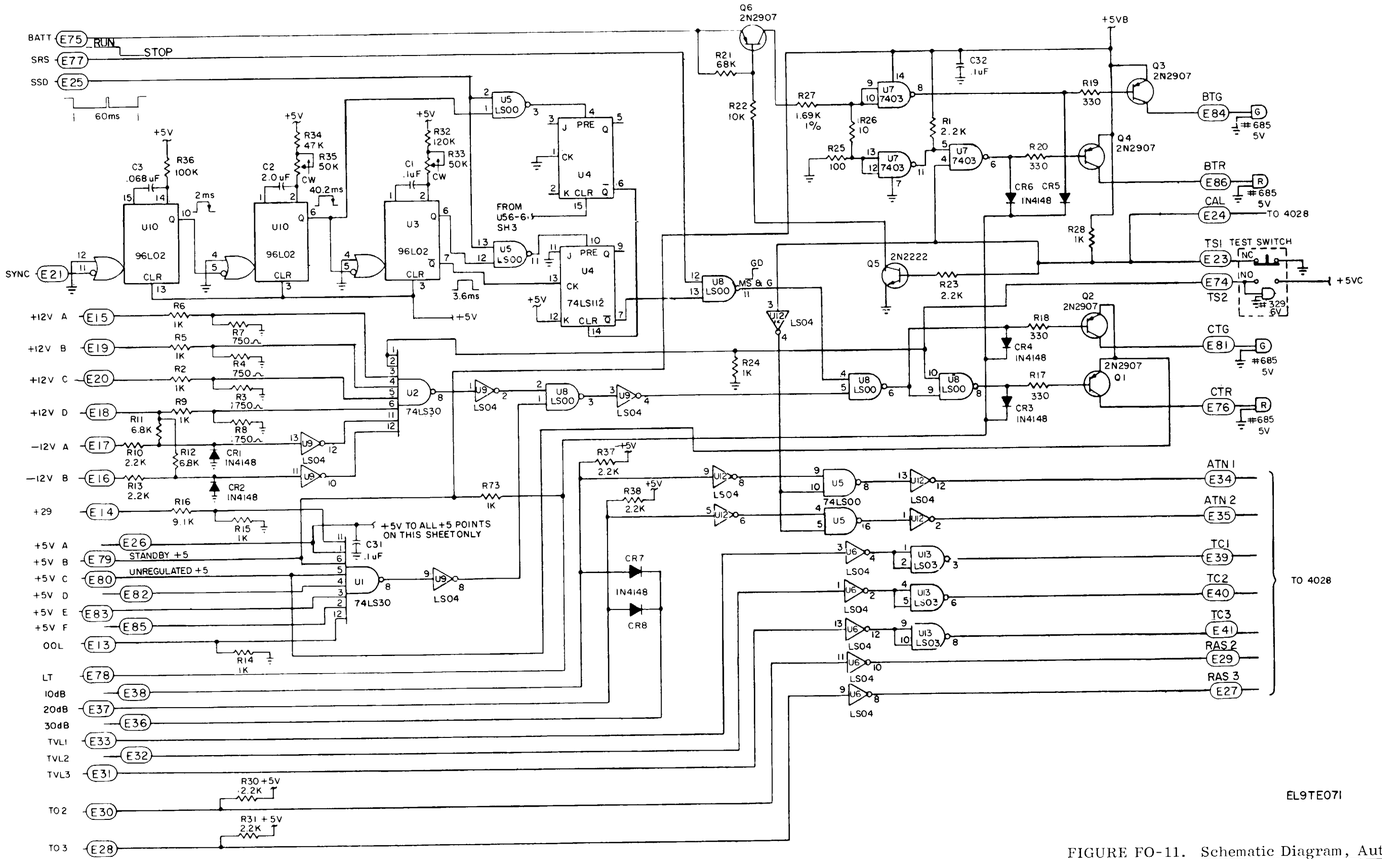
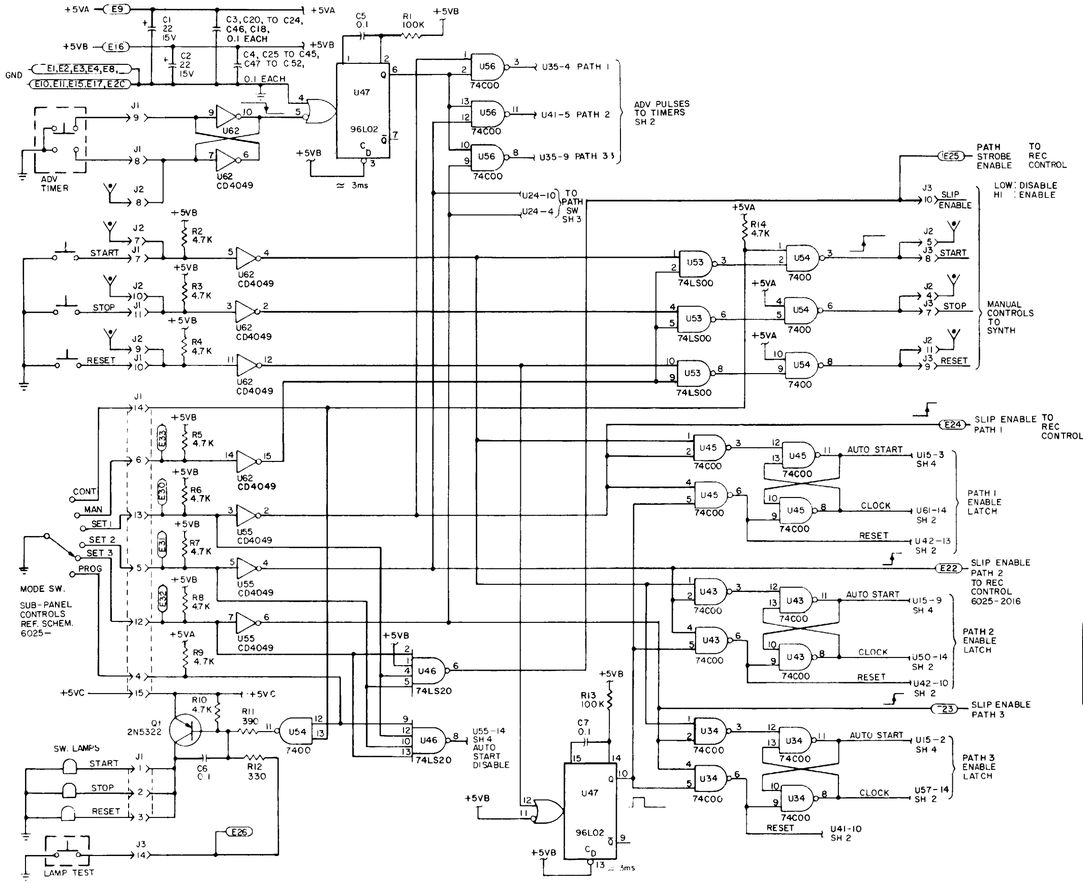


FIGURE FO-11. Schematic Diagram, Auto Sync/Test Assy (6025-2007) (Sheet 4 of 4).



POWER DISTRIBUTION				
DEVICE		+5A	+5B	GND
74LS10	U15	14		7
74C00	U34, U35, U41, U42 U43, U45, U56, U69		14	7
74LS00	U4, U24, U53	14		7
74C00	U11	14		7
7400	U54	14		7
74C04	U32, U36, U44		14	7
74S04	U3	14		7
74C10	U5, U6	14		7
74LS20	U46	14		7
74LS42	U8, U9, U13	16		8
74LS159	U1	24		12
74LS175	U2	16		8
74C192	U25, U26, U27, U28, U29, U30, U31, U33, U37, U38, U39, U40, U48, U49, U50, U51, U52, U57, U58, U59, U60, U61, U64, U66		16	8
74LS192	U63, U65, U67		16	8
74LS257	U10, U12, U16, U17, U18, U19, U20, U21, U22, U23	16		8
CD4049	U55, U62		1	8
96L02	U7, U14, U68	16		8
96L02	U47		16	8

4. PINS 1, 4, 9, 10, 11, & 15 CONNECTED TO V_{CC} (PIPLC SH2)
3. ALL CAPACITORS ARE IN MICROFARADS
2. ALL RESISTORS ARE IN OHMS 1/4 W, ± 5 %
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN, FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSY DESIGNATION

NOTES : UNLESS OTHERWISE SPECIFIED

HIGHEST REFERENCE DESIGNATION						
C53	E35	J5	Q1	R27	U69	
REF DESIGNATION NOT USED						

EL9TE072

FIGURE FO-12. Schematic Diagram, 3-Path Programmer Assy (6025-2015) (Sheet 1 of 4) (S/N 400101 and on).

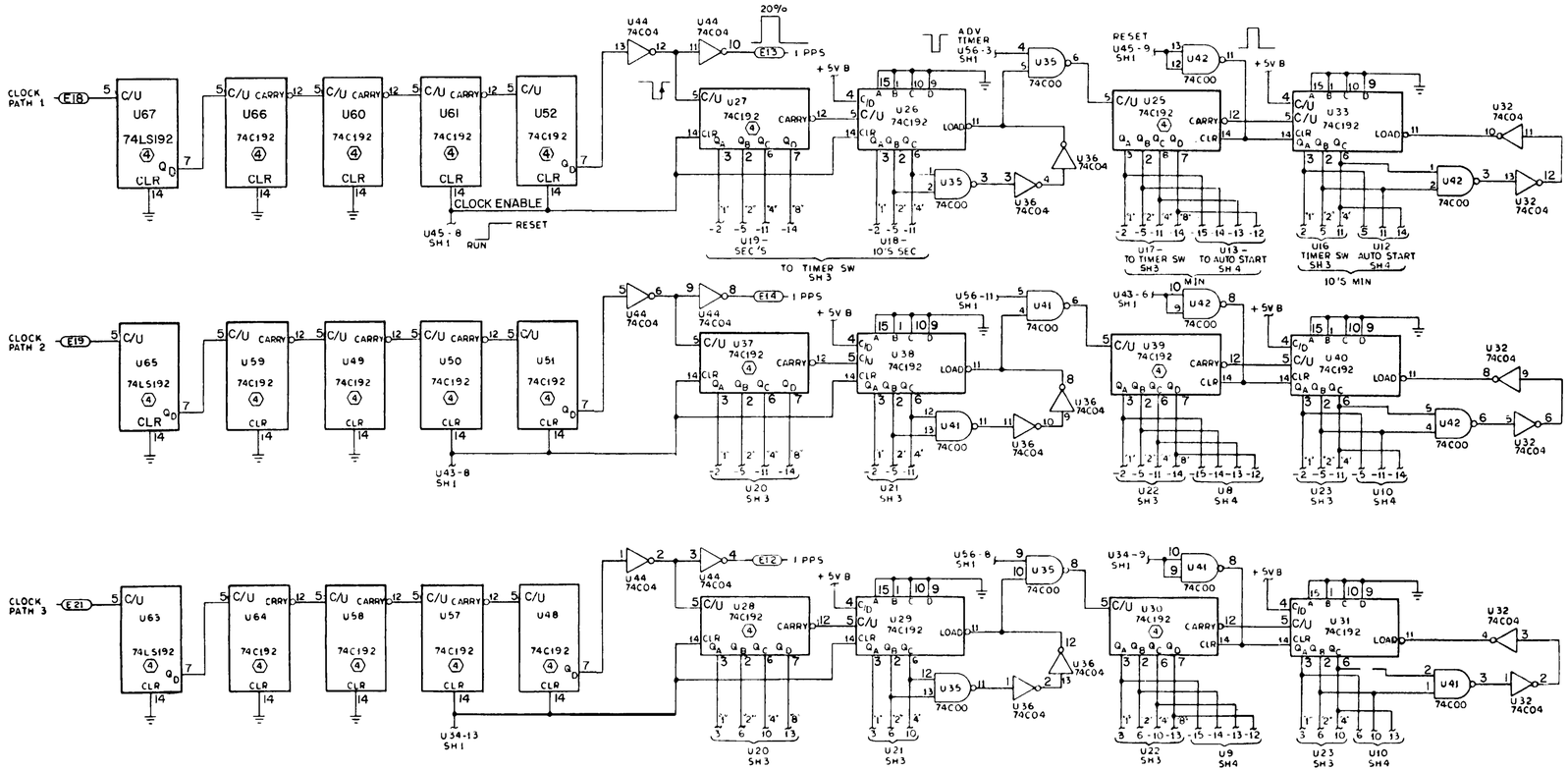


FIGURE FO-12. Schematic Diagram, 3-Path Programmer Assy (6025-2015) (Sheet 2 of 4) (S/N 400101 and on).

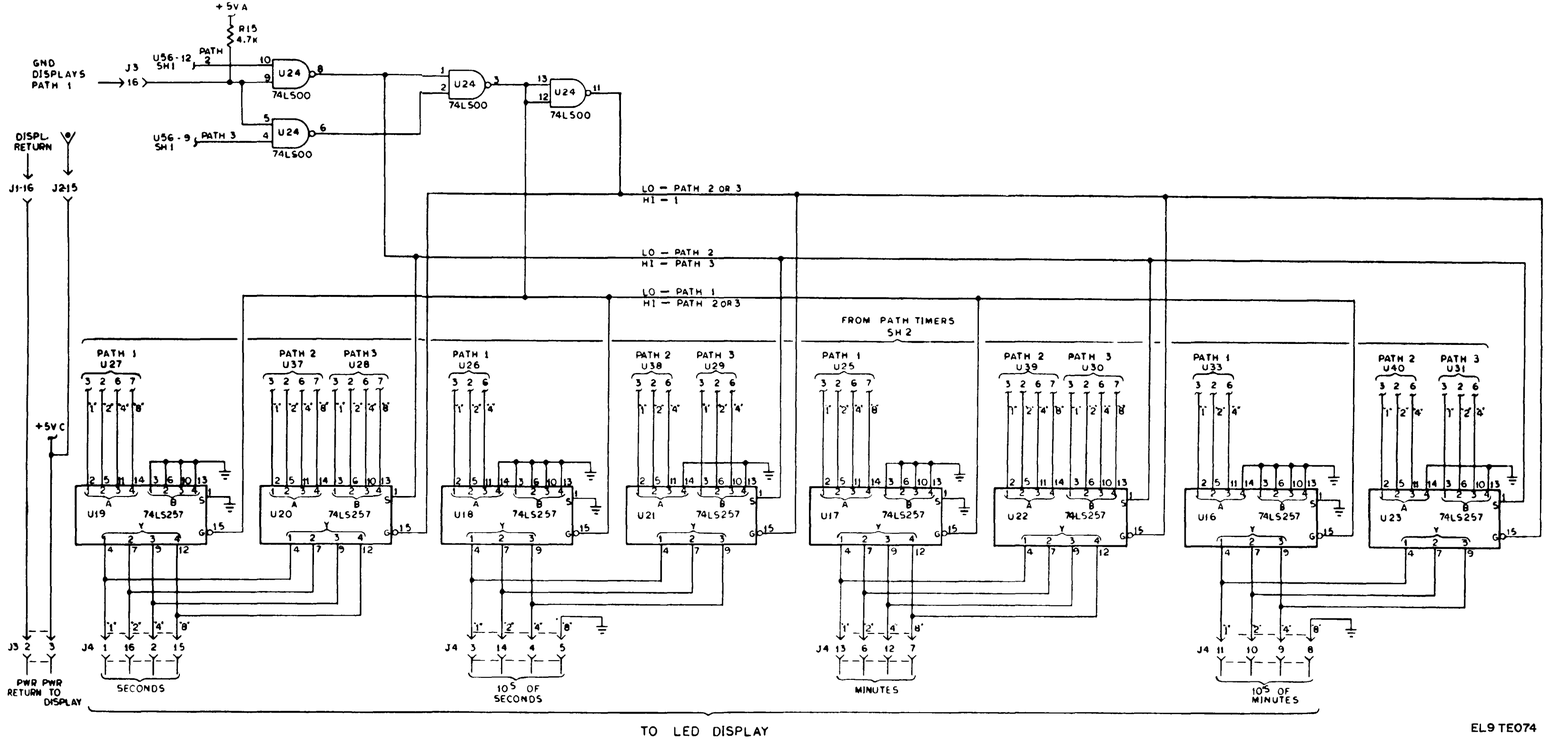
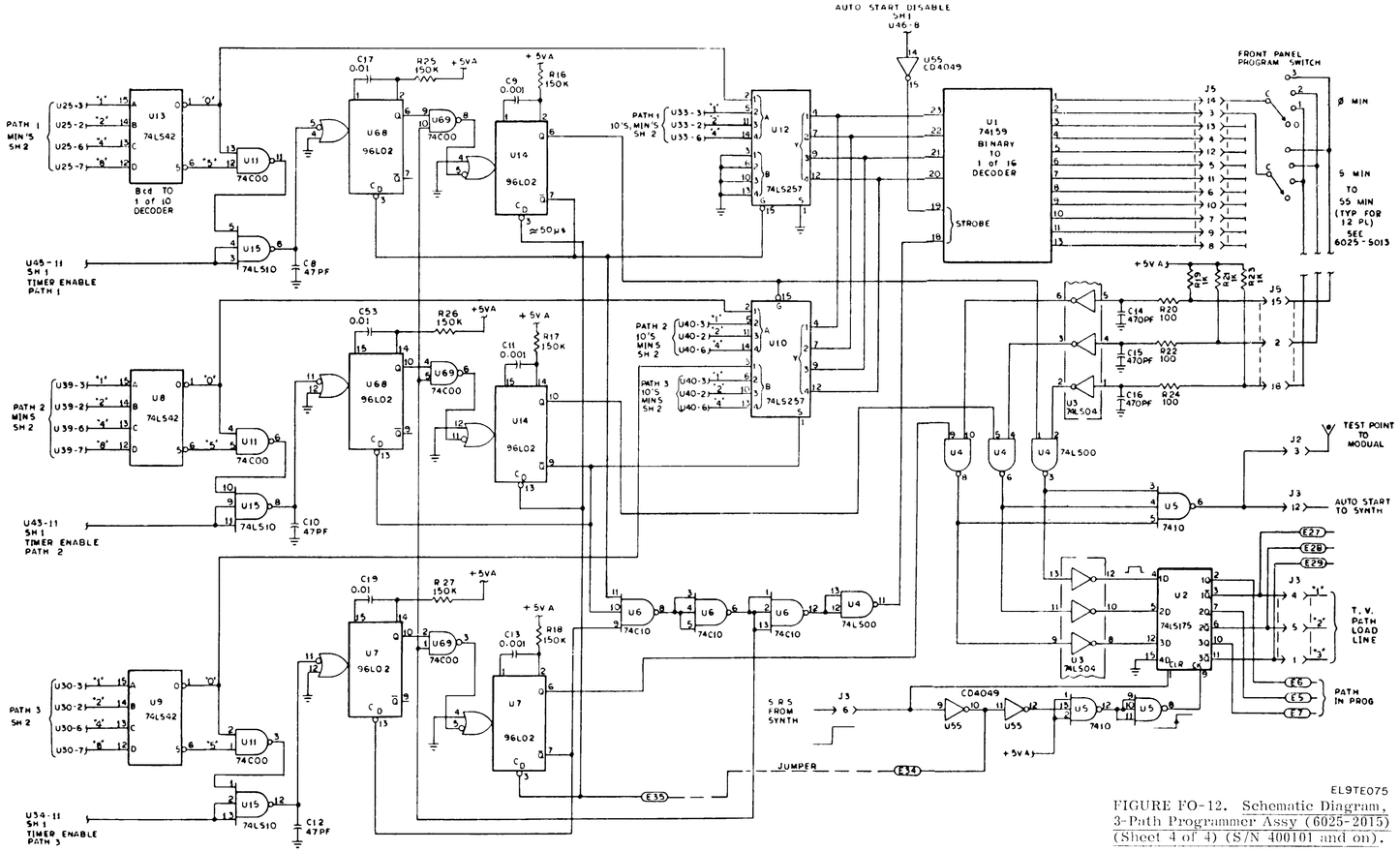
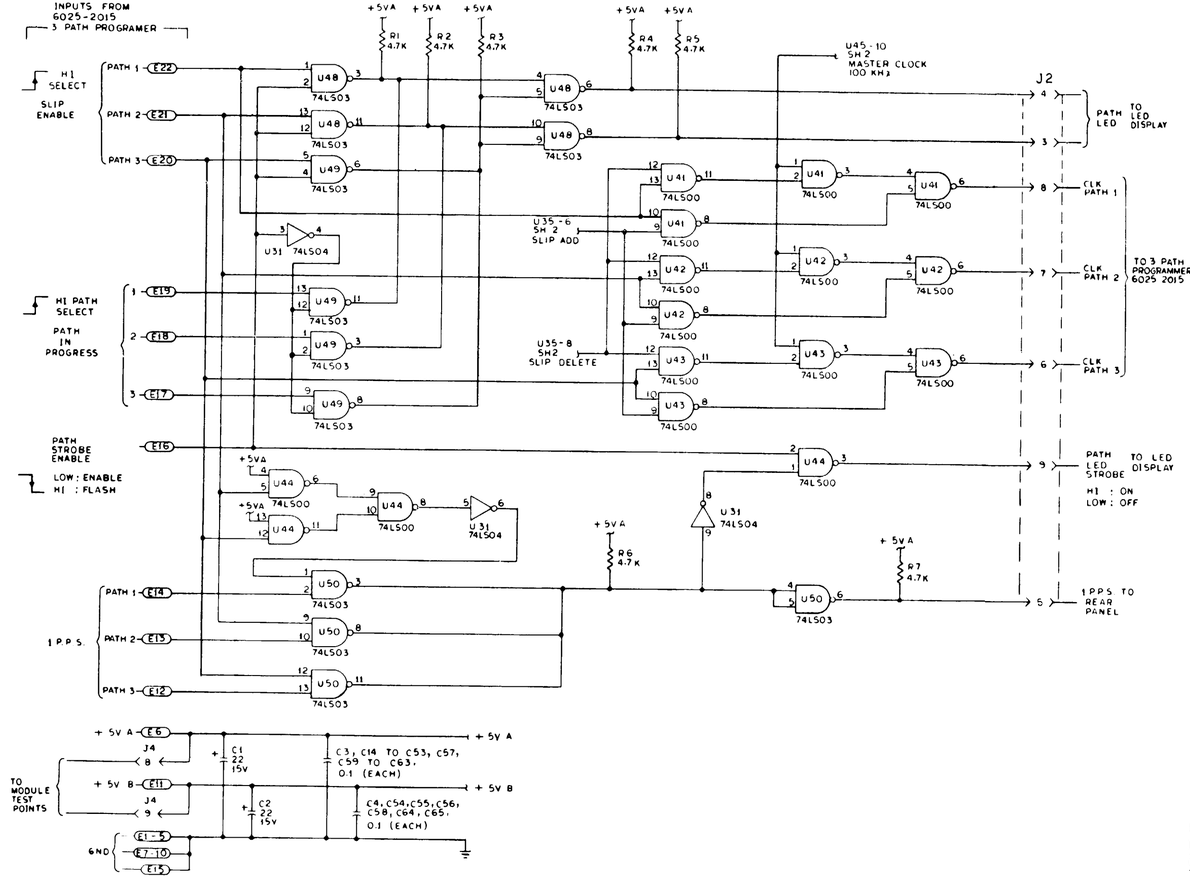


FIGURE FO-12. Schematic Diagram, 3-Path Programmer Assy (6025-2015) (Sheet 3 of 4) (S/N 400101 and on).



EL9TE075

FIGURE FO-12. Schematic Diagram, 3-Path Programmer Assy (6025-2015) (Sheet 4 of 4) (S/N 400101 and on).



POWER DISTRIBUTION				
I.C. Nº	DEVICE	+5VA	+5VB	GND
U35, U38, U44	74LS00	14		7
U41, U42, U43	74LS00		14	7
U48, U49, U50	74LS03	14		7
U1, U3, U31, U34	74LS04	14		7
U45	74LS04		14	7
U4, U9	7406	14		7
U37	74LS10	14		7
U2	74LS42	16		8
U10, U12, U13	74LS85	16		8
U7, U19, U28	74LS112	16		8
U5, U15, U16, U17, U18	74LS175	16		8
U11	74S188	16		8
U20, U23, U24, U27	74LS192	16		8
U6	74LS193	16		8
U29, U30, U32, U33 U39, U40, U46, U47	74LS196	14		7
U51, U52	74LS196		14	7
U21, U22, U25, U26	74LS257	16		8
U8, U14, U36	96L02	16		8

3. ALL CAPACITORS ARE IN MICROFARADS.
2. ALL RESISTORS ARE IN OHMS 1/4 W, ±5%.
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSY DESIGNATION.

NOTES: UNLESS OTHERWISE SPECIFIED.

HIGHEST REFERENCE DESIGNATION				
C65	E27	J6	R40	U52
REF DESIGNATION NOT USED				

EL9TE076

FIGURE FO-13. Schematic Diagram, Receiver Control Assy (6025-2016) (Sheet 1 of 4) (S/N 400101 and on).

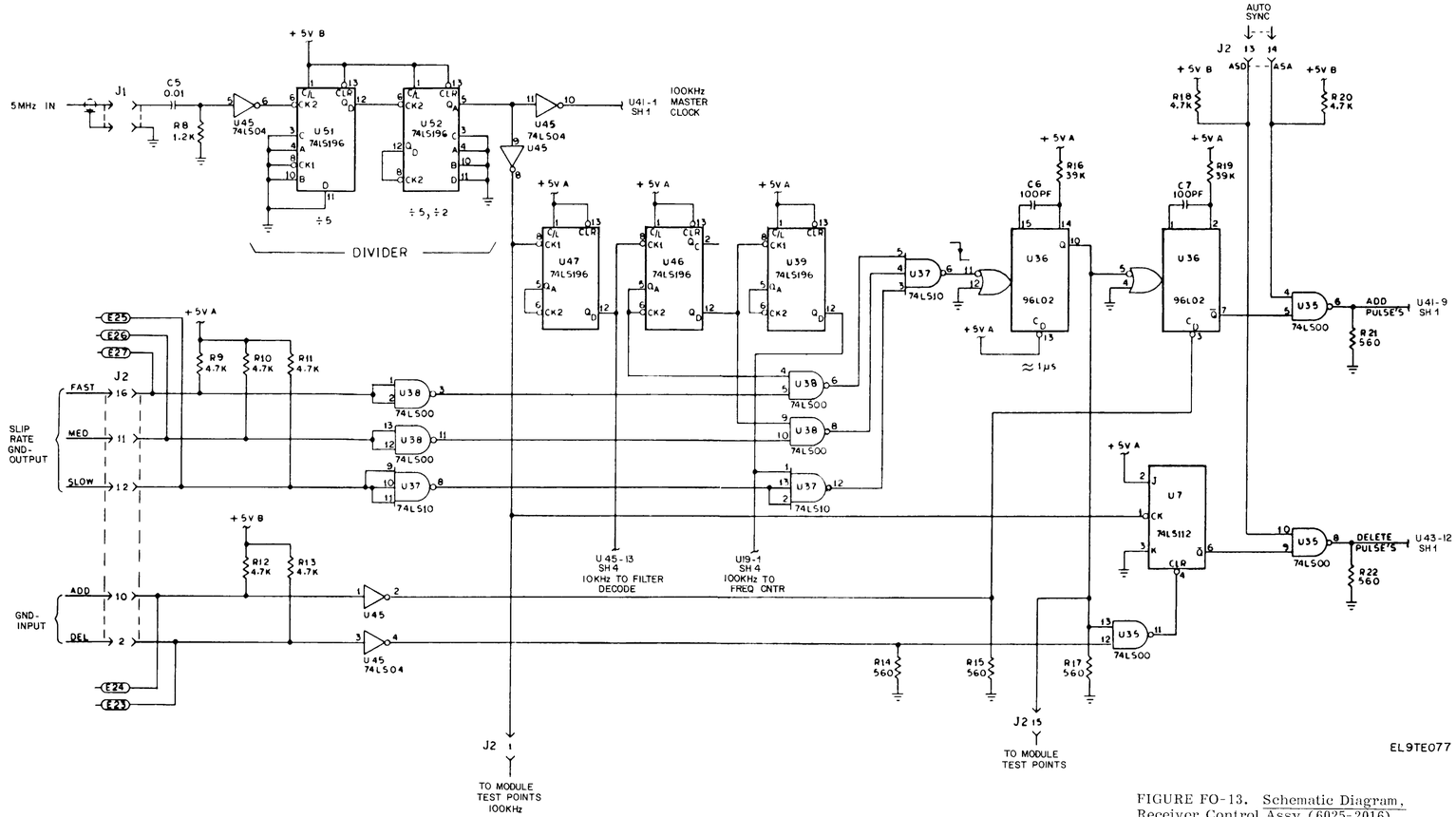
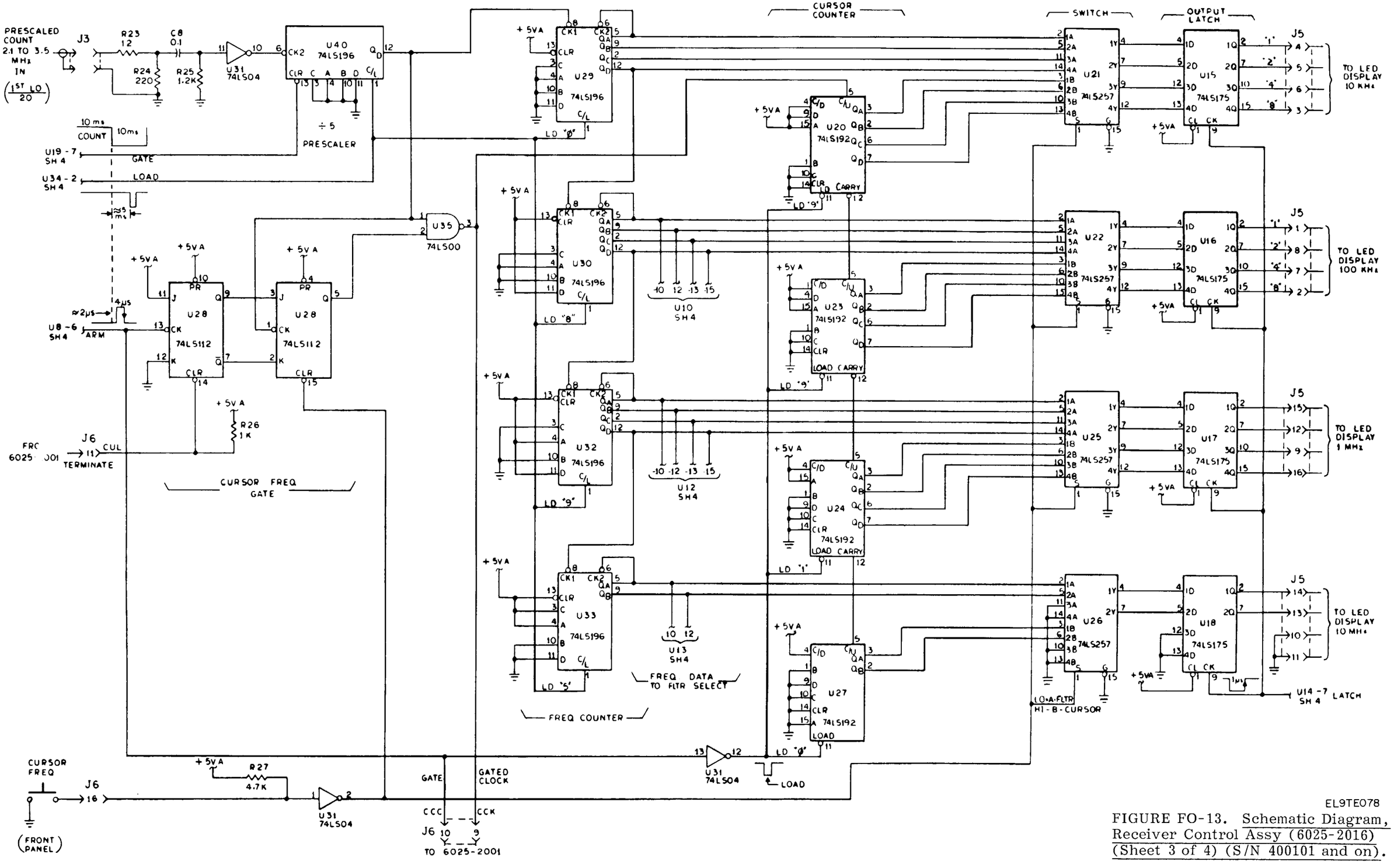
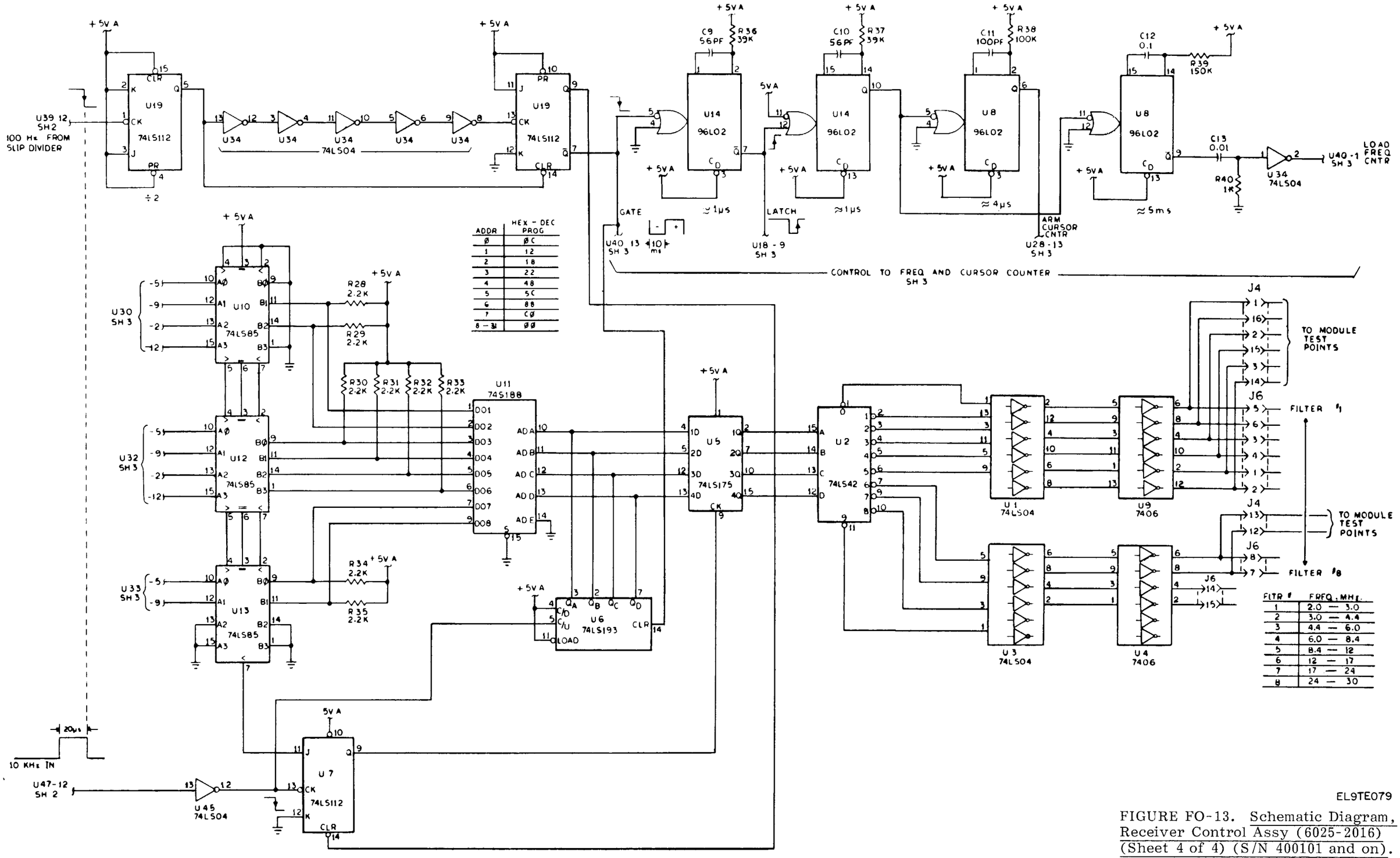


FIGURE FO-13. Schematic Diagram, Receiver Control Assy (6025-2016) (Sheet 2 of 4) (S/N 400101 and on).



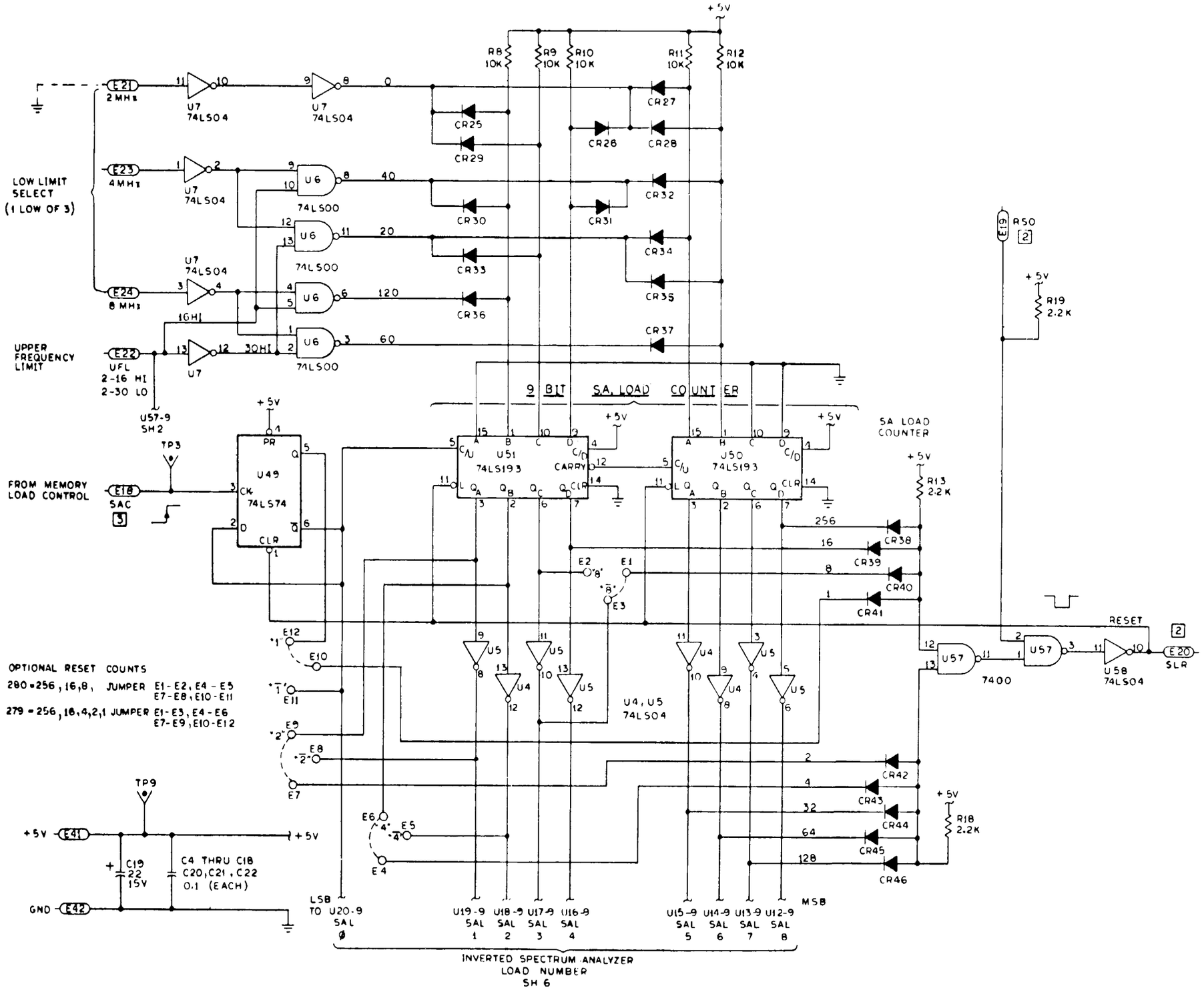
EL9TE078

FIGURE FO-13. Schematic Diagram, Receiver Control Assy (6025-2016) (Sheet 3 of 4) (S/N 400101 and on).



EL9TE079

FIGURE FO-13. Schematic Diagram, Receiver Control Assy (6025-2016) (Sheet 4 of 4) (S/N 400101 and on).



POWER DISTRIBUTION		
DEVICE	+5V	GND
74(LS)00	14	7
74LS02	14	7
74LS04	14	7
74LS10	14	7
74LS74	14	7
74LS164	14	7
74LS175	16	8
74LS192	16	8
74LS193	16	8
93L12	16	8

4. ALL DIODES ARE 1N4148.
3. ALL CAPACITORS ARE IN MICROFARADS.
2. ALL RESISTORS ARE IN OHMS 1/4W, ±5%.
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSY DESIGNATION.

NOTES: UNLESS OTHERWISE SPECIFIED.

HIGHEST REFERENCE DESIGNATION								
C29	CR46	E43	R25	TP8	U58			
REF DESIGNATION NOT USED								
C28								

EL9TE080

FIGURE FO-14. Schematic Diagram, Cursor Storage and Readout Assy (6025-2001) (Sheet 1 of 6).

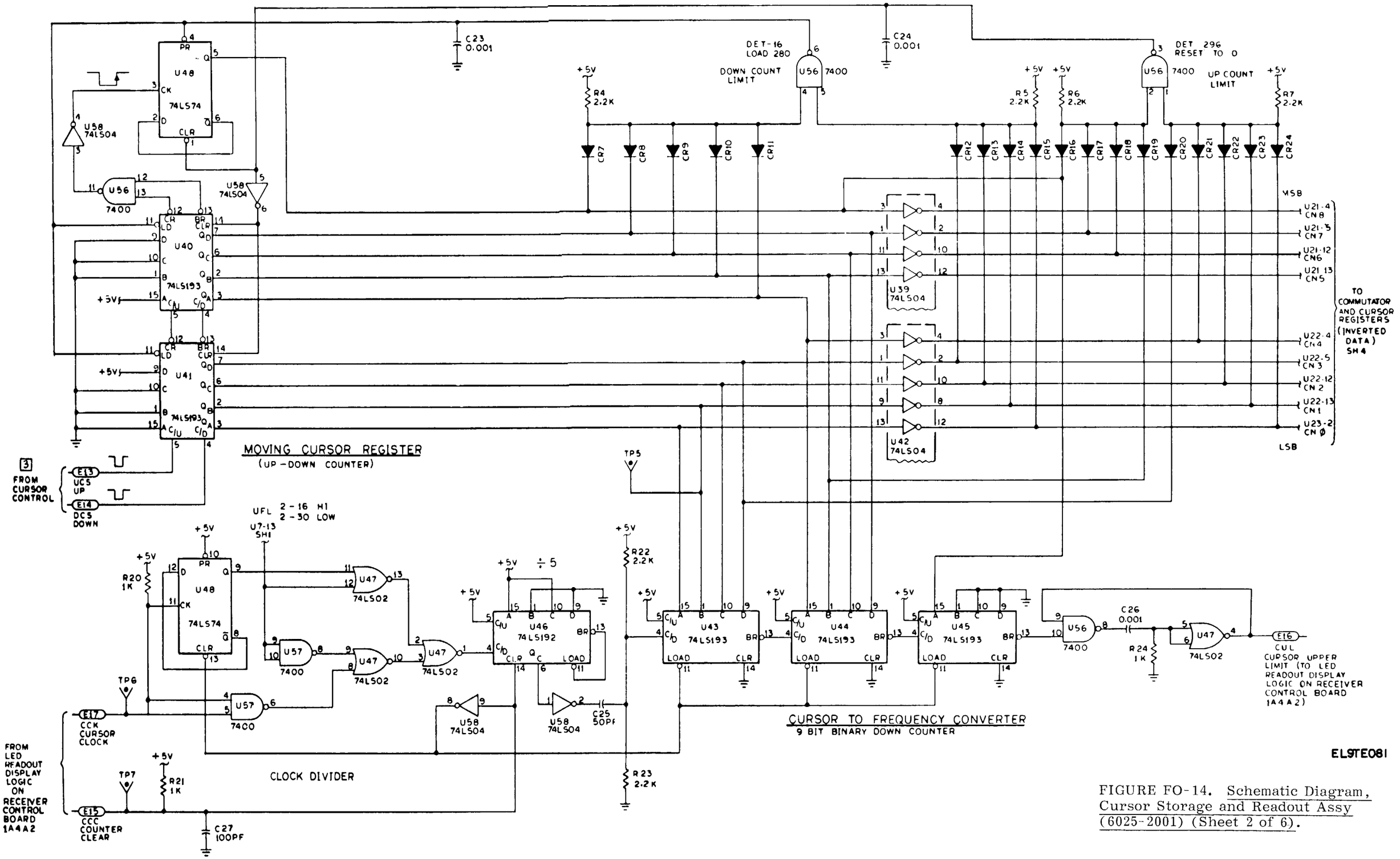
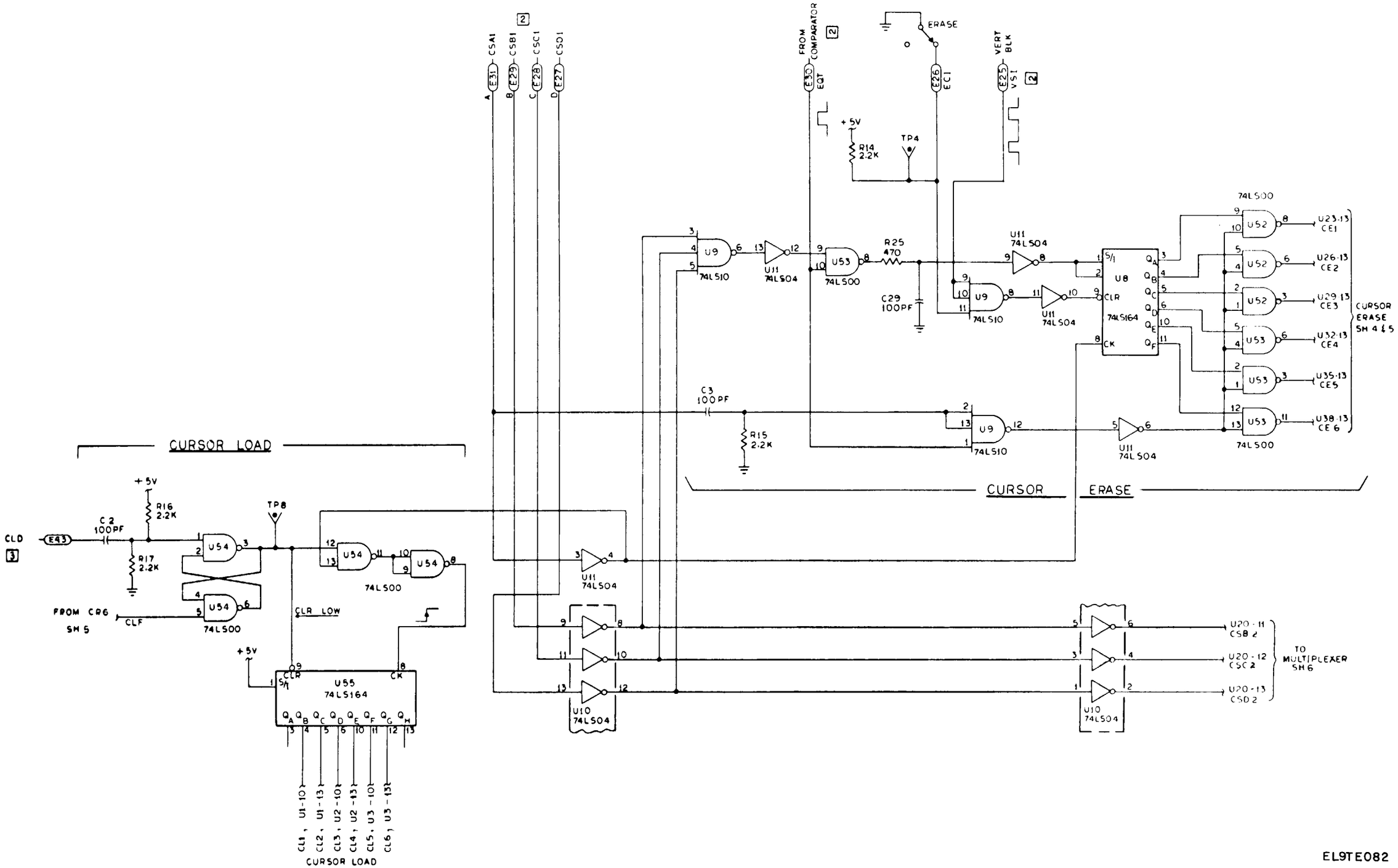


FIGURE FO-14. Schematic Diagram, Cursor Storage and Readout Assy (6025-2001) (Sheet 2 of 6).



EL9TE082

FIGURE FO-14. Schematic Diagram, Cursor Storage and Readout Assy (6025-2001) (Sheet 3 of 6).

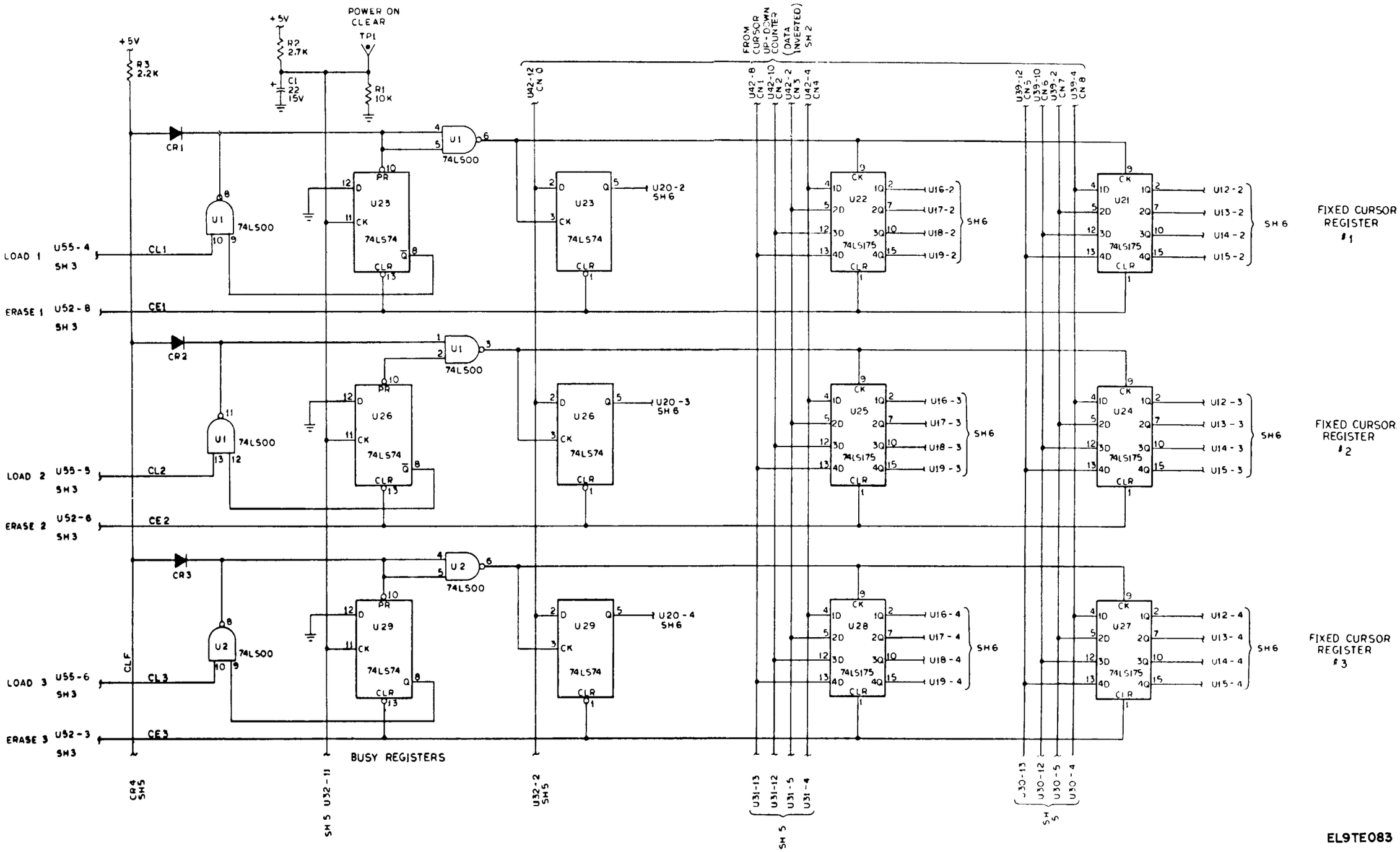


FIGURE FO-14. Schematic Diagram, Cursor Storage and Readout Assy (6025-2001) (Sheet 4 of 6).

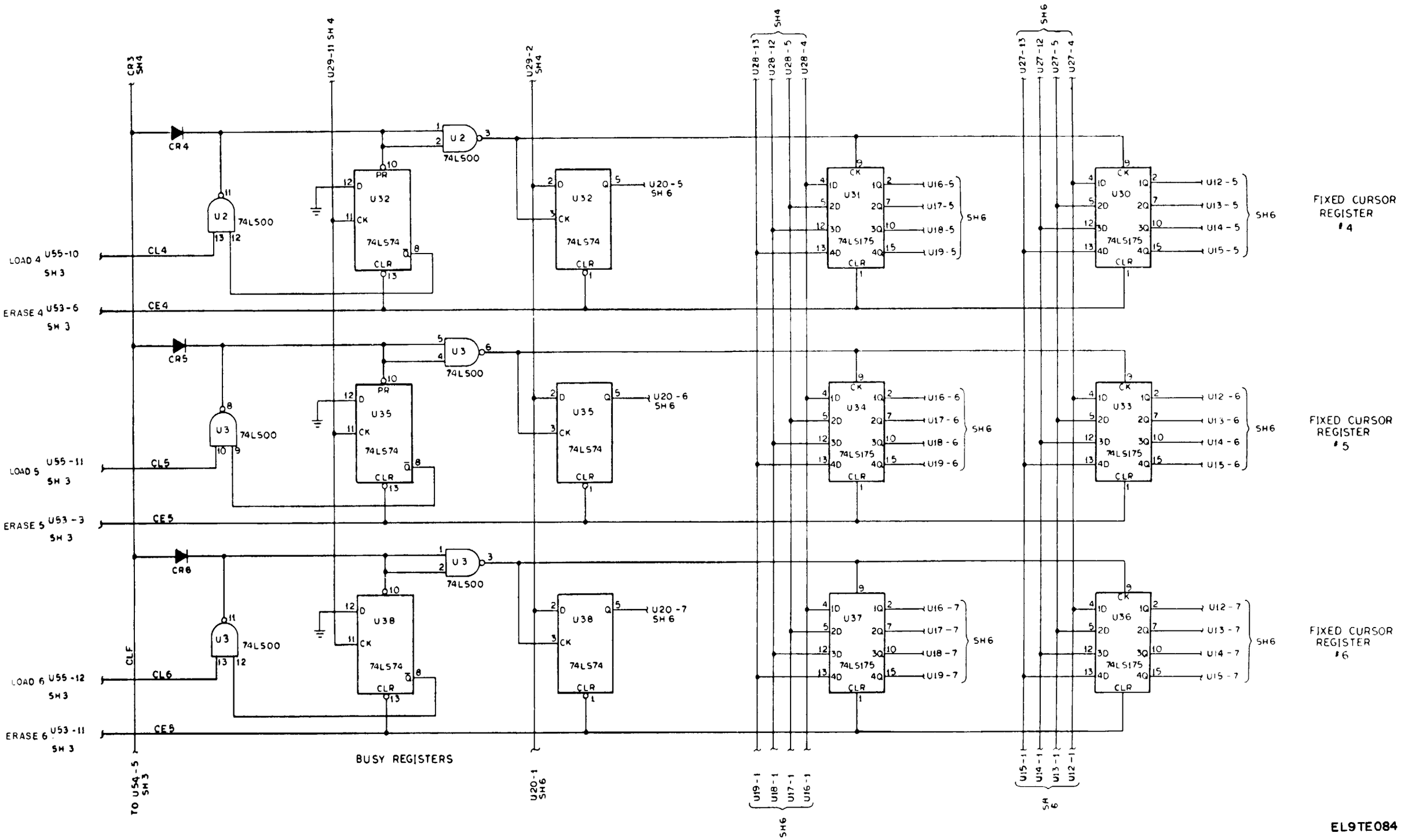
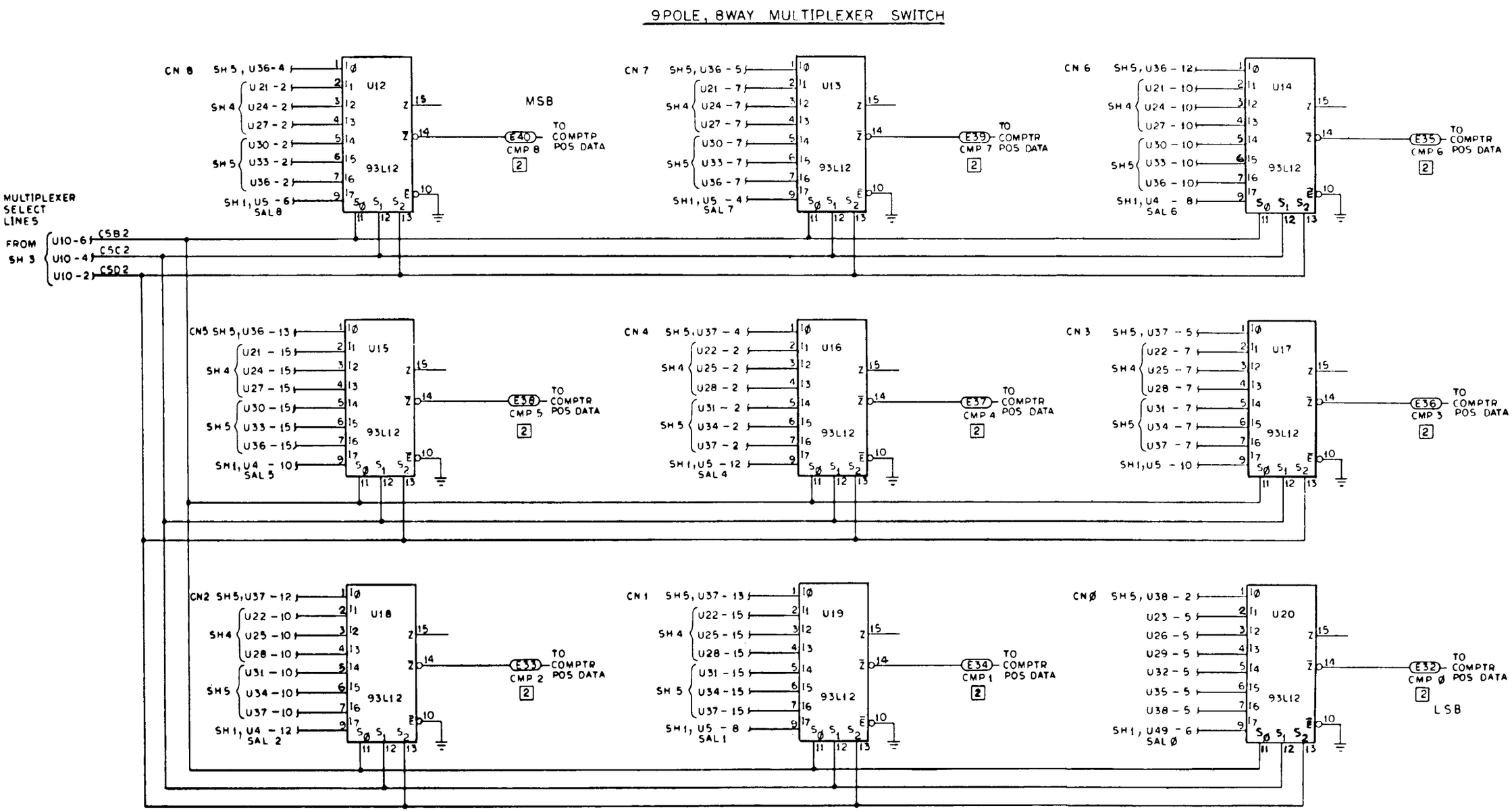


FIGURE FO-14. Schematic Diagram, Cursor Storage and Readout Assy (6025-2001) (Sheet 5 of 6).

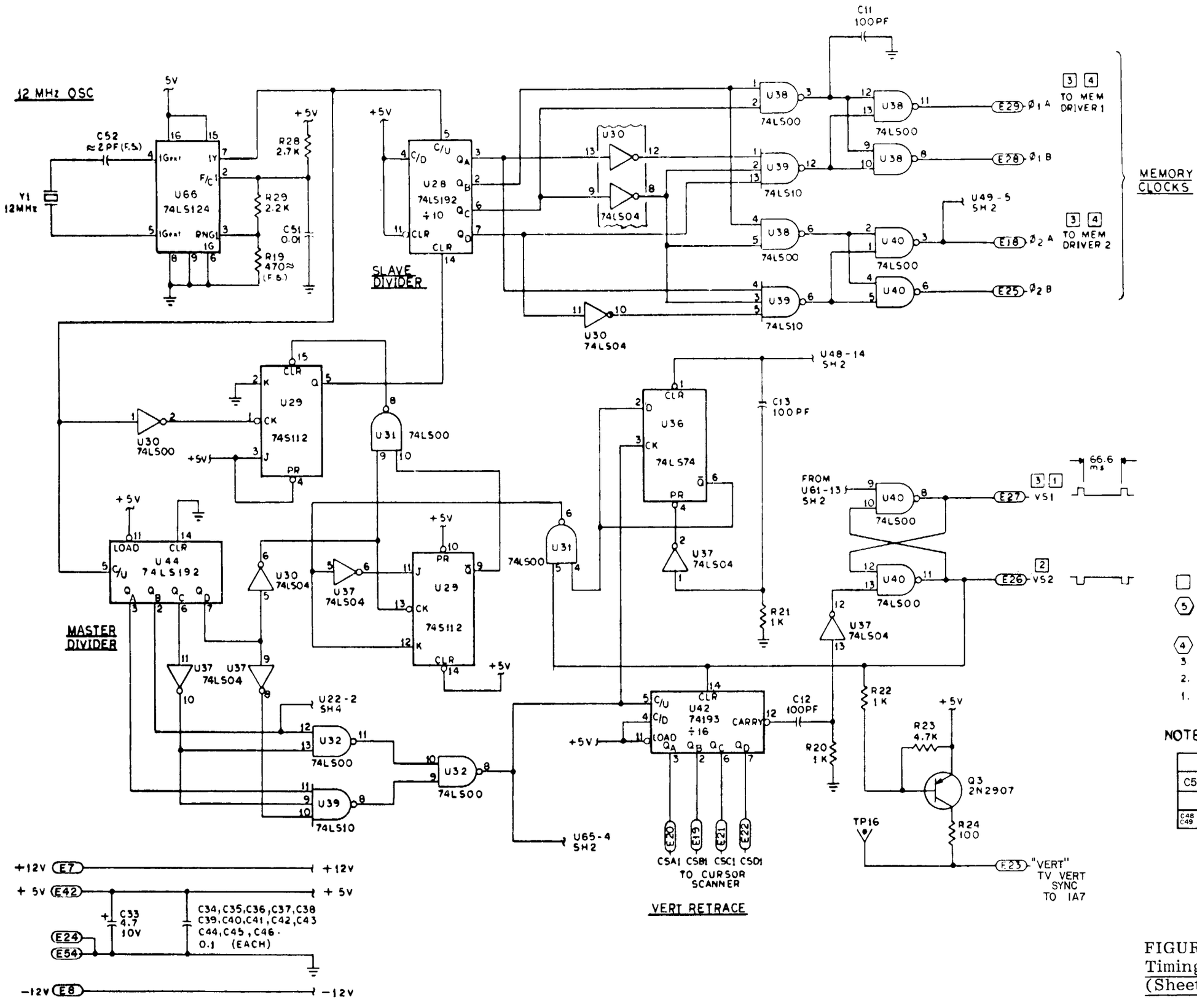


9 BIT CURSOR MULTIPLEXER

I Ø	MOVING CURSOR	
I 1	FIXED CURSOR	1
I 2		2
I 3		3
I 4		4
I 5		5
I 6	FIXED CURSOR	6
I 7	SPECTRUM ANALYZER LOAD LINE	

EL9TE085

FIGURE FO-14. Schematic Diagram, Cursor Storage and Readout Assy (6025-2001) (Sheet 6 of 6).



POWER DISTRIBUTION			
DEVICE	+5V	GND	-12V
74(LS) 00	14	7	
74LS02	14	7	
74LS03	14	7	
74LS04	14	7	
74LS10	14	7	
74LS74	14	7	
74(S)LS112	16	8	
74LS124	16	8	
74165	16	8	
74LS192	16	8	
74(LS)193	16	8	
F3257	24	12	23
93S46	16	8	
96LO2	16	8	

□ NUMBER IN SQUARE INDICATES LEAD GOING TO NEXT CORRESPONDING PCB.

(5) WITH E24 TO E25 IN PLACE 50 OR 100KHz SWEEP RATES ARE SELECTED BY ONE WIRE ON "100" LOW = 100KHz/SEC. HIGH = 50KHz/SEC.

(4) C3 & C4 MAY BE REPLACED WITH JUMPERS.

3. ALL CAPACITORS ARE IN MICROFARADS.

2. ALL RESISTORS ARE IN OHMS 1/4W, ±5%.

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSY DESIGNATION.

NOTES: UNLESS OTHERWISE SPECIFIED.

HIGHEST REFERENCE DESIGNATION								
C52	CR9	E25	Q3	R62	TP16	U66	Y1	
REF DESIGNATION NOT USED								
C48 C3 C49 C4								

EL9TE086

FIGURE FO-15. Schematic Diagram, Timing and Control Assy (6025-2002) (Sheet 1 of 5).

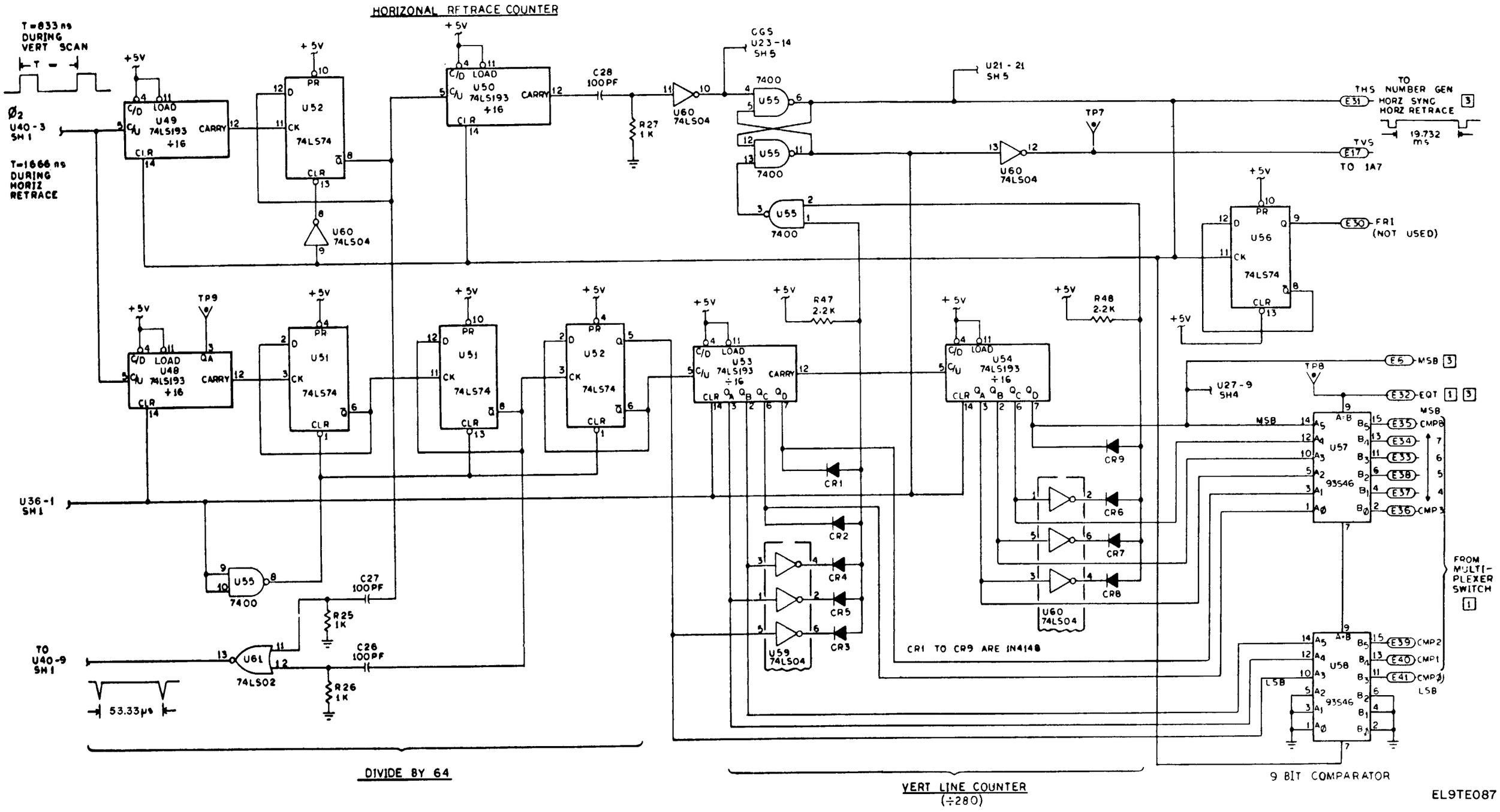
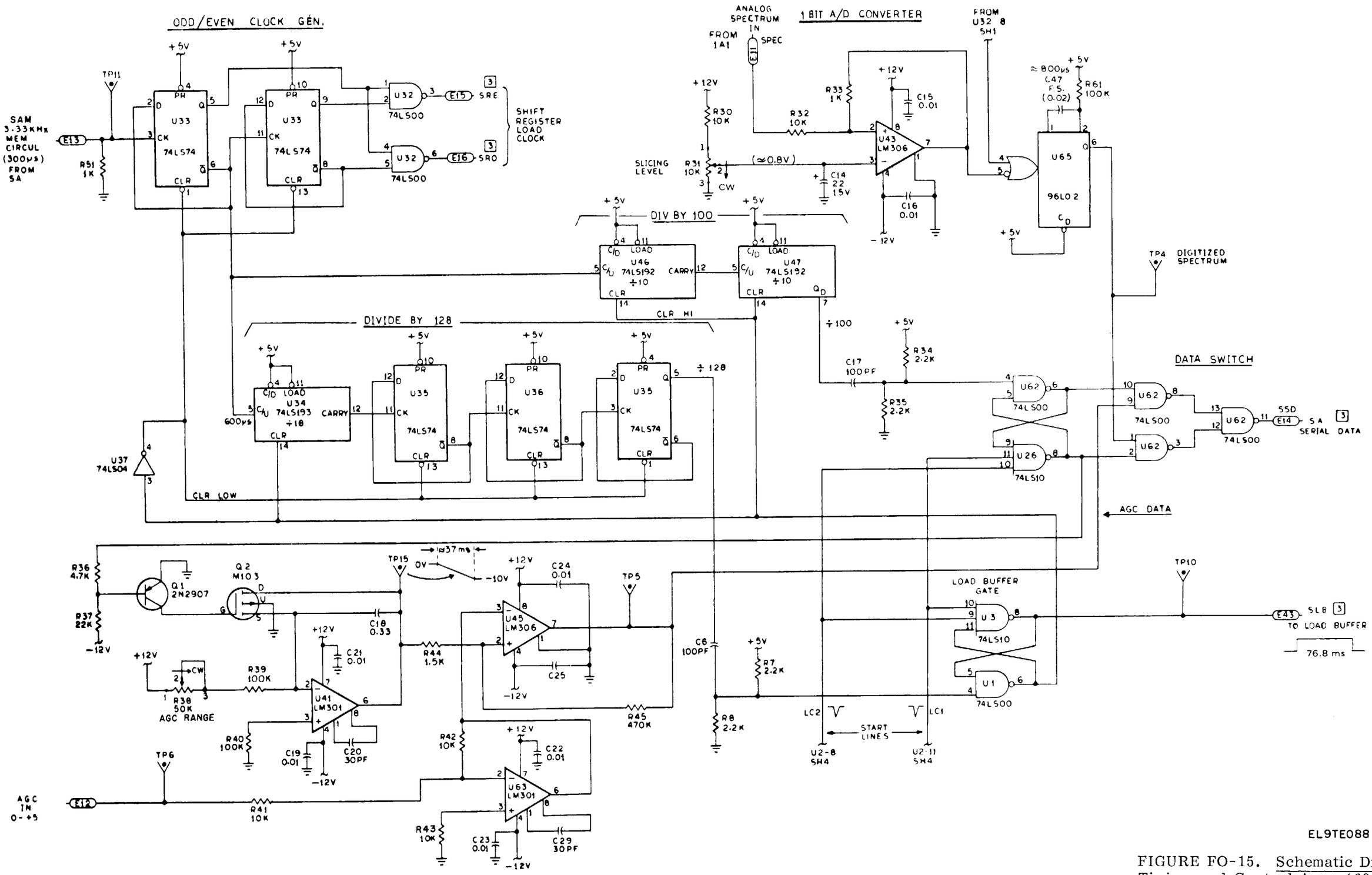


FIGURE FO-15. Schematic Diagram, Timing and Control Assy (6025-2002) (Sheet 2 of 5).



EL9TE088

AGC TO TIME CONVERTER

FIGURE FO-15. Schematic Diagram, Timing and Control Assy (6025-2002) (Sheet 3 of 5).

S/A TRIGGER RATE TABLE

SWEEP RATE KHz / SEC	UPPER LIMIT (UFL) 16MHz (50KHz/LINE) TIME	DIV RATIO	30MHz (100KHz LINE) TIME	DIV RATIO
50	1/SEC	100	0.5/SEC	200
100	2/SEC	50	1/SEC	100
200	4/SEC	25	2/SEC	50
500	10/SEC	10	5/SEC	20

DIVIDER PROGRAMING

100 Hz INPUT DIVIDED BY	U9 A	B	C	D	U10 A	B	C	D	DIVIDED BY 2	START PULSE ON
200	0	1	0	1	0	1	0	1	1	LC1
100	0	1	0	1	0	1	0	1	0	LC2
50	1	0	1	0	0	1	0	1	0	LC2
25	1	0	1	0	1	0	1	0	0	LC2
20	0	1	0	0	0	1	0	1	0	LC2
10	0	1	0	0	1	0	1	0	0	LC2

EL9TE089

FIGURE FO-15. Schematic Diagram, Timing and Control Assy (6025-2002) (Sheet 4 of 5).

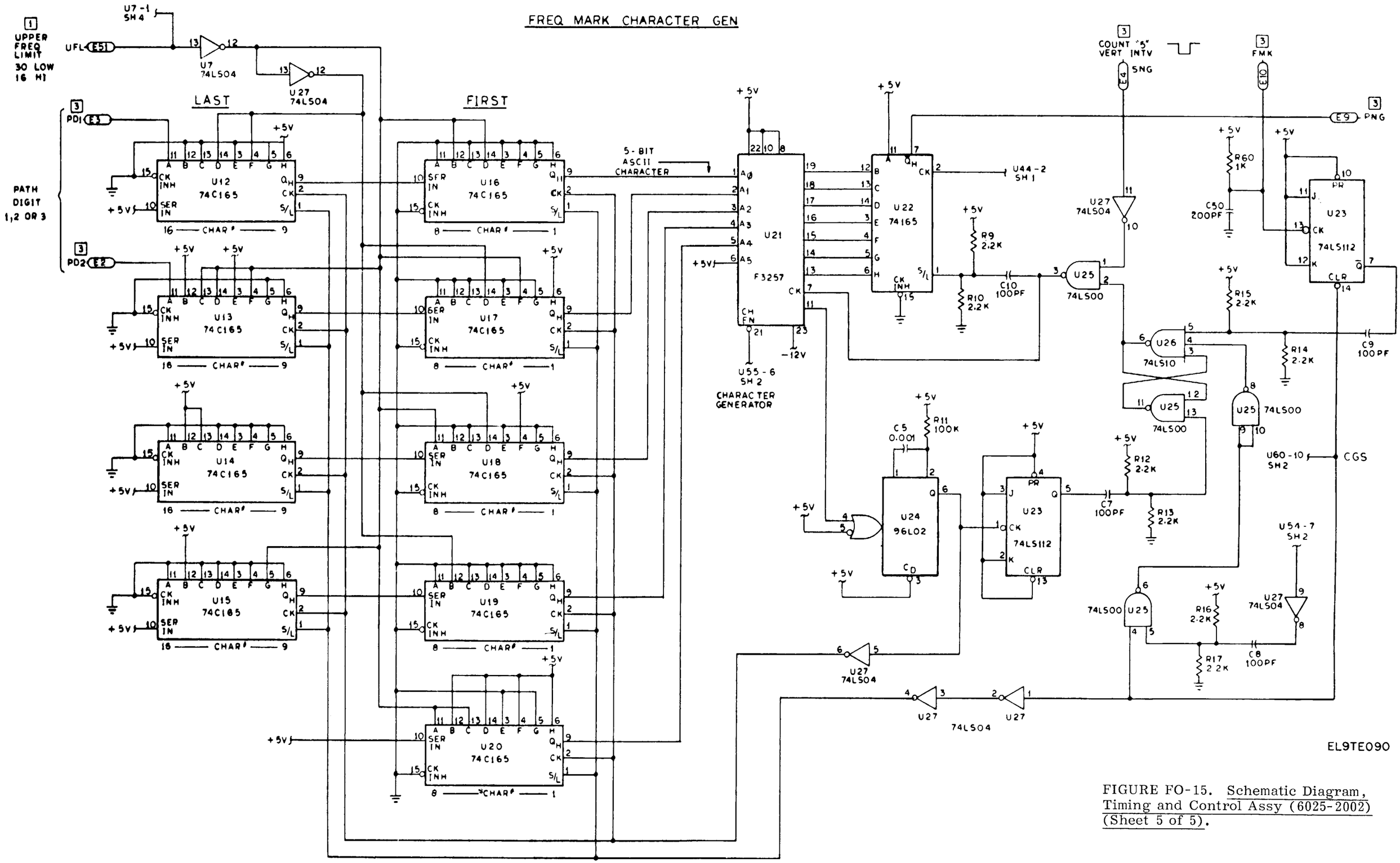
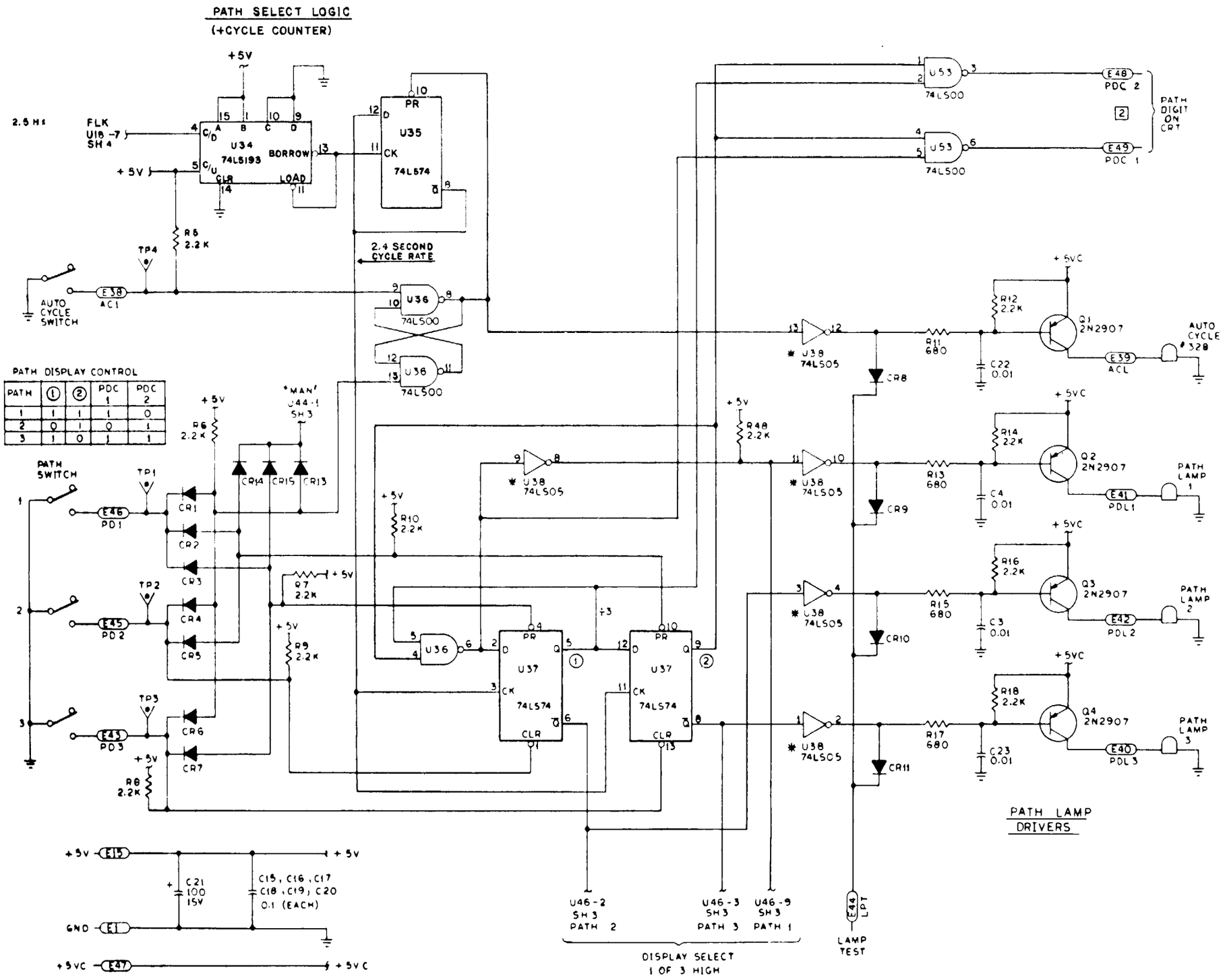


FIGURE FO-15. Schematic Diagram, Timing and Control Assy (6025-2002) (Sheet 5 of 5).



□ NUMBER IN SQUARE INDICATES LEAD GOING NEXT CORRESPONDING PCB.

POWER DISTRIBUTION		
DEVICE	+5V	GND
74LS00	14	7
74LS02	14	7
74LS03	14	7
74LS04	14	7
74LS05	14	7
74LS10	14	7
74LS26	14	7
7442	16	8
74LS74	14	7
74LS112	16	8
74LS192	16	8
74LS193	16	8
93L28	16	8
96LO2	16	8

5. * INDICATES OPEN COLLECTOR.
4. ALL DIODES ARE IN4148.
3. ALL CAPACITORS ARE IN MICROFARADS
2. ALL RESISTORS ARE IN OHMS 1/4W . ±5%
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSY DESIGNATION

HIGHEST REFERENCE DESIGNATION							
C26	CR15	E	04	R56	TP10	U55	
REF DESIGNATION NOT USED							
				R25			

EL9TE091

FIGURE FO-16. Schematic Diagram, Memory Load Logic Assy (6025-2003) (Sheet 1 of 5).

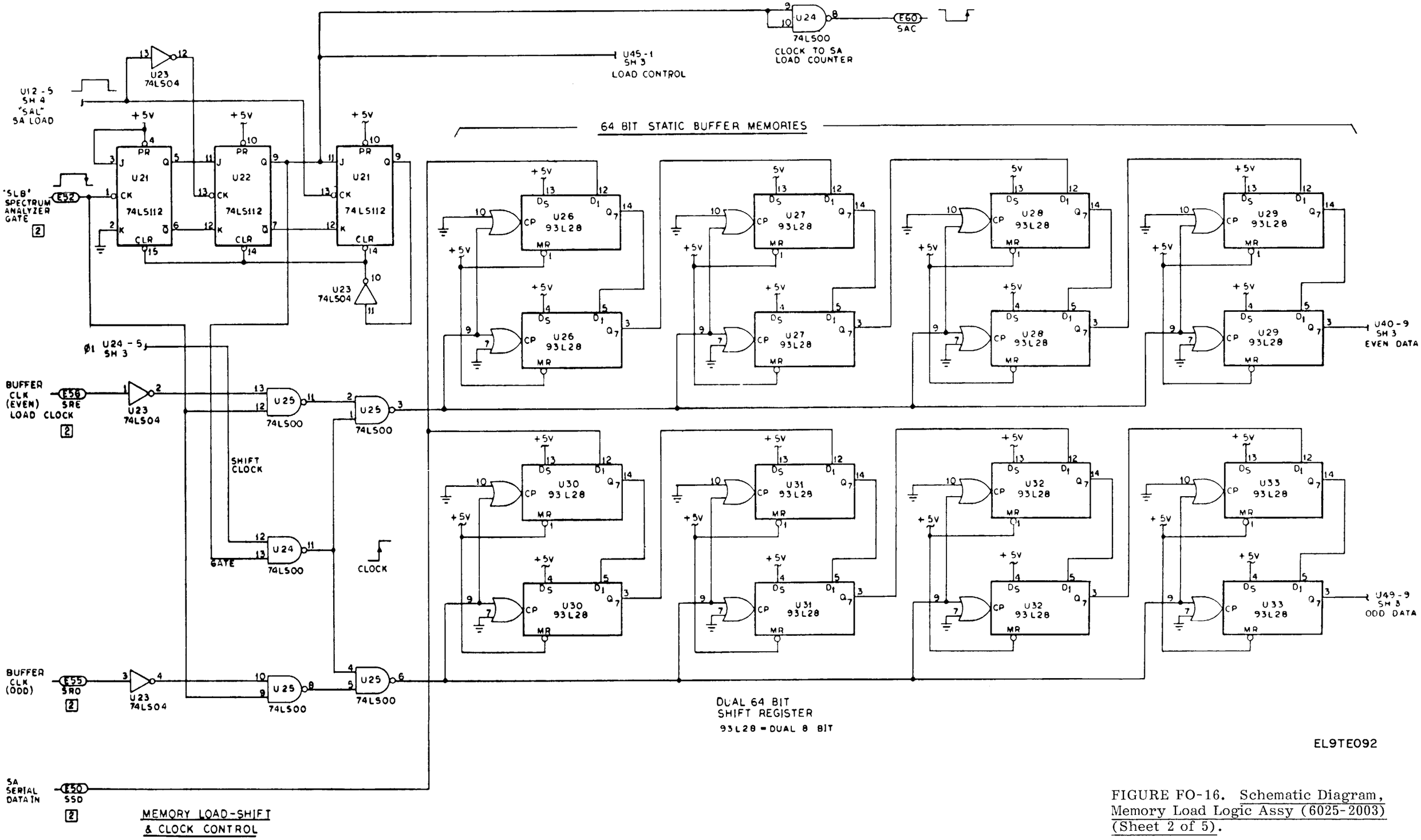
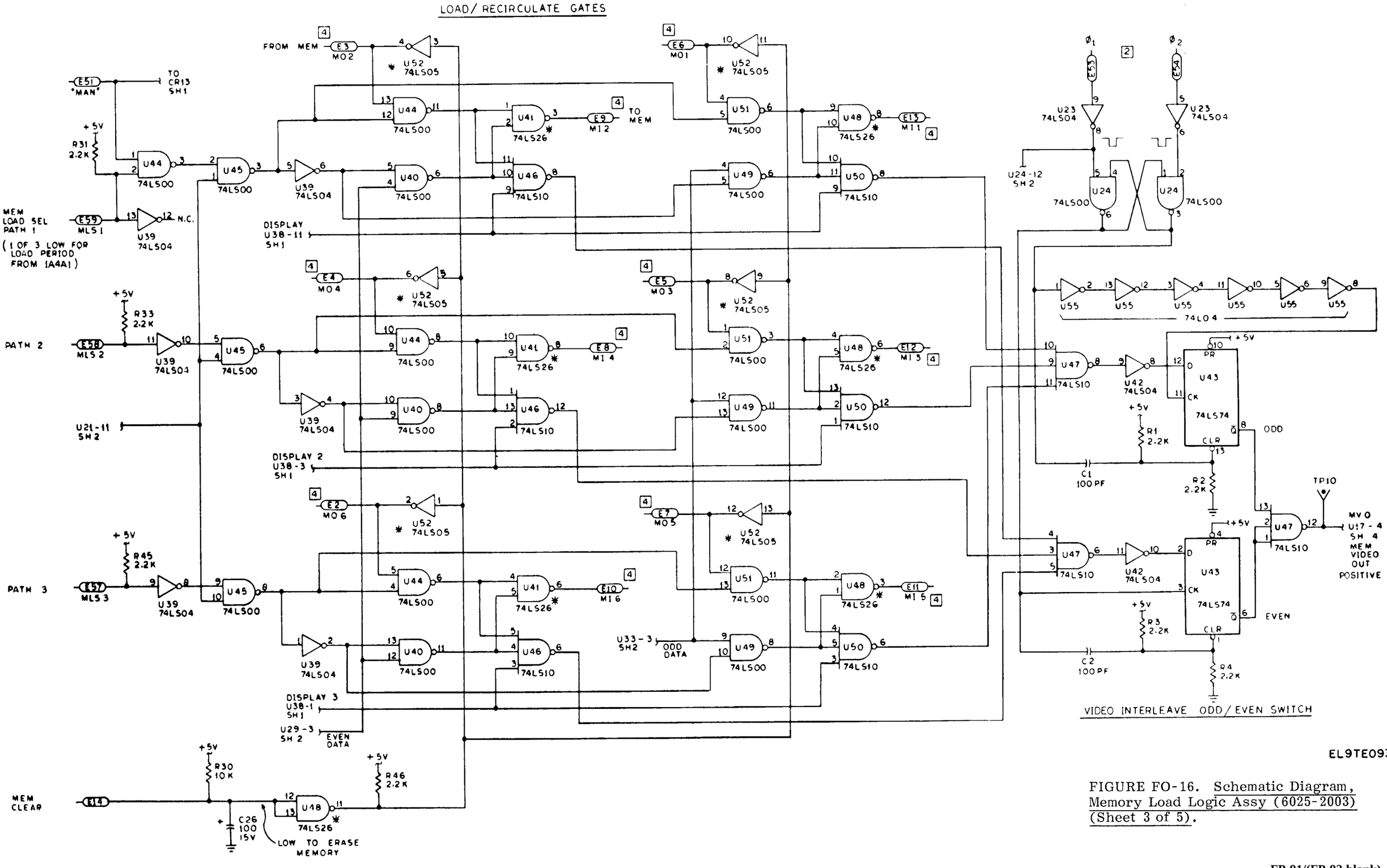


FIGURE FO-16. Schematic Diagram, Memory Load Logic Assy (6025-2003) (Sheet 2 of 5).



EL9TE093

FIGURE FO-16. Schematic Diagram, Memory Load Logic Assy (6025-2003) (Sheet 3 of 5).

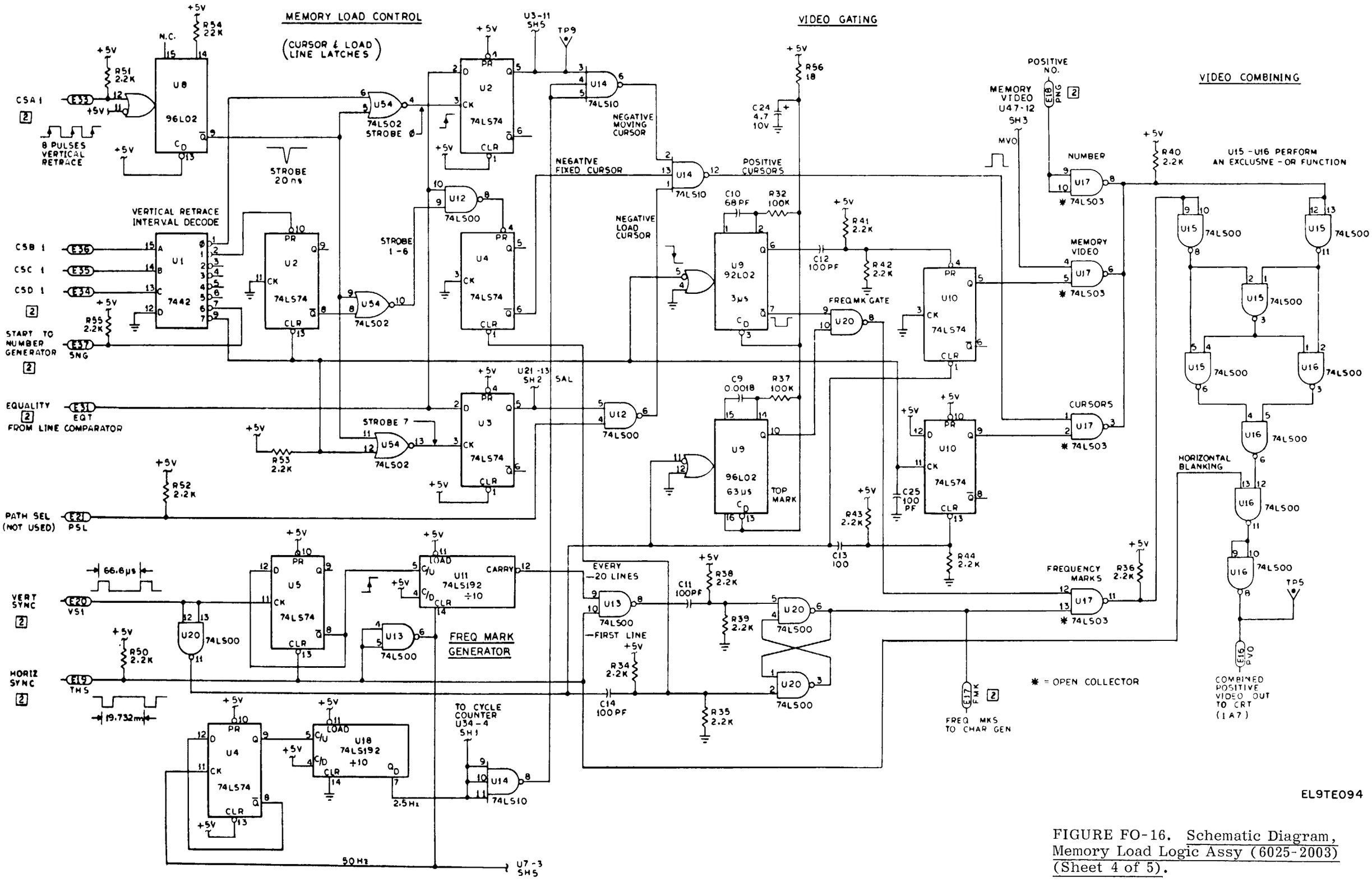
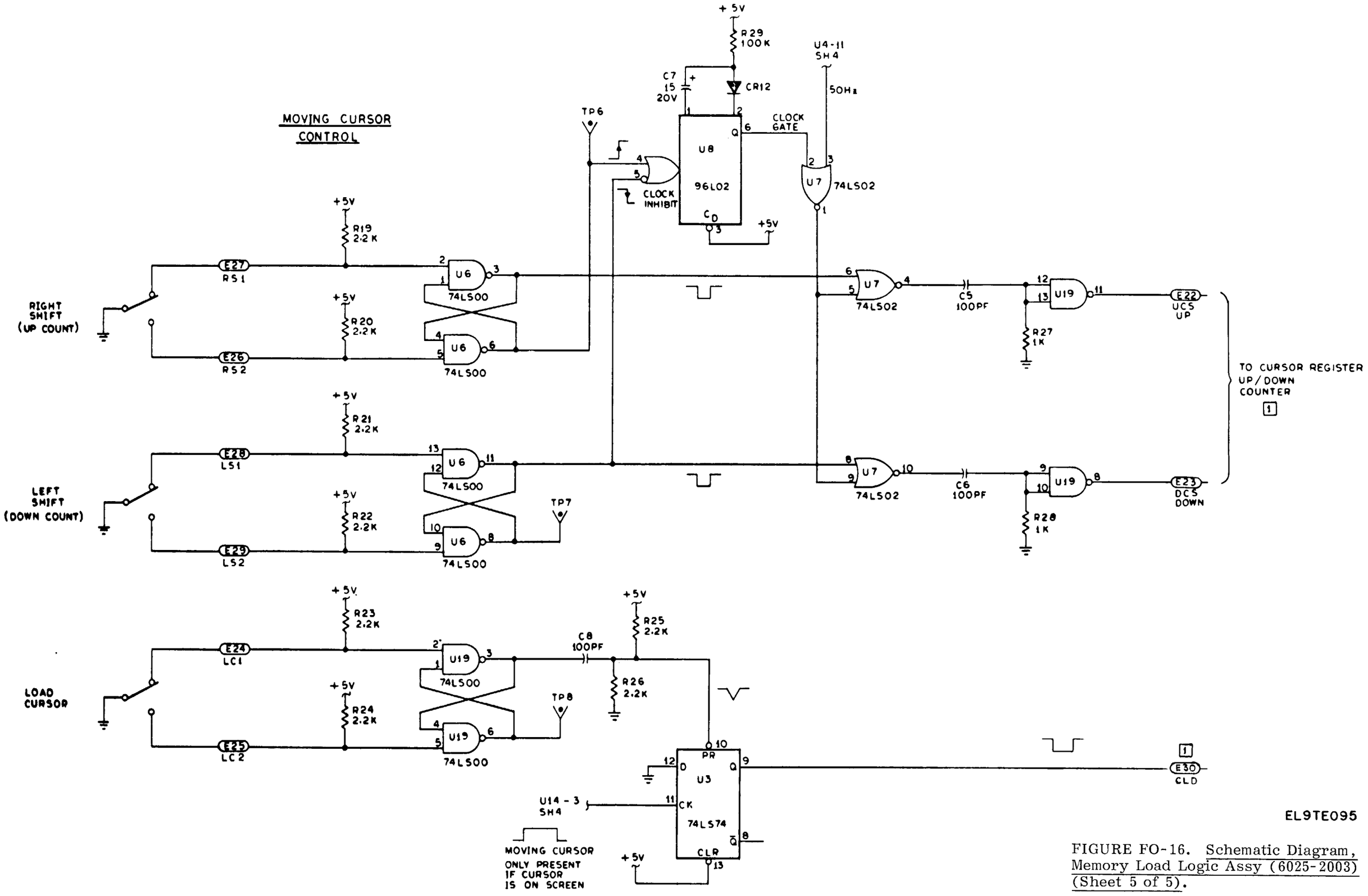
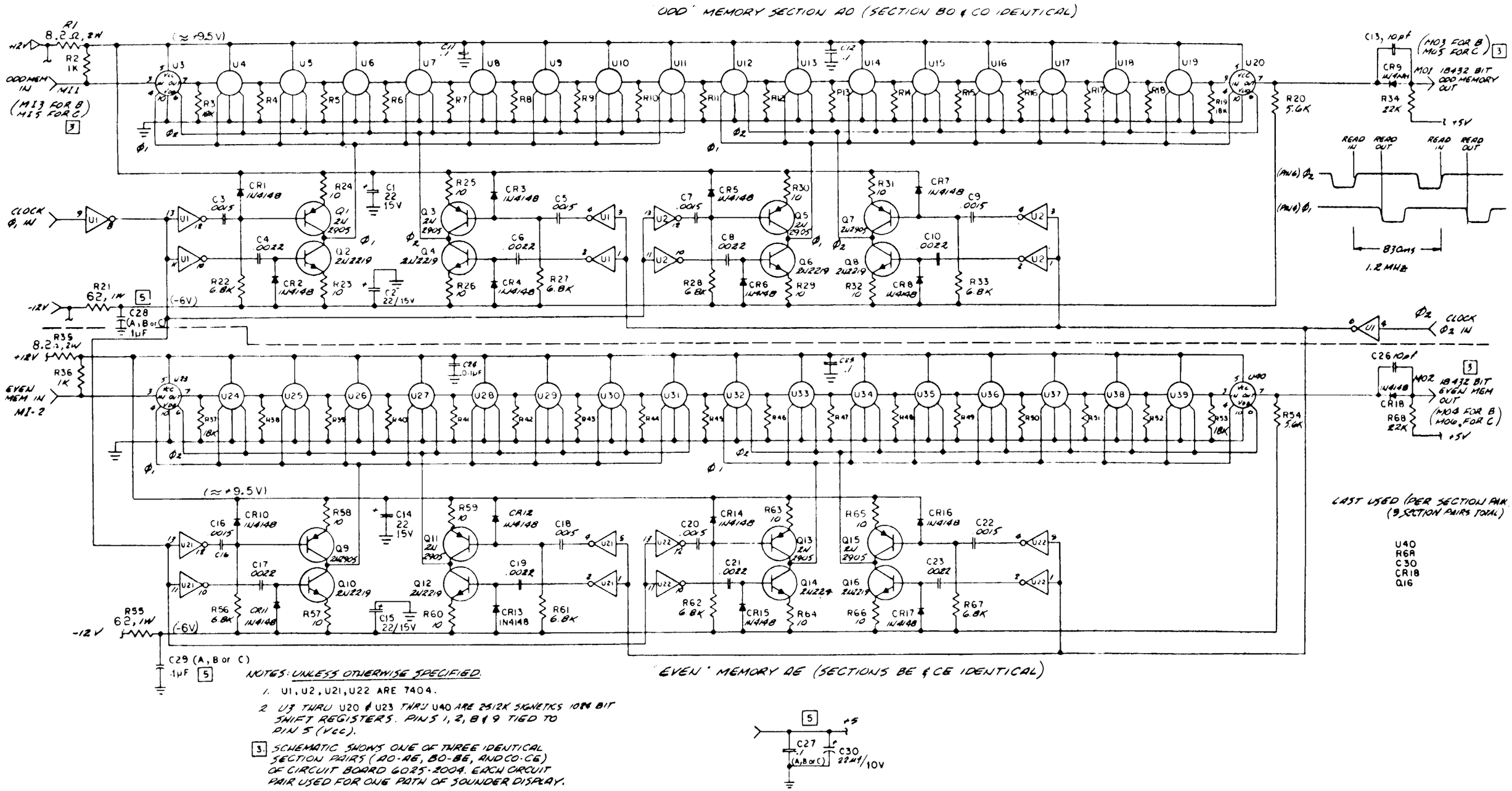


FIGURE FO-16. Schematic Diagram, Memory Load Logic Assy (6025-2003) (Sheet 4 of 5).



EL9TE095

FIGURE FO-16. Schematic Diagram, Memory Load Logic Assy (6025-2003) (Sheet 5 of 5).



NOTES: UNLESS OTHERWISE SPECIFIED.

1. U1, U2, U21, U22 ARE 7404.
2. U3 THRU U20 & U23 THRU U40 ARE 2512K SIGNETICS 100K BIT SHIFT REGISTERS. PINS 1, 2, 8 & 9 TIED TO PIN 5 (Vcc).
3. SCHEMATIC SHOWS ONE OF THREE IDENTICAL SECTION PAIRS (AO-AE, BO-BE, AND CO-CE) OF CIRCUIT BOARD 6025-2004. EACH CIRCUIT PAIR USED FOR ONE PATH OF SOUNDER DISPLAY.

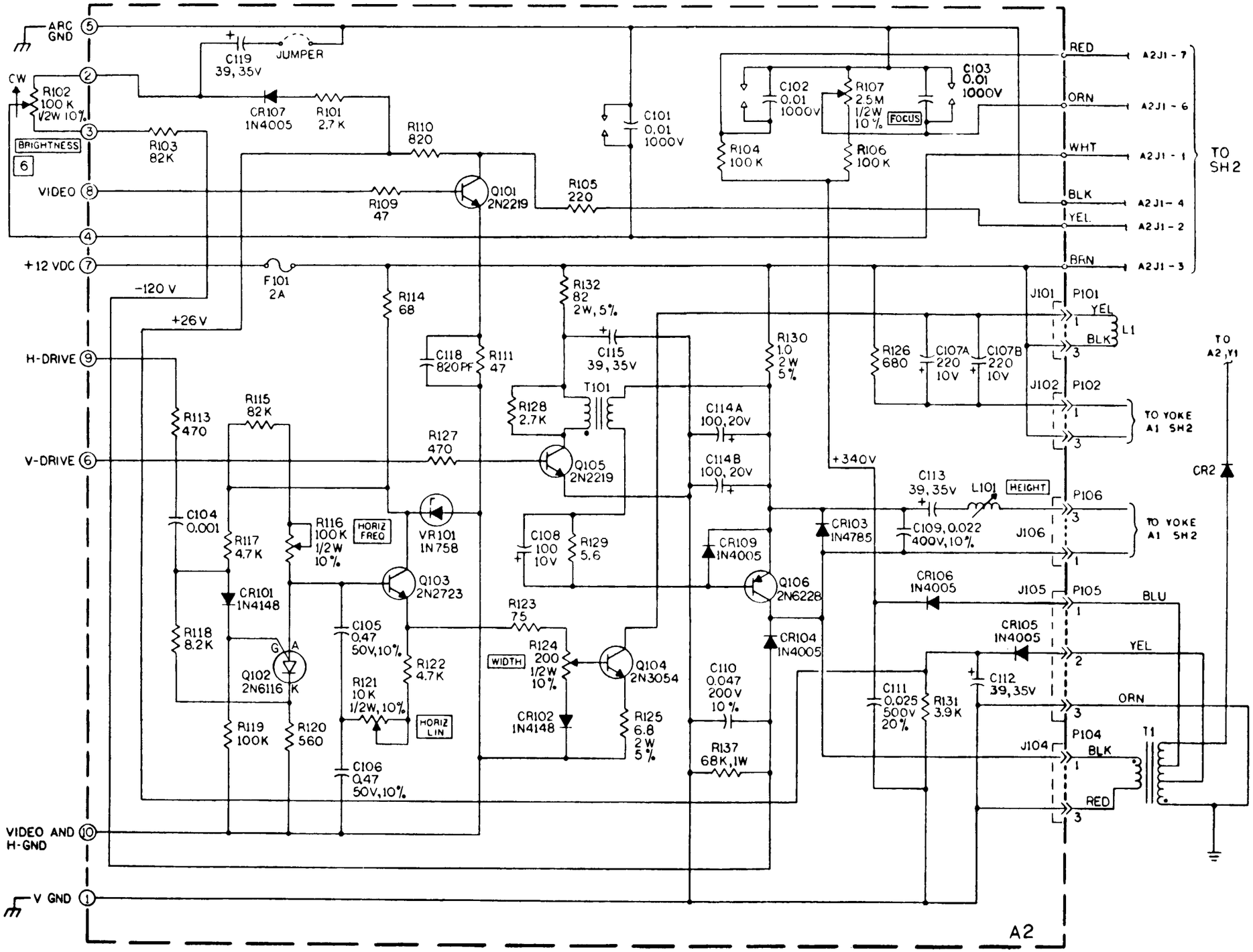
   PATH 1 = A = AO + AE
   2 = B = BO + BE
   3 = C = CO + CE

4. +12V SUPPLY SEPARATE FOR EACH SECTOR.
5. +5V COMMON TO ALL SECTIONS.
   C30 ONLY USED ONCE, COMMON TO ALL SECTIONS.
   C28 (A B or C) ONE PER SECTION.
   C29 (A B or C) ONE PER SECTION.
   C27 (A B or C) ONE PER SECTION.

"EVEN" MEMORY AE (SECTIONS BE & CE IDENTICAL)

EL9TE096

FIGURE FO-17. Schematic Diagram, CRT Display Memory Assy (6025-2004).



6 BRIGHTNESS POT (R102) IS MOUNTED ON PCB FOR -02 VERSION ONLY.

5 YOKE LEAD COLORS:
P106 BLUE AND RED LEADS,
P102 BROWN AND YELLOW LEADS.

4. CRT OPERATES WITH A VERTICAL RASTER.
3. ALL CAPACITORS ARE IN MICROFARADS.
2. ALL RESISTORS ARE IN OHMS 1/4W, ±5%.
1. REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX THE DESIGNATOR WITH UNIT OR ASSY DESIGNATOR.

NOTES: UNLESS OTHERWISE SPECIFIED.

HIGHEST REFERENCE DESIGNATION								
C119	CR109	F101	J106	L101	Q106	R137	T101	VR101

REF DESIGNATION NOT USED								
C116 C117	CR108		J103			R108,112 133,134 135,136		

EL9TE097

FIGURE FO-18. Schematic Diagram, CRT Drive Assy (6025-2010) (Sheet 1 of 2).

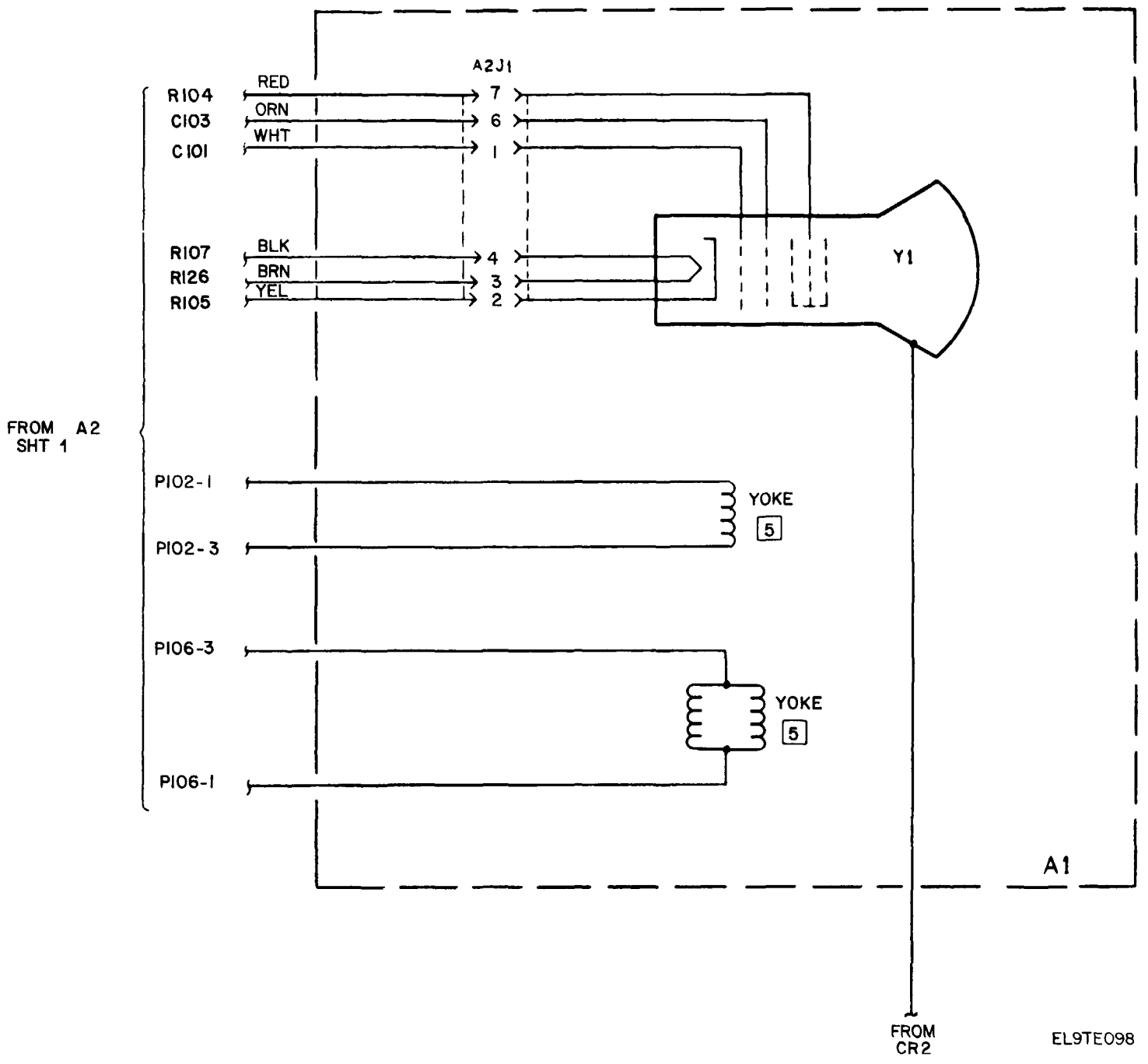
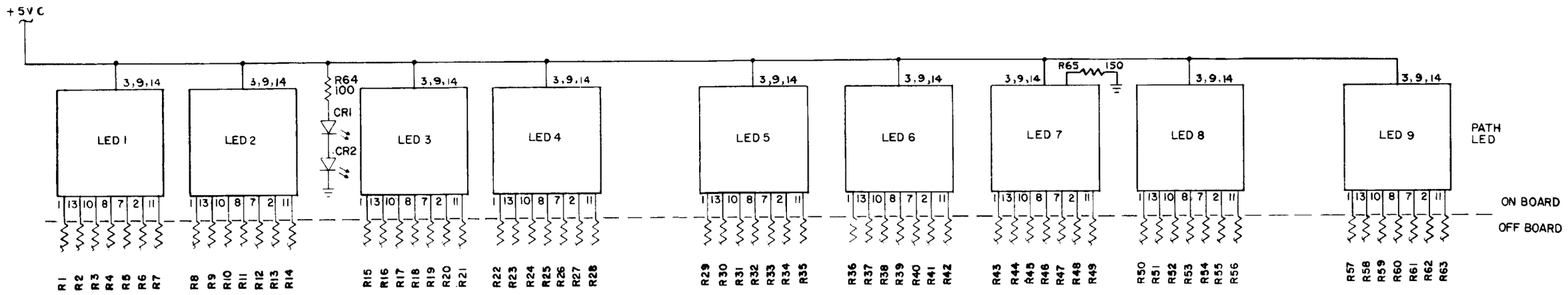
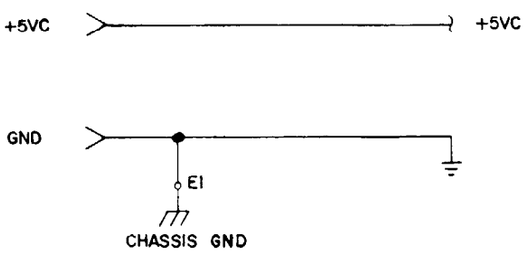


FIGURE FO-18. Schematic Diagram, CRT Drive Assy (6025-2010) (Sheet 2 of 2).





NOTES: UNLESS OTHERWISE SPECIFED.
1. R1 THRU R63 ARE 120 OHMS, 1/4W, 5%.
2. LEDS ARE LITRONIX DL707.
3. CR1 & CR2 ARE RL 50.

EL9TE099

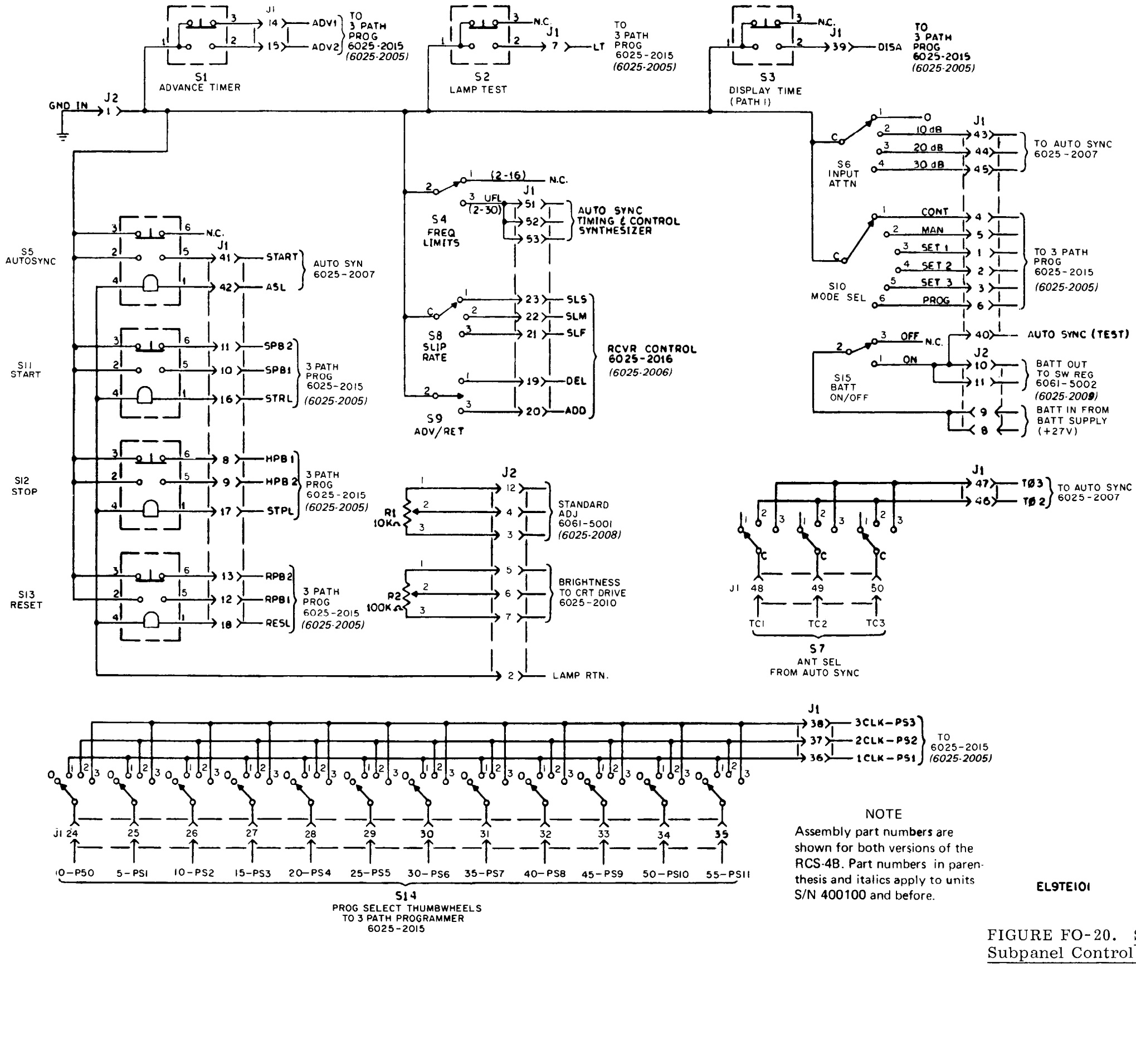
FIGURE FO-19. Schematic Diagram, Numeric Display Assy (6025-1009) (Sheet 1 of 2).

NOTES: UNLESS OTHERWISE SPECIFIED.

1. R1 THRU R63 ARE 120 OHMS, 1/4 W, 5%.
2. U1 THRU U8 ARE 7447'S.

EL9TE100

FIGURE FO-19. Schematic Diagram, Numeric Display Assy (6025-1009) (Sheet 2 of 2).

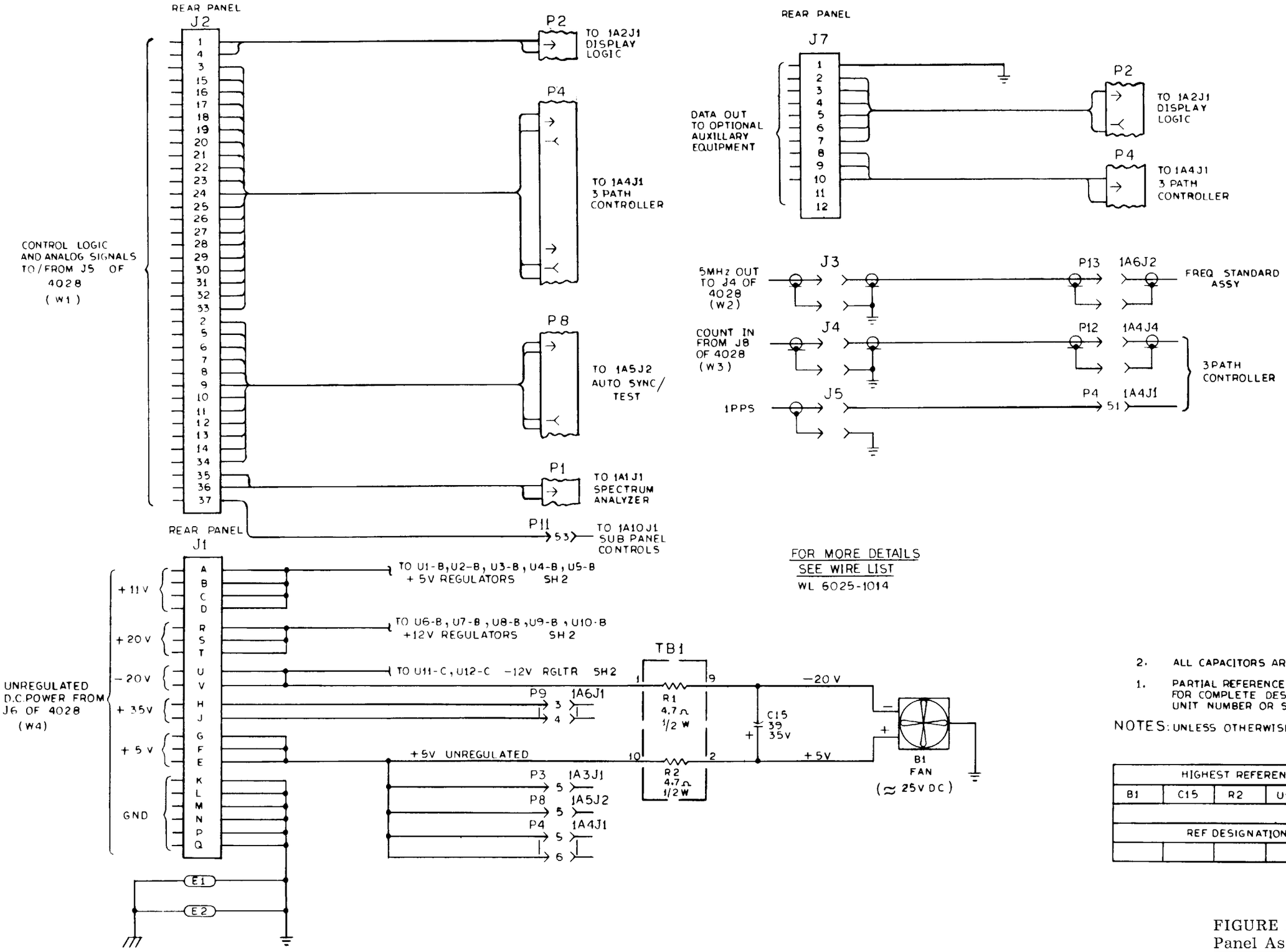


NOTE

Assembly part numbers are shown for both versions of the RCS-4B. Part numbers in parenthesis and italics apply to units S/N 400100 and before.

EL9TE101

FIGURE FO-20. Schematic Diagram, Subpanel Control (6025-1010).



2. ALL CAPACITORS ARE IN MICROFARADS.

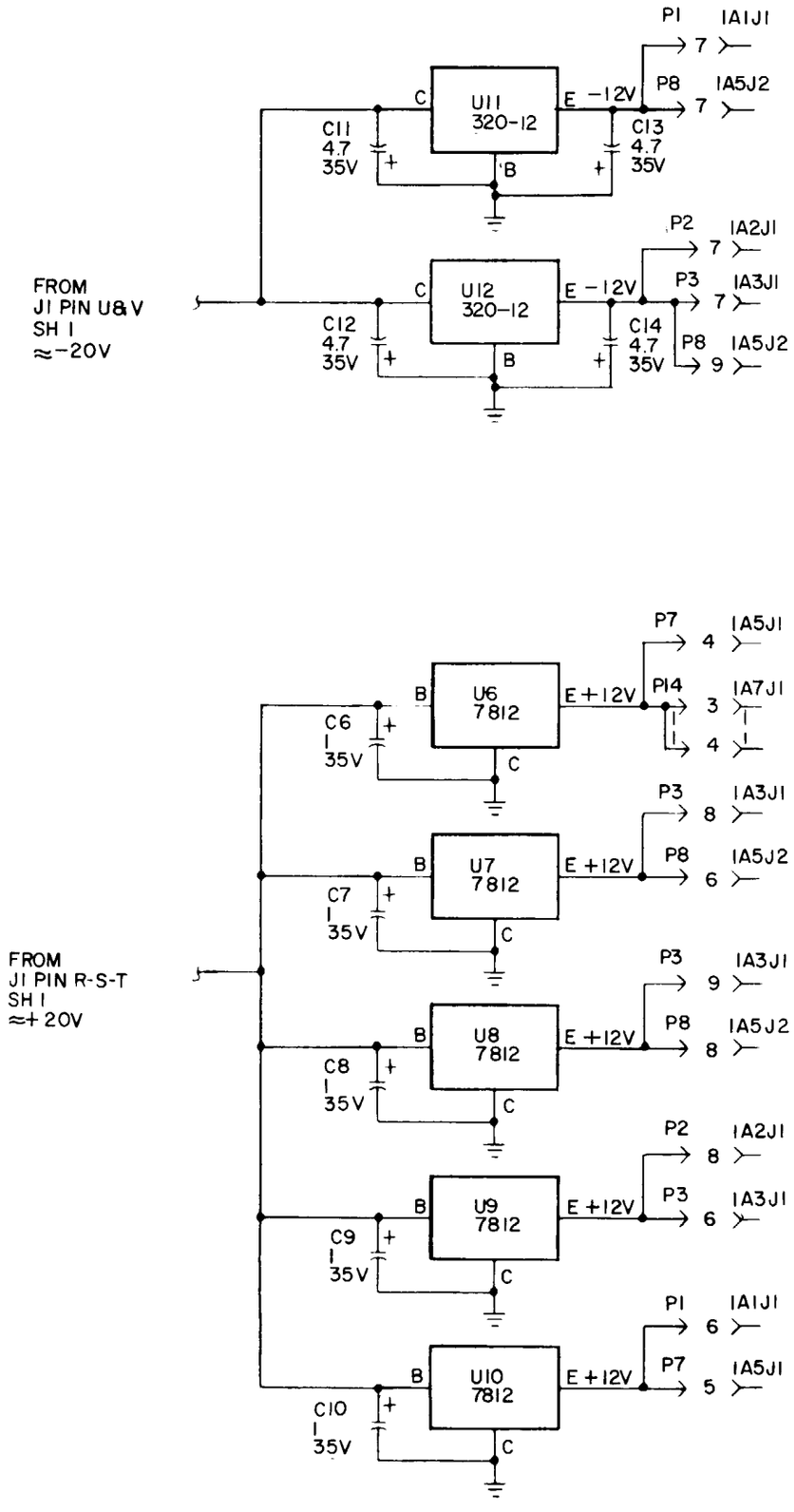
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSY DESIGNATION.

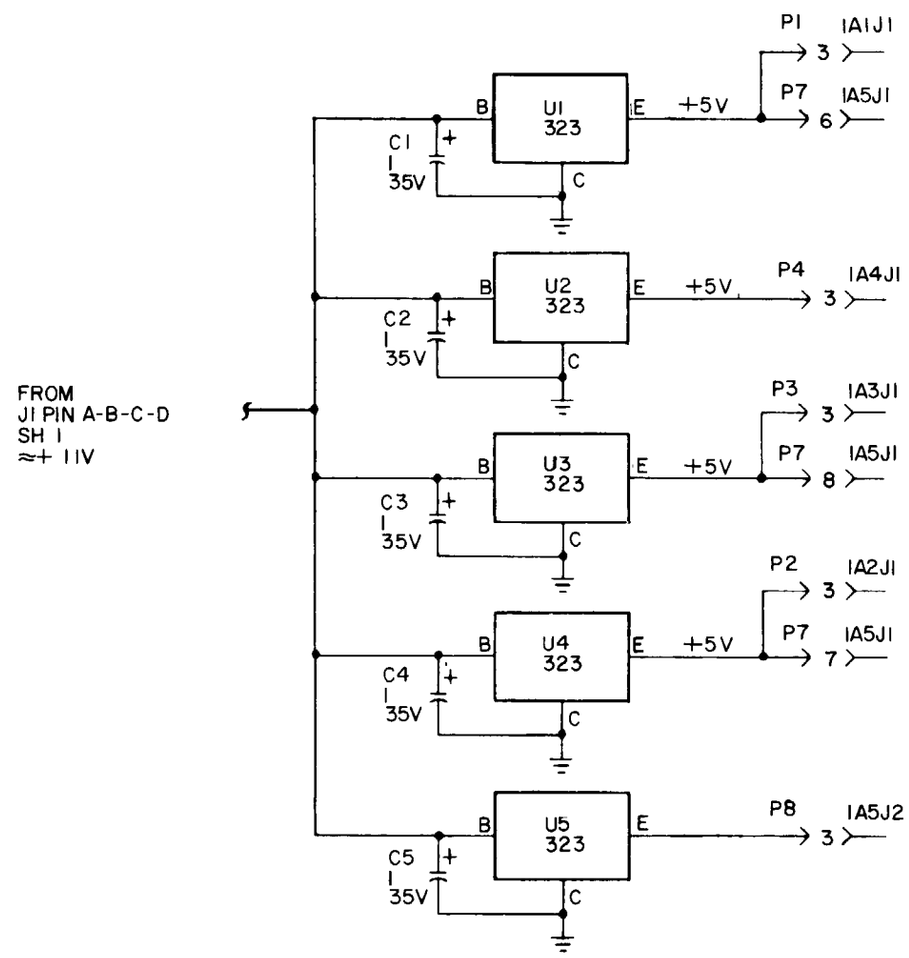
NOTES: UNLESS OTHERWISE SPECIFIED.

HIGHEST REFERENCE DESIGNATION						
B1	C15	R2	U12	J7	TB1	
REF DESIGNATIONS NOT USED						
				J6		

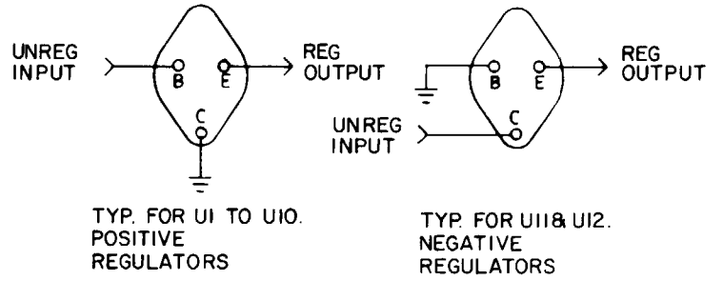
EL9TE102

FIGURE FO-21. Schematic Diagram, Rear Panel Assy (6025-1014) (Sheet 1 of 2).





P1 CONNECTS TO 1A1 SPECTRUM ANALYZER
P2 1A2 DISPLAY LOGIC
P3 1A3 DISPLAY MEMORY
P4 1A4 3 PATH CONTROLLER
P7 1A5 AUTO SYNC/TEST
P8
P14 CONNECTS TO 1A7 CART DISPLAY



EL9TE103

FIGURE FO-21. Schematic Diagram, Rear Panel Assy (6025-1014) (Sheet 2 of 2).

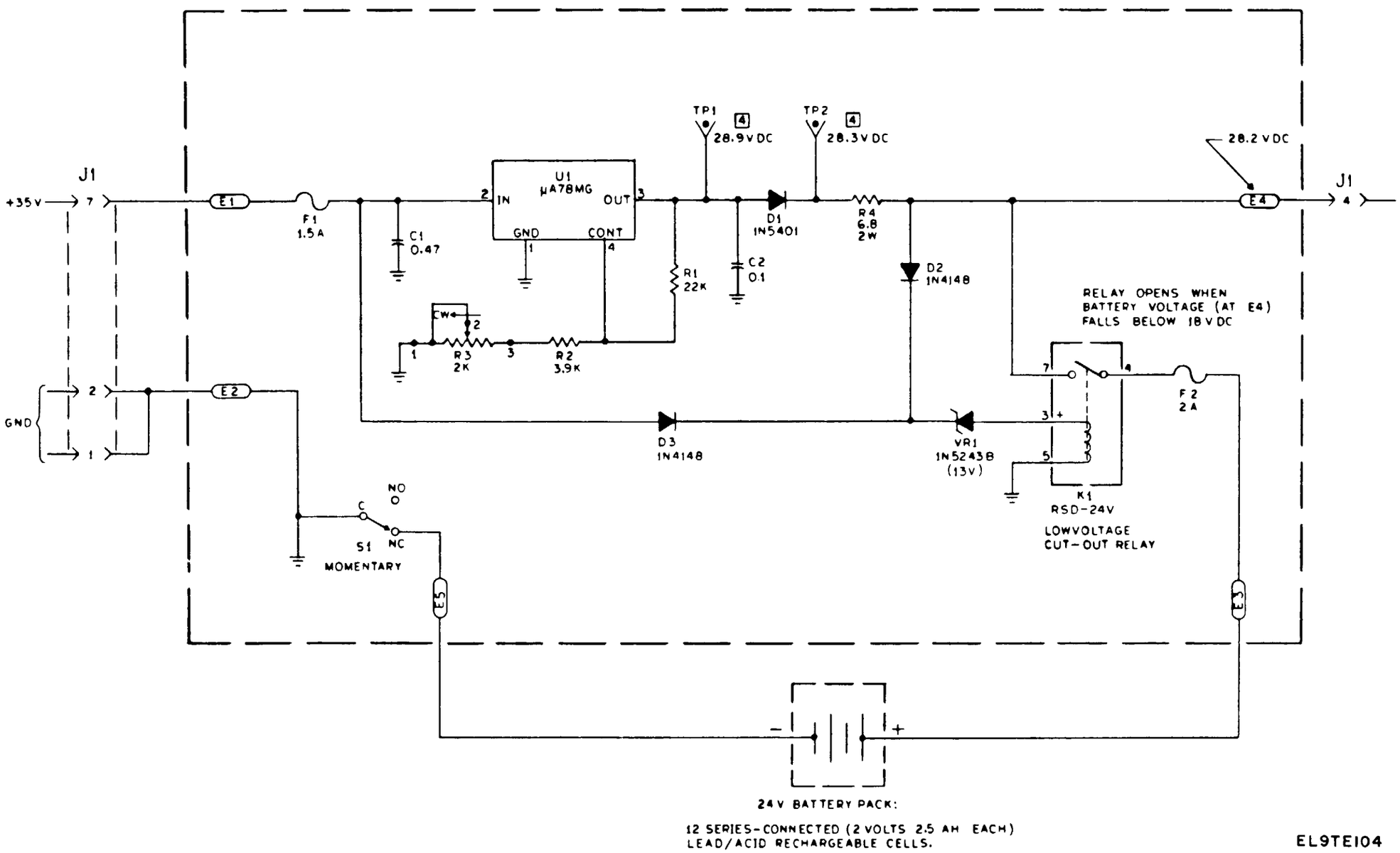
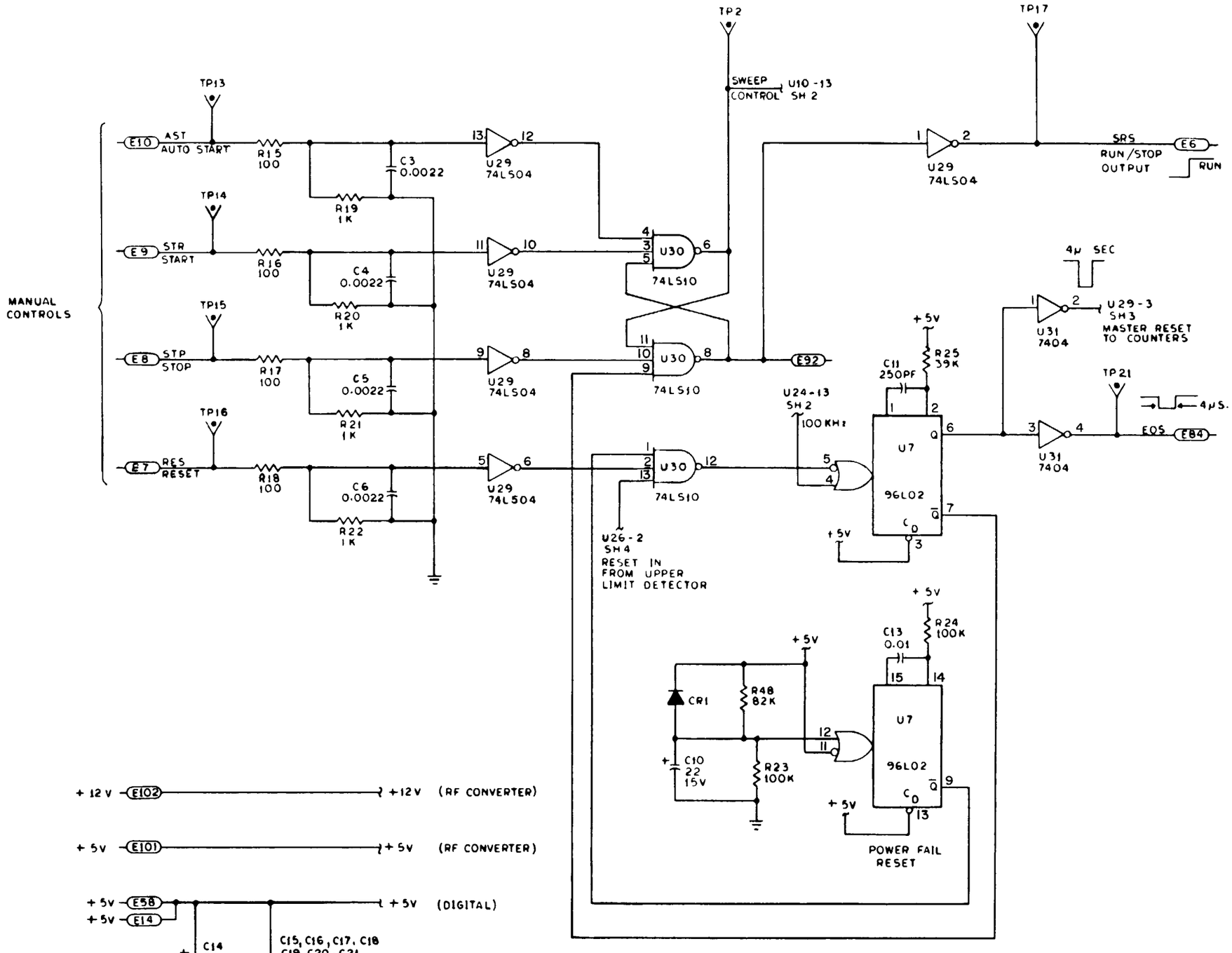


FIGURE FO-22. Schematic Diagram, Rechargeable Battery Supply (6025-1018).



POWER DISTRIBUTION		
DEVICE	+5v	GND
74LS(S)00	14	7
74(LS)04	14	7
74LS10	14	7
74LS20	14	7
74LS85	16	8
74LS112	16	8
74LS192	16	8
74LS257	16	8
96L02	16	8

6. W1 THRU W22 JUMPERS INSTALLED AS SHOWN.
5. T1, T2, & T3 WATKINS JOHNSON BALANCED TRANSFORMERS BT8.
4. ALL DIODES ARE IN4148.
3. ALL CAPACITORS ARE IN MICROFARADS.
2. ALL RESISTORS ARE IN OHMS 1/4 W, ±5%.
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSY DESIGNATION.

NOTES: UNLESS OTHERWISE SPECIFIED.

HIGHEST REFERENCE DESIGNATION								
C21 C154	CR14	F93 E110	J106 K101	L112 M101	Q105 T104	R60 R169	TP22 TP105	U42 U105
REF DESIGNATION NOT USED								
C103 C137 C149						R56, R141-R143 R153-154, R157		U41

EL9TE105

FIGURE FO-23. Schematic Diagram, Synth Converter Assy (5030-2001) (Sheet 1 of 6).

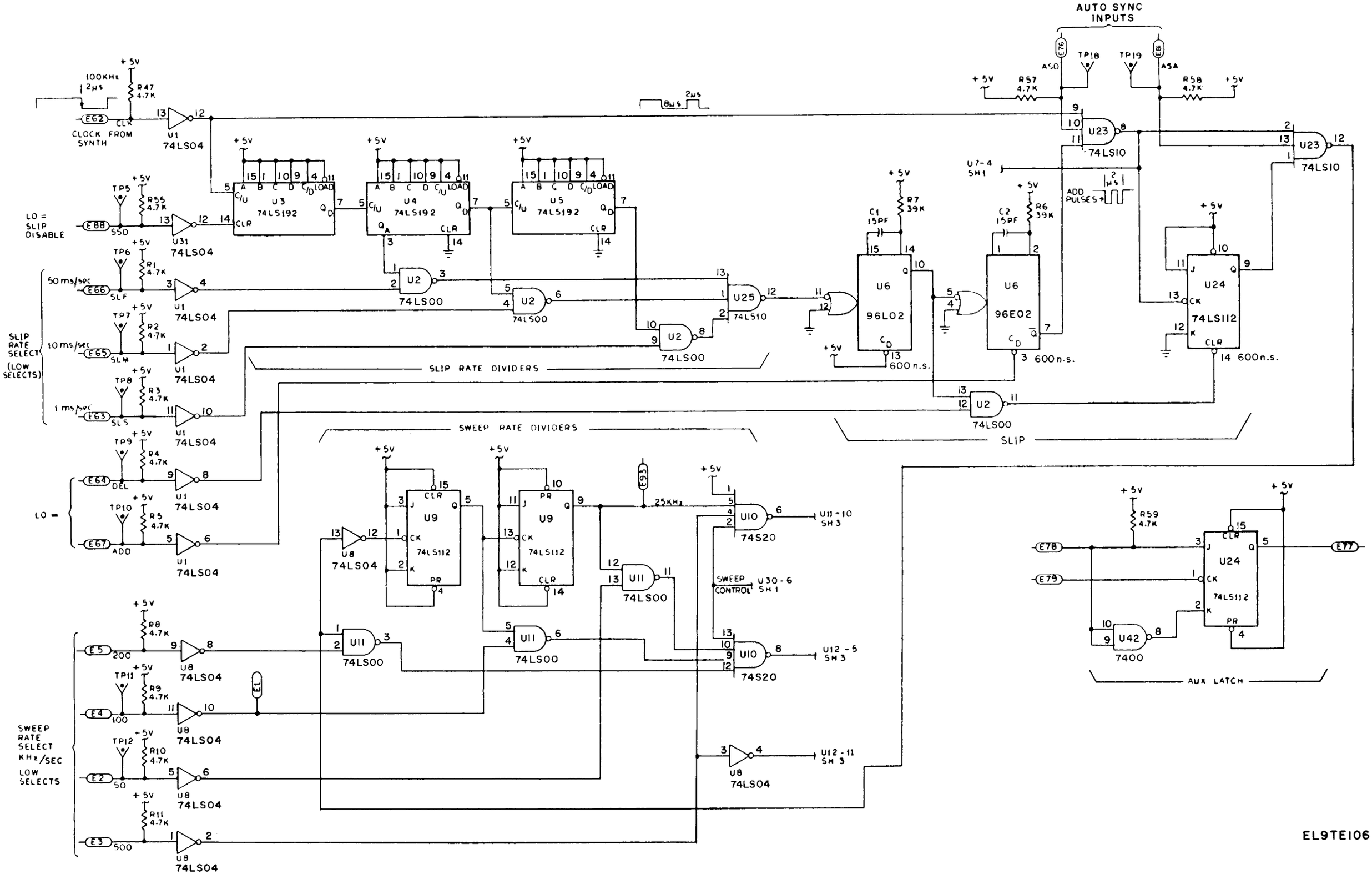


FIGURE FO-23. Schematic Diagram, Synth Converter Assy (5030-2001) (Sheet 2 of 6).

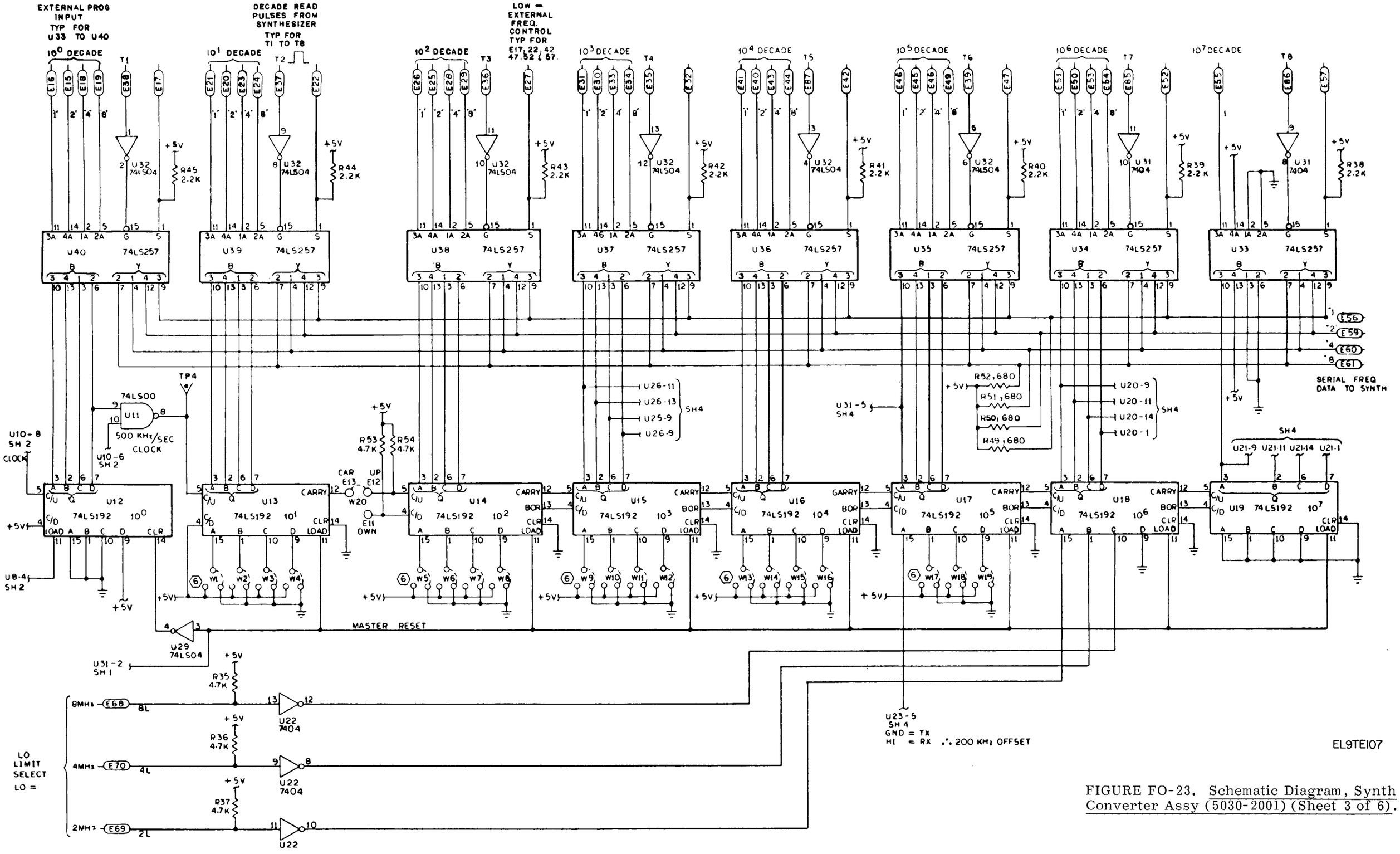


FIGURE FO-23. Schematic Diagram, Synth Converter Assy (5030-2001) (Sheet 3 of 6).

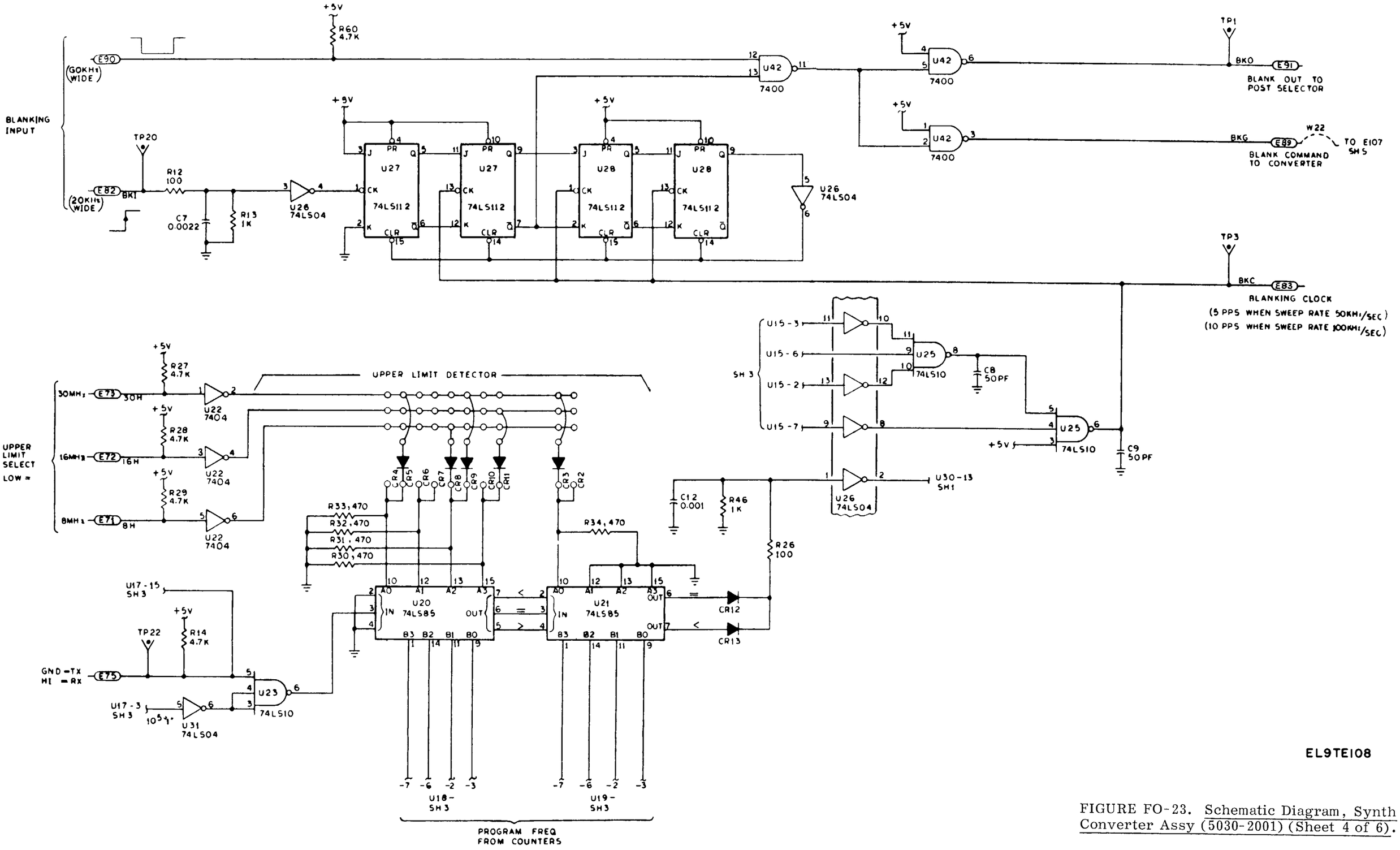


FIGURE FO-23. Schematic Diagram, Synth Converter Assy (5030-2001) (Sheet 4 of 6).

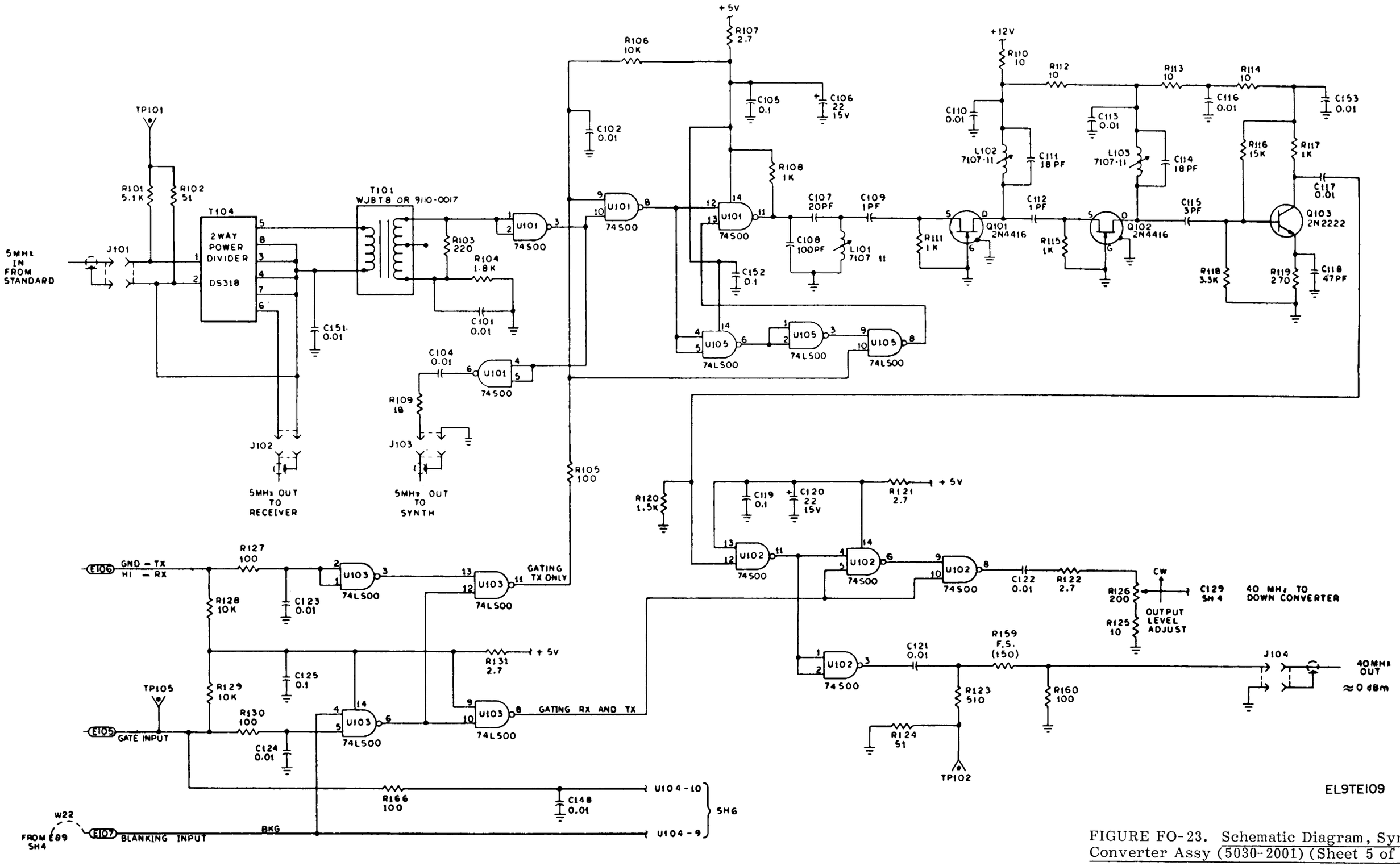
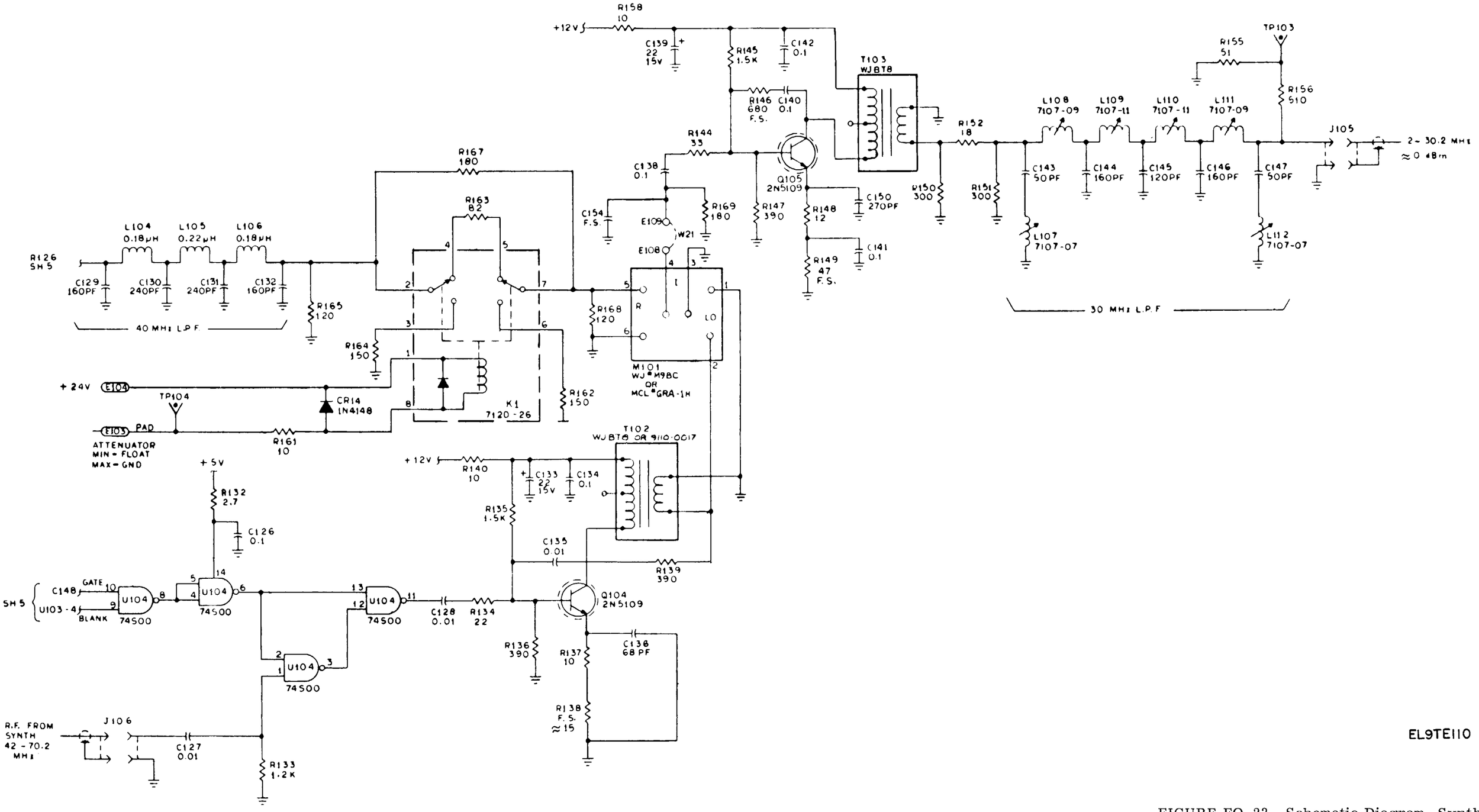
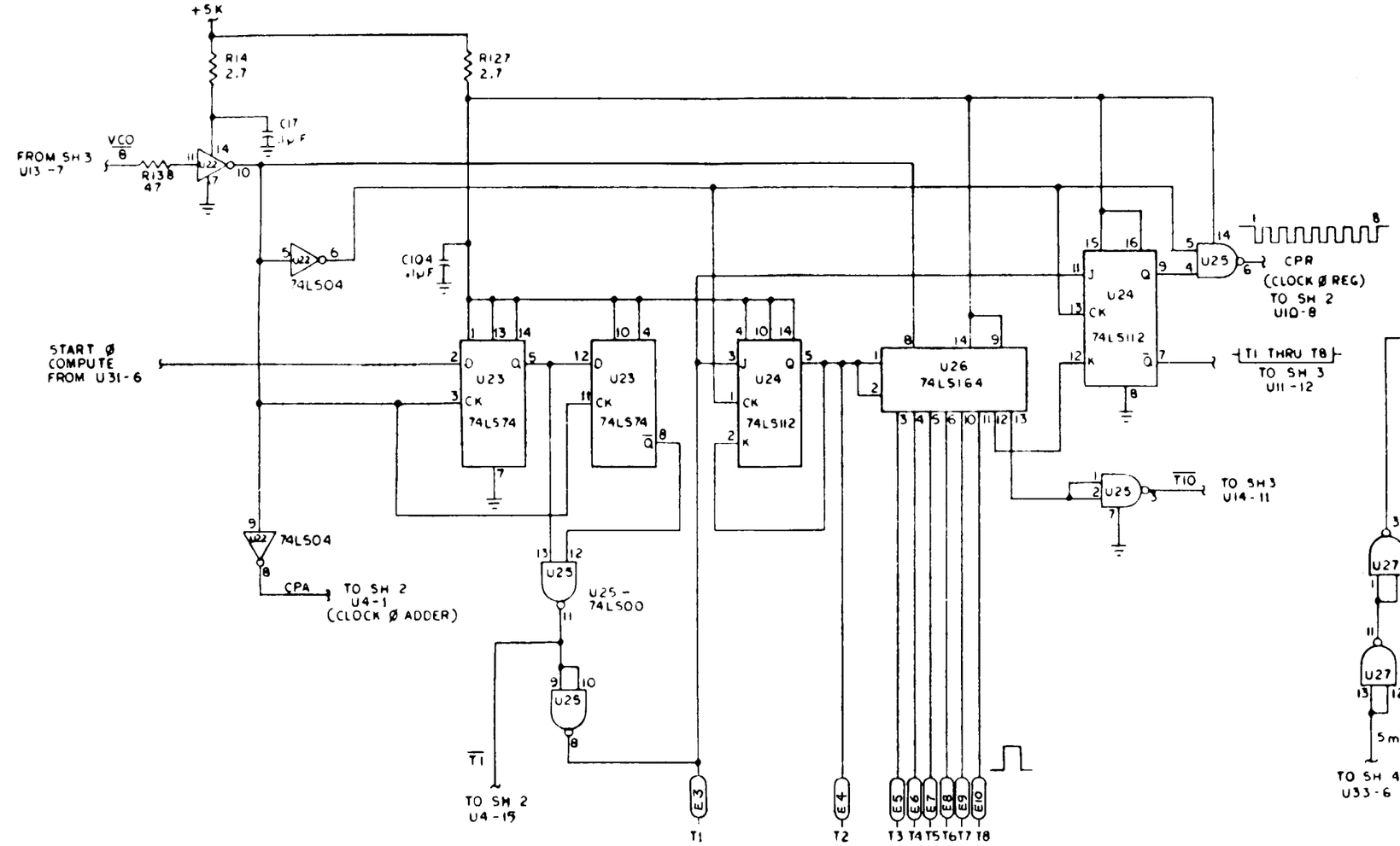


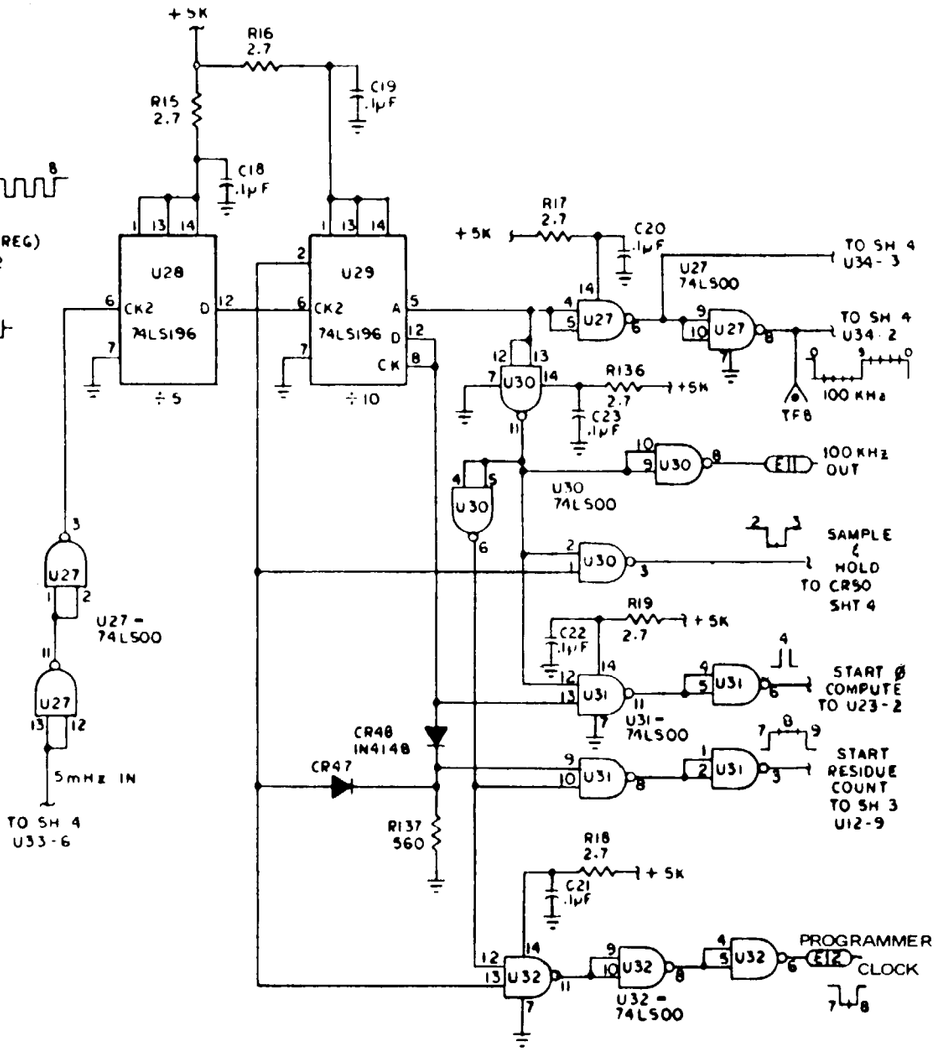
FIGURE FO-23. Schematic Diagram, Synth Converter Assy (5030-2001) (Sheet 5 of 6).

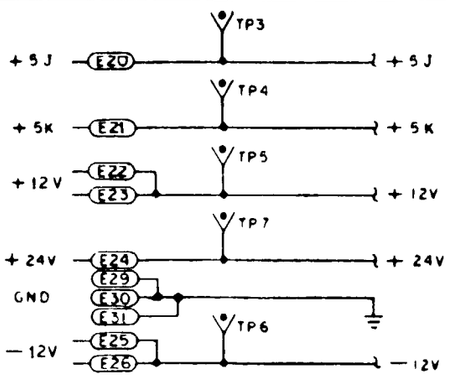


EL9TE110

FIGURE FO-23. Schematic Diagram, Synth Converter Assy (5030-2001) (Sheet 6 of 6).







TIMING GENERATOR

REF ÷

NOTE: UNLESS OTHERWISE SPECIFIED.
1. ALL RESISTORS ARE IN OHMS, 5% 1/4 W.
2. ALL CAPACITORS ARE IN MICROFARADS.
3. Q15 & Q16 ARE NOT USED.

HIGHEST REFERENCE DESIGNATION								
E28	C117	CR57	L13	Q17	R150	TP9	U52	T1
REF. DESIGNATION NOT USED								
	U37	U41						

EL9TE111

FIGURE FO-24. Schematic Diagram, Microphase Synthesizer Assy (5030-2002) (Sheet 1 of 5).

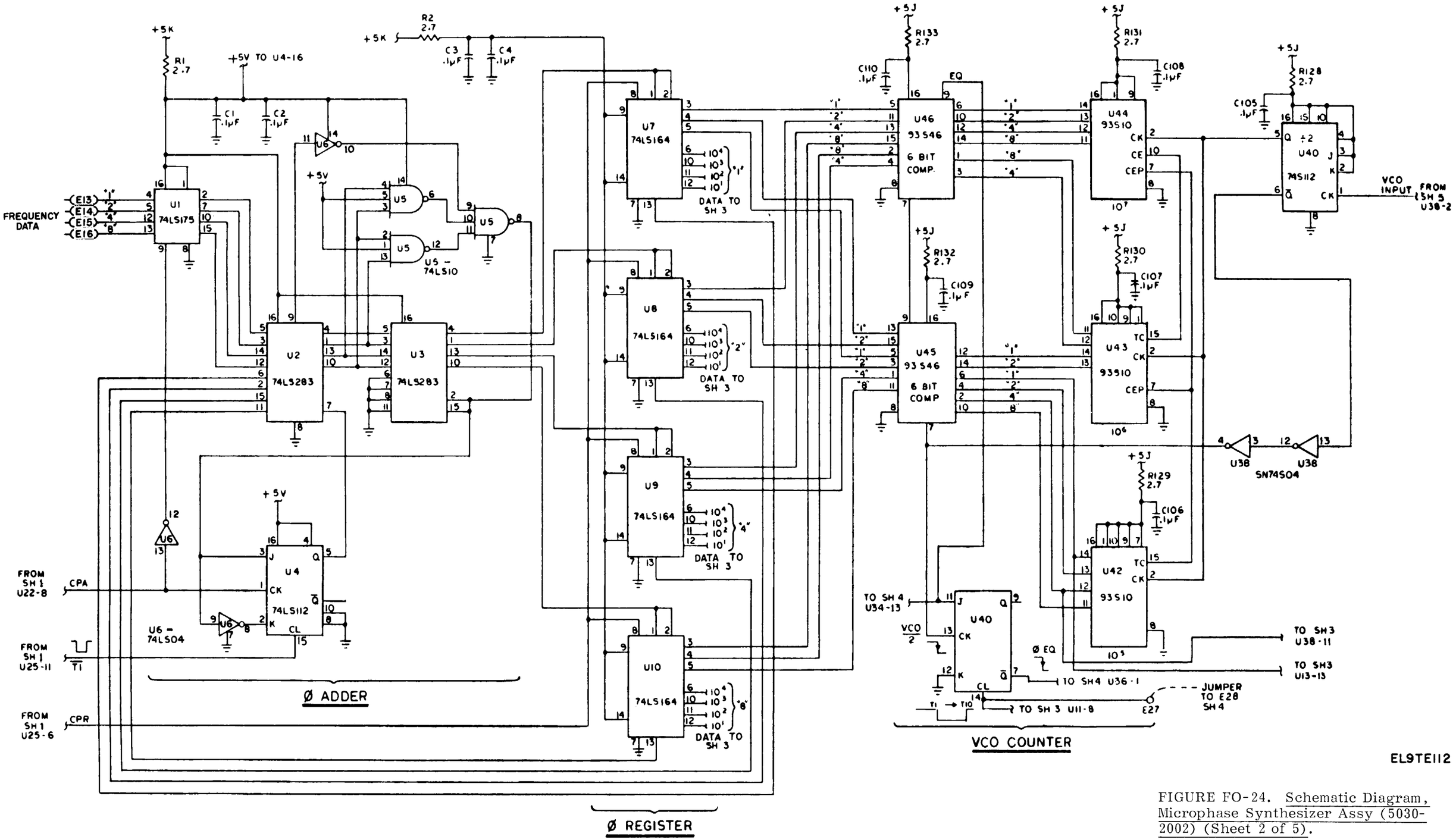


FIGURE FO-24. Schematic Diagram, Microphase Synthesizer Assy (5030-2002) (Sheet 2 of 5).

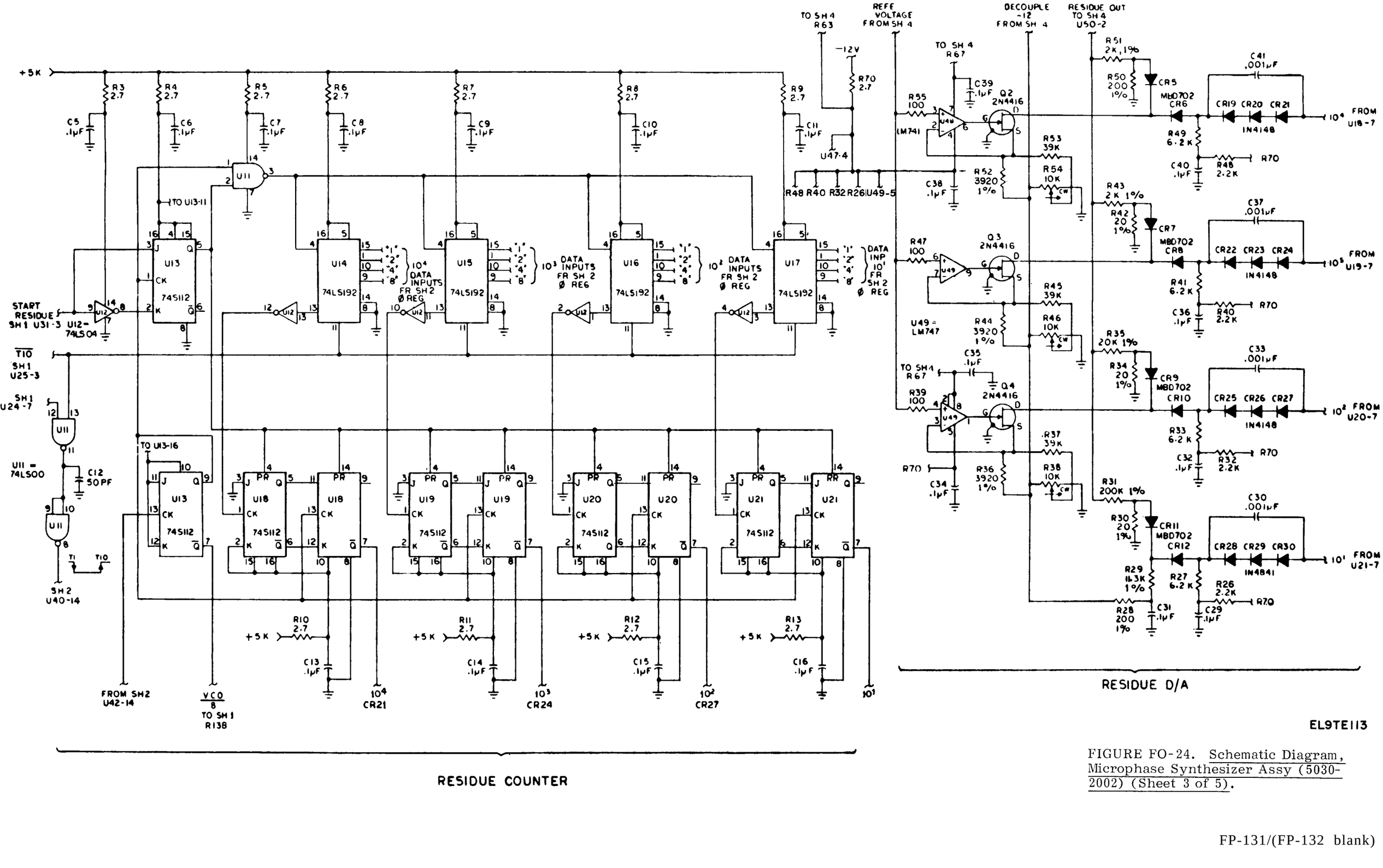


FIGURE FO-24. Schematic Diagram, Microphase Synthesizer Assy (5030-2002) (Sheet 3 of 5).

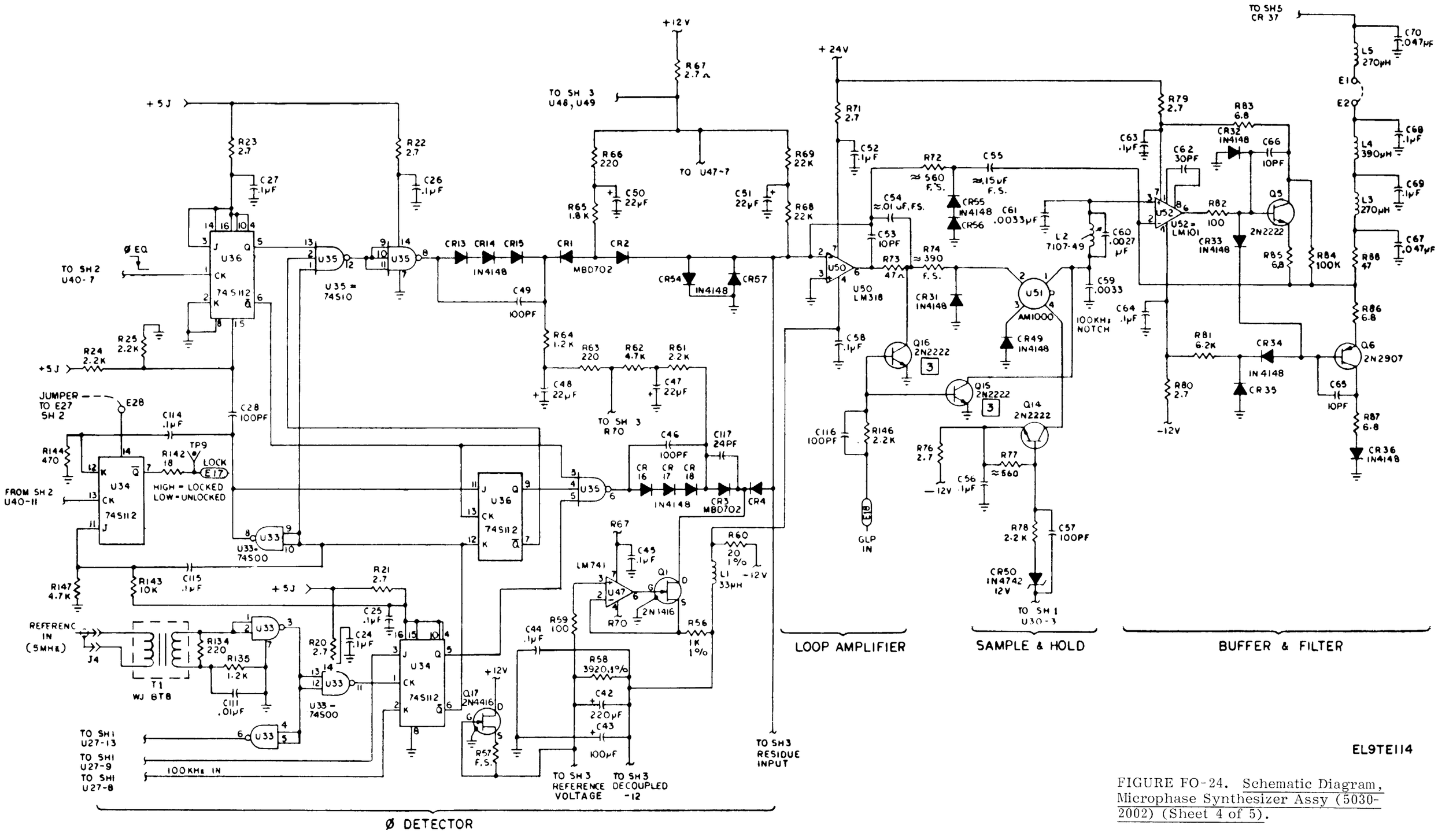


FIGURE FO-24. Schematic Diagram, Microphase Synthesizer Assy (5030-2002) (Sheet 4 of 5).

EL9TE115

FIGURE FO-24. Schematic Diagram, Microphage Synthesizer Assy (5030-2002) (Sheet 5 of 5).

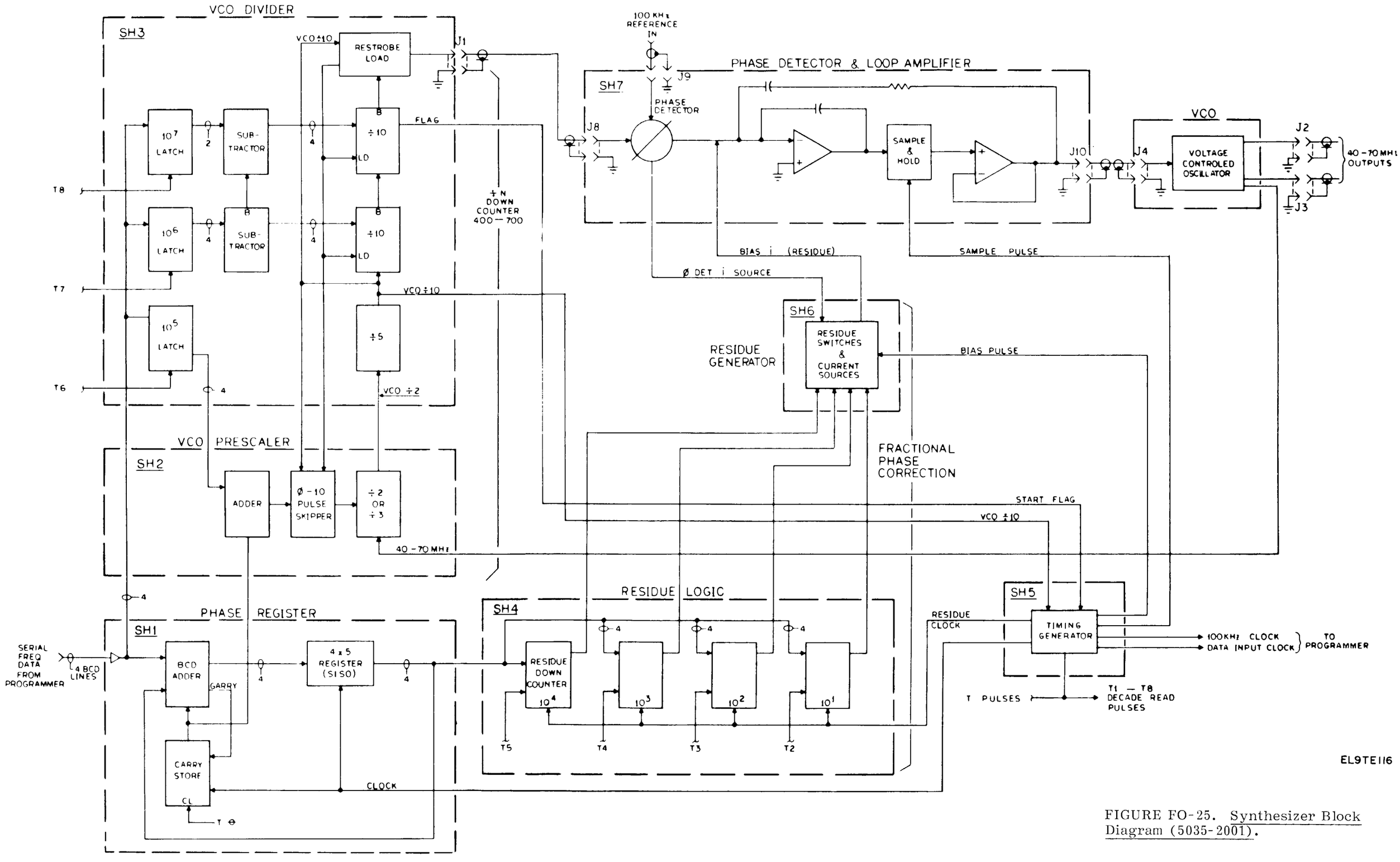
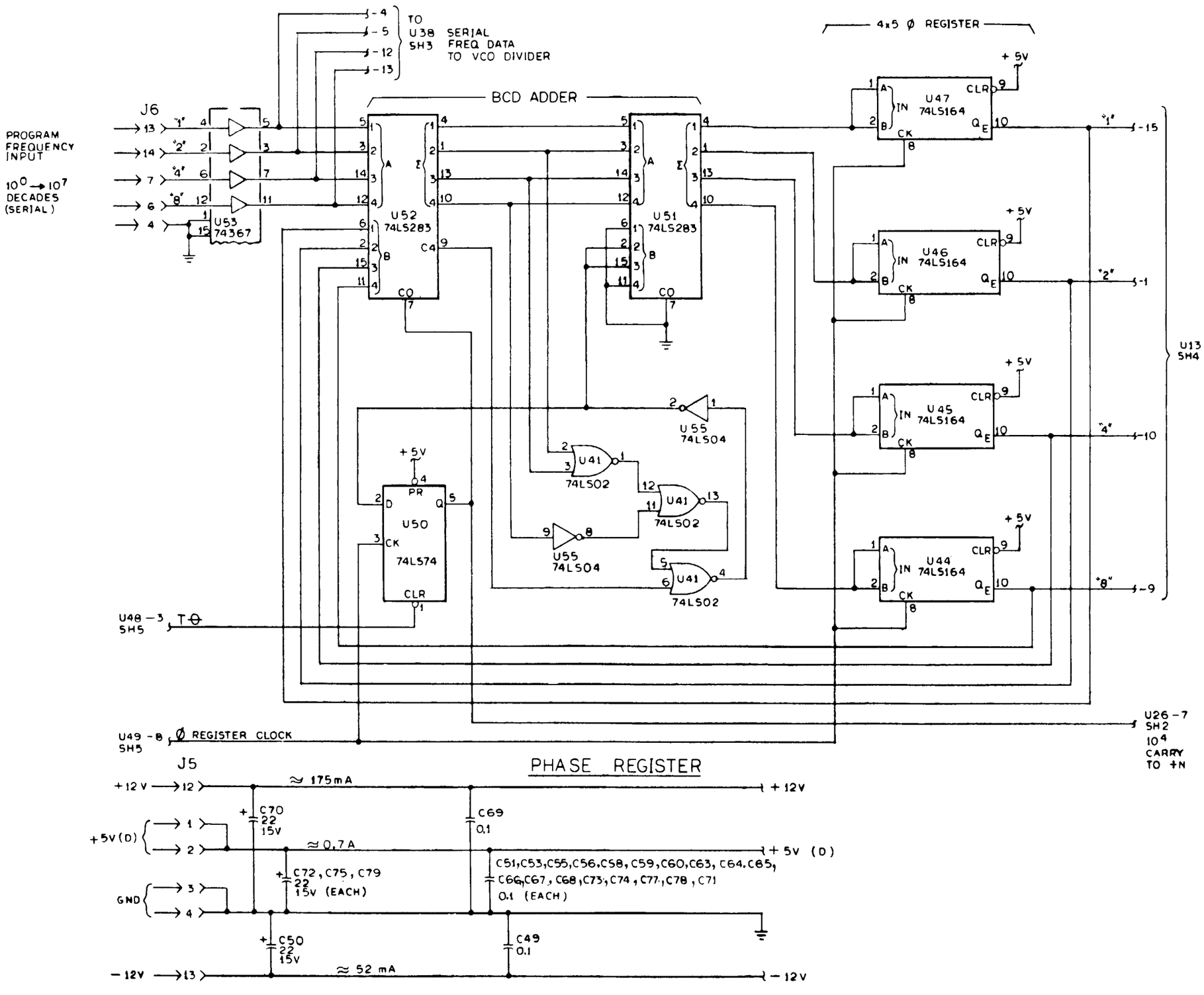


FIGURE FO-25. Synthesizer Block Diagram (5035-2001).



POWER DISTRIBUTION		
DEVICE	+5VD	GND
74(S)(LS)00	14	7
74LS02	14	7
74(S)(LS)04	14	7
74(S)(LS)74	14	7
74(S)(LS)112	16	8
74LS164	14	7
74LS175	16	8
74(S)(LS)192	16	8
74LS283	16	8
74367	16	8

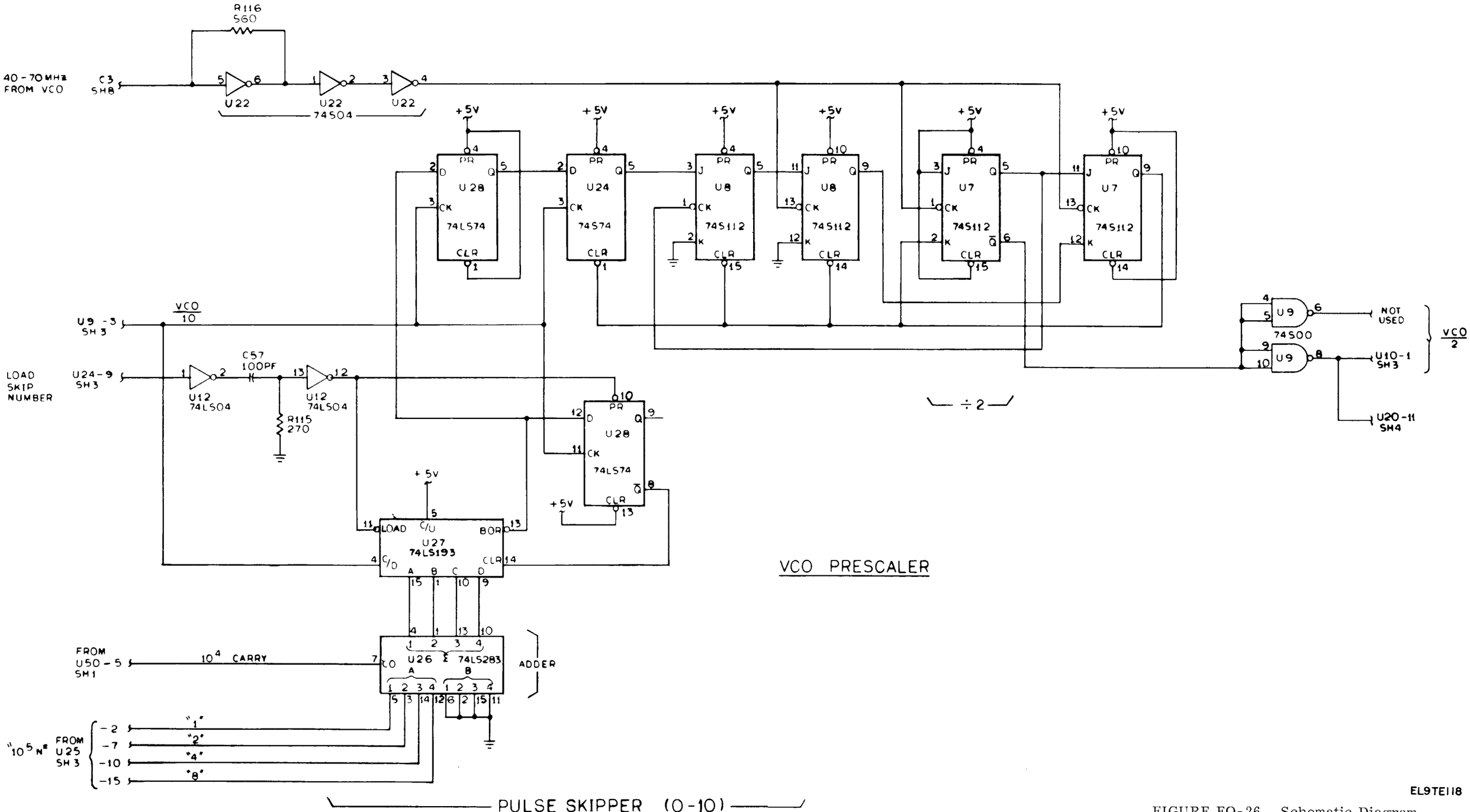
[8] U34 AND U39 ARE BR 5035-4801 PROMS.
[7] RESISTOR, DIP 14PIN BECKMAN 899-1-R4.7K.
6. (XXX) INDICATES D.C. VOLTAGE.
5. +5V IS +5VD.
4. ALL INDUCTORS ARE IN MICROHENRYS.
3. ALL CAPACITORS ARE IN MICROFARADS.
2. ALL RESISTORS ARE IN OHMS 1/4W, 5%.
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSY DESIGNATION

NOTES: UNLESS OTHERWISE SPECIFIED.

HIGHEST REFERENCE DESIGNATION									
C81	D21	J10	L7	Q36	R123	RP1	U56	VR1	TP2
REF DESIGNATIONS NOT USED									
C76					R12				

EL9TE117

FIGURE FO-26. Schematic Diagram, Synthesizer (5035-2001) (Sheet 1 of 8).



EL9TE118

FIGURE FO-26. Schematic Diagram, Synthesizer (5035-2001) (Sheet 2 of 8).

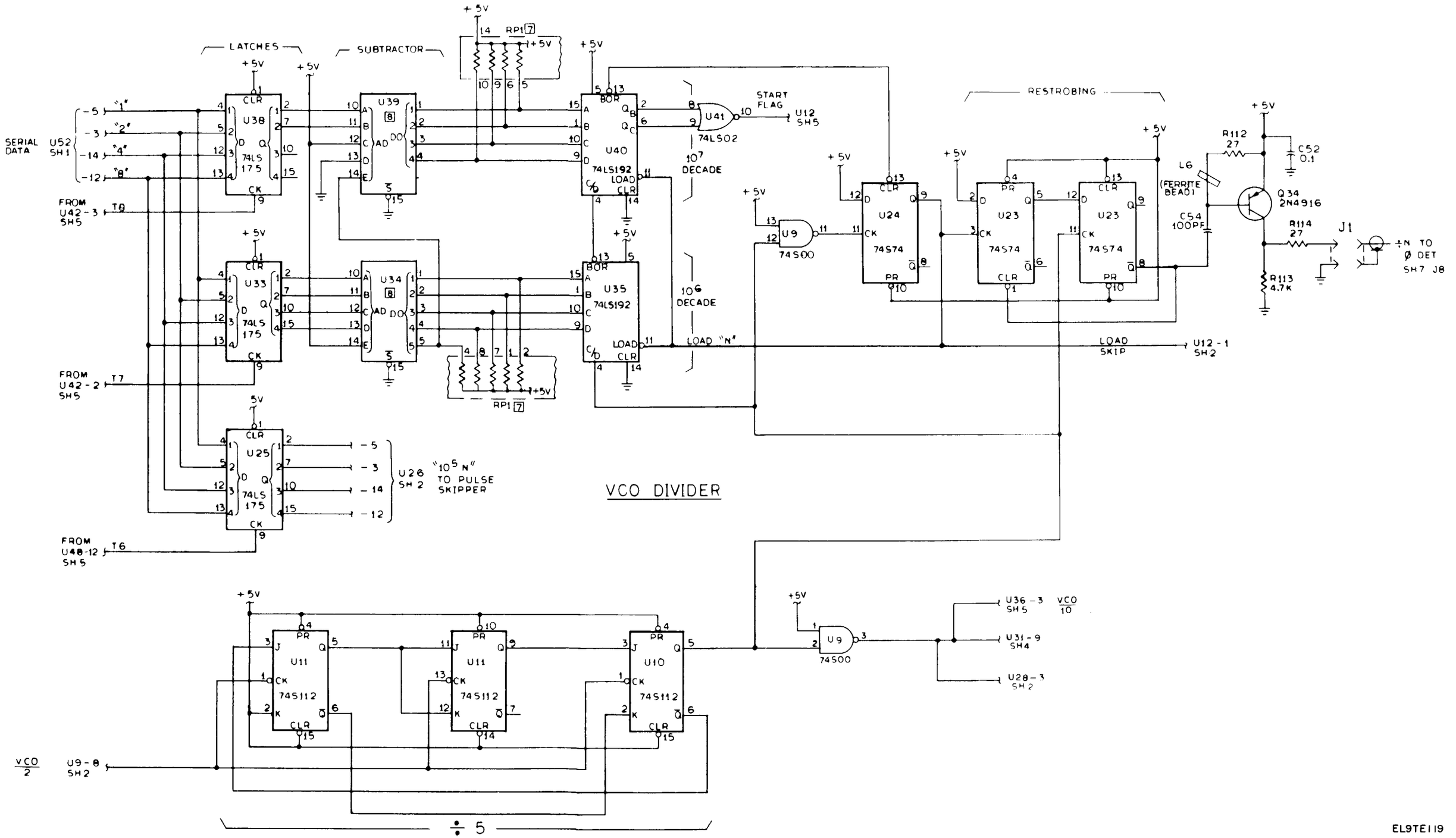
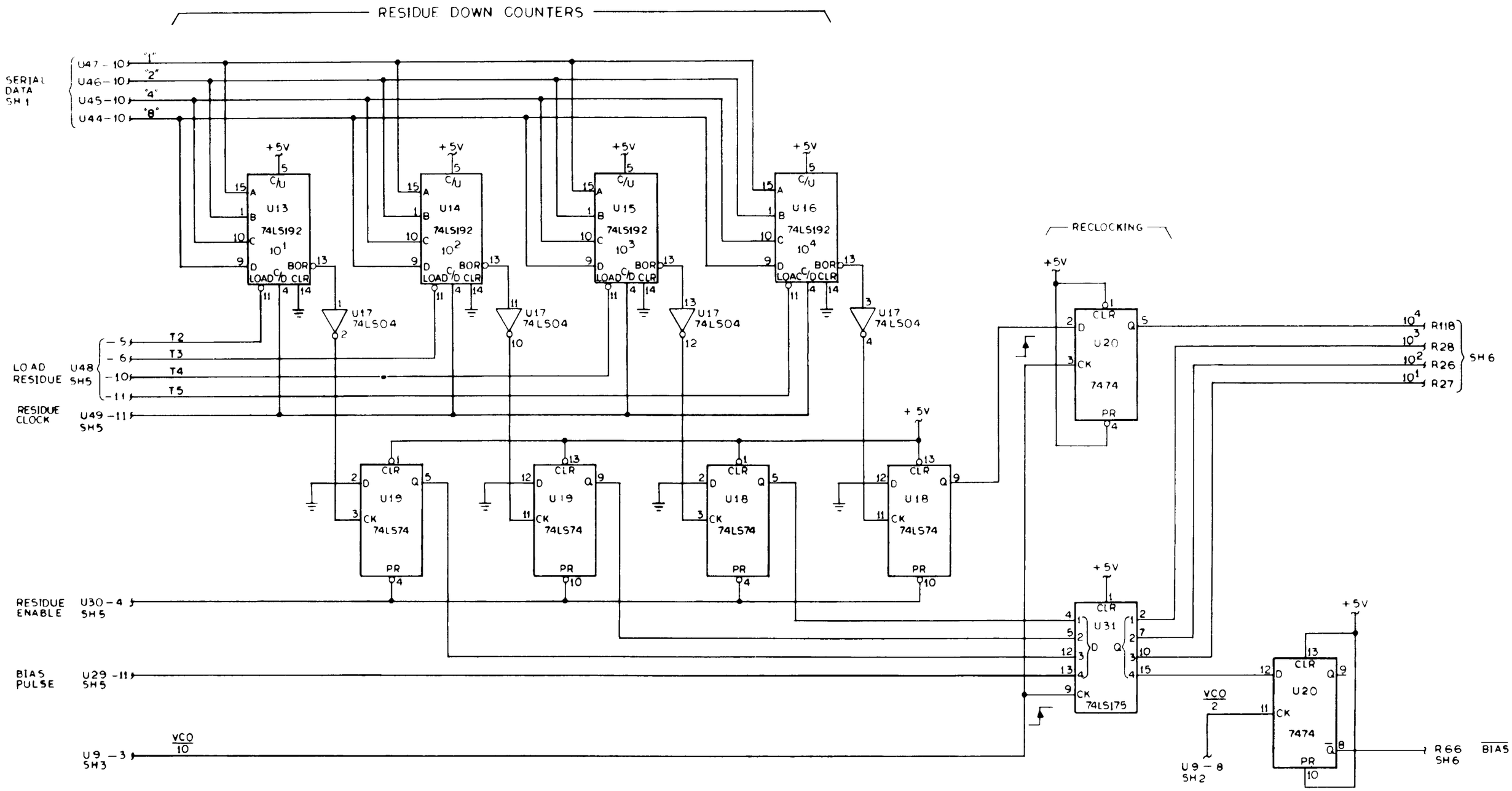


FIGURE FO-26. Schematic Diagram, Synthesizer (5035-2001) (Sheet 3 of 8).



RESIDUE LOGIC

EL9TE120

FIGURE FO-26. Schematic Diagram, Synthesizer (5035-2001) (Sheet 4 of 8).

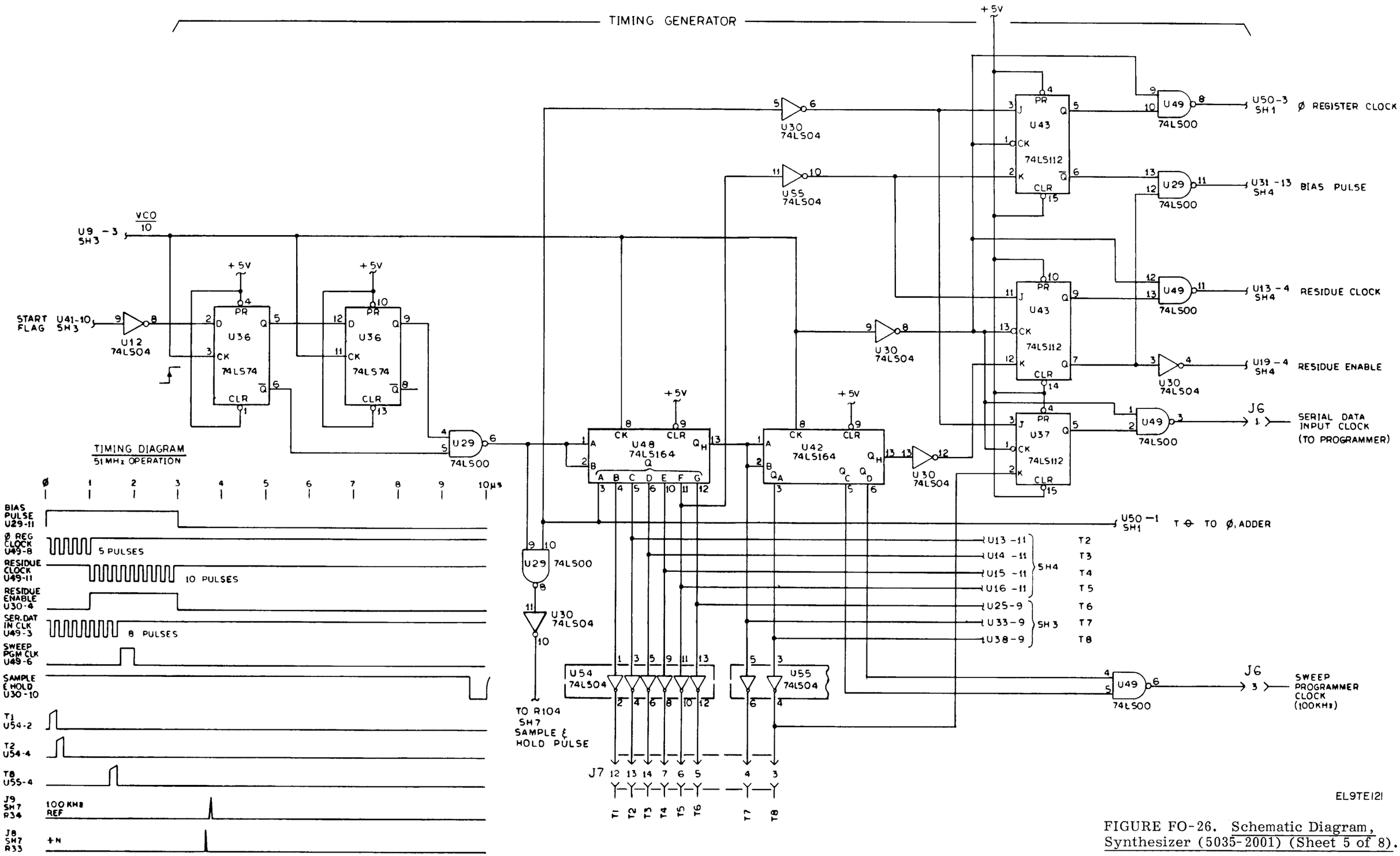
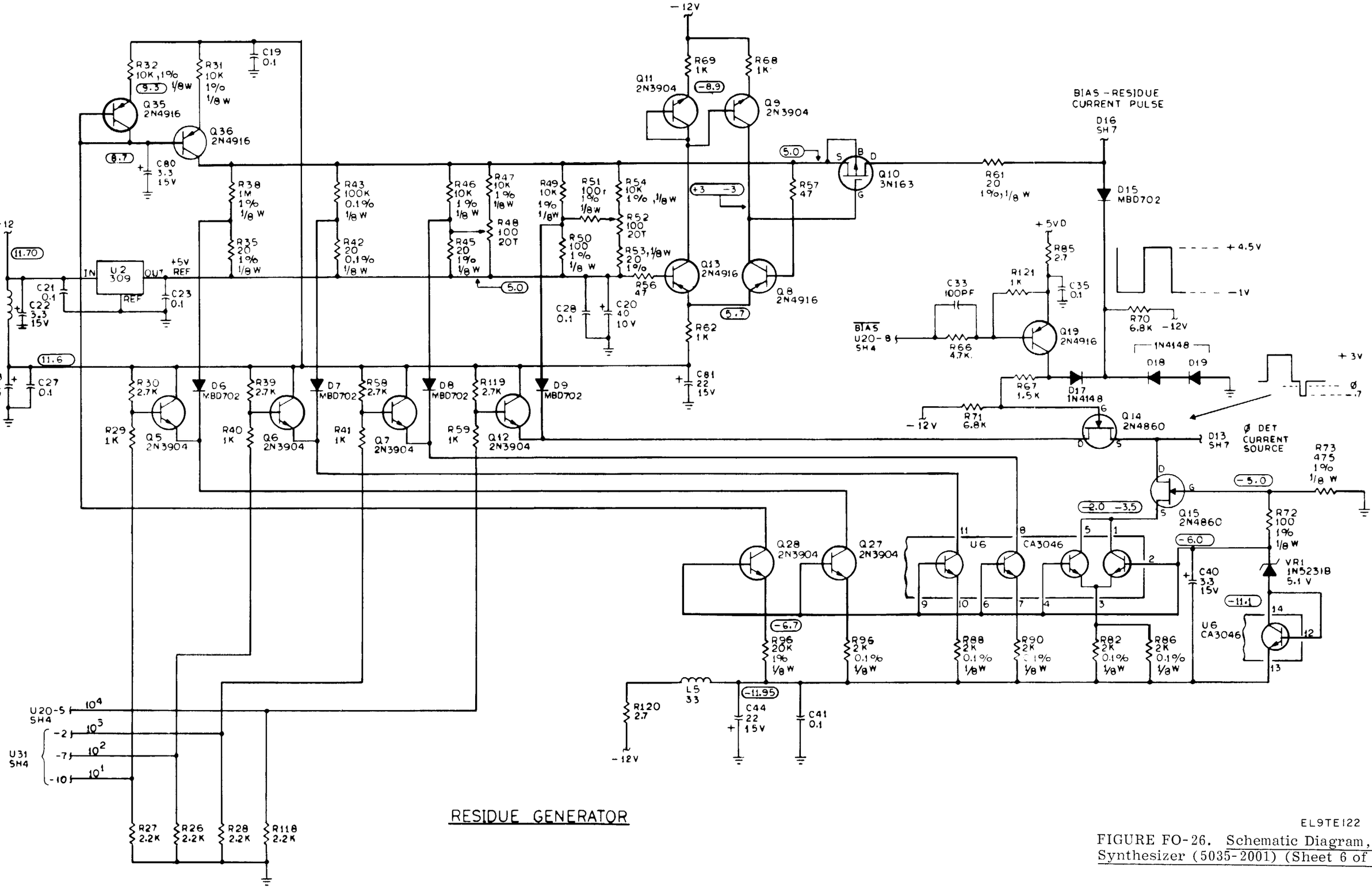


FIGURE FO-26. Schematic Diagram, Synthesizer (5035-2001) (Sheet 5 of 8).



RESIDUE GENERATOR

EL9TE122

FIGURE FO-26. Schematic Diagram, Synthesizer (5035-2001) (Sheet 6 of 8).

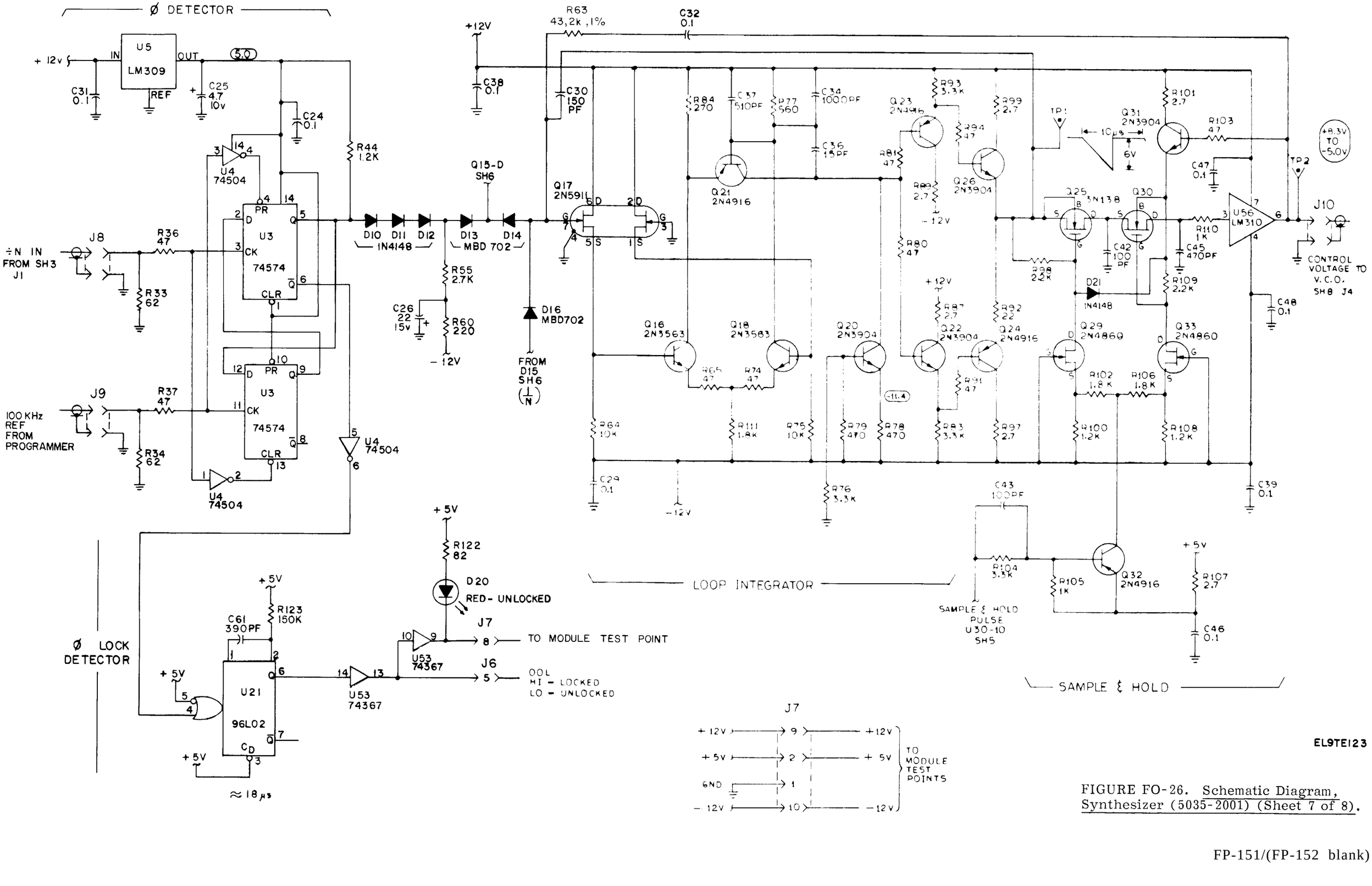


FIGURE FO-26. Schematic Diagram, Synthesizer (5035-2001) (Sheet 7 of 8).

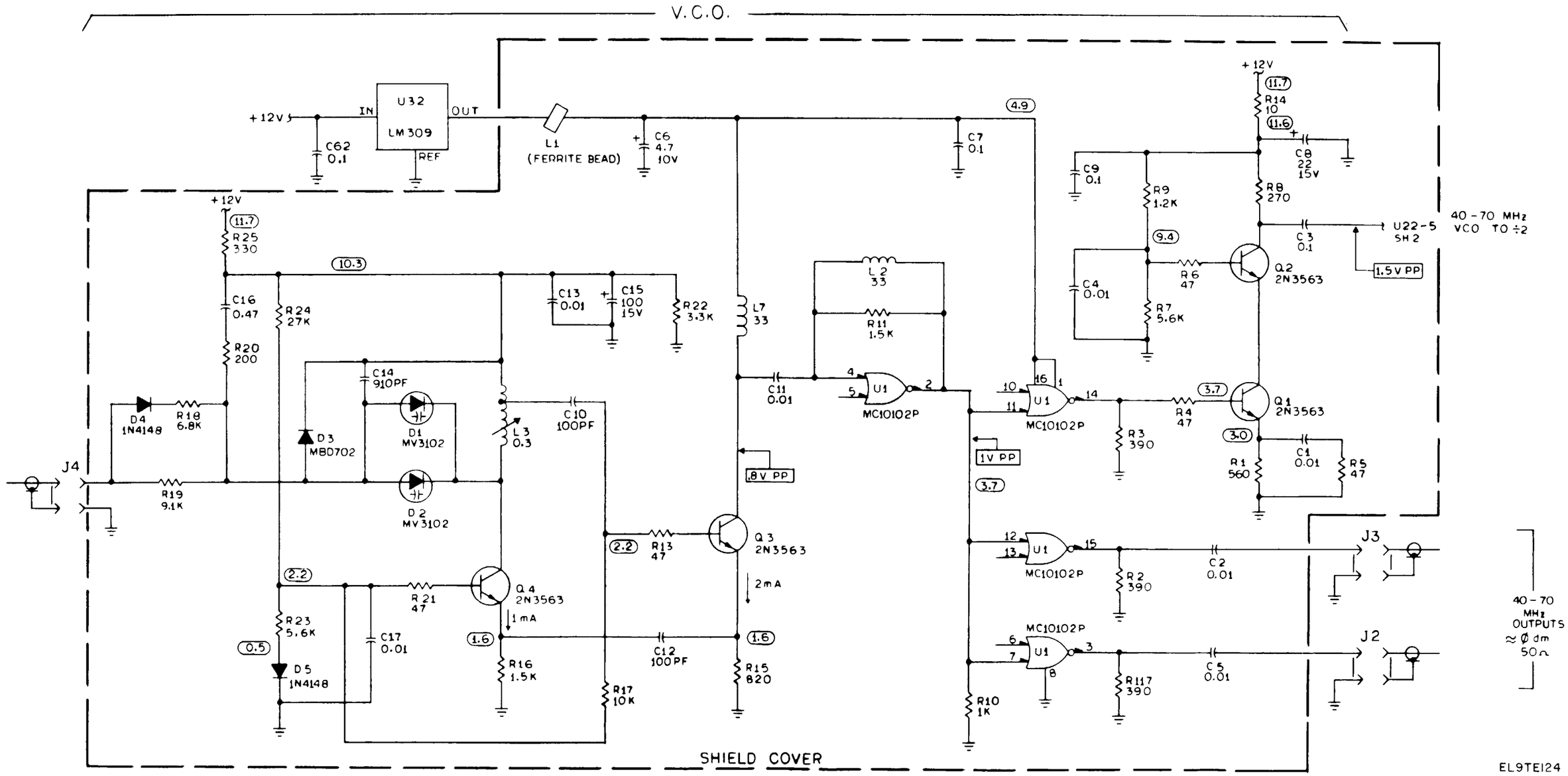


FIGURE FO-26. Schematic Diagram, Synthesizer (5035-2001) (Sheet 8 of 8).

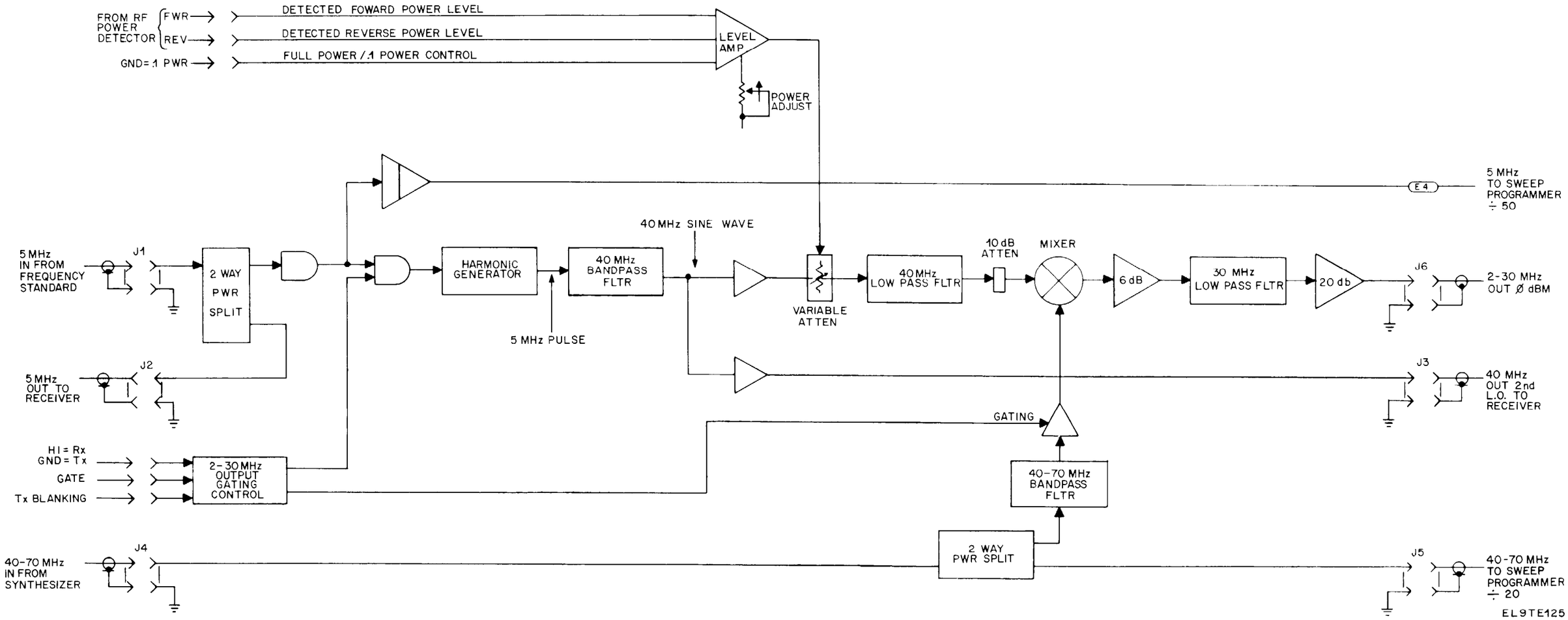
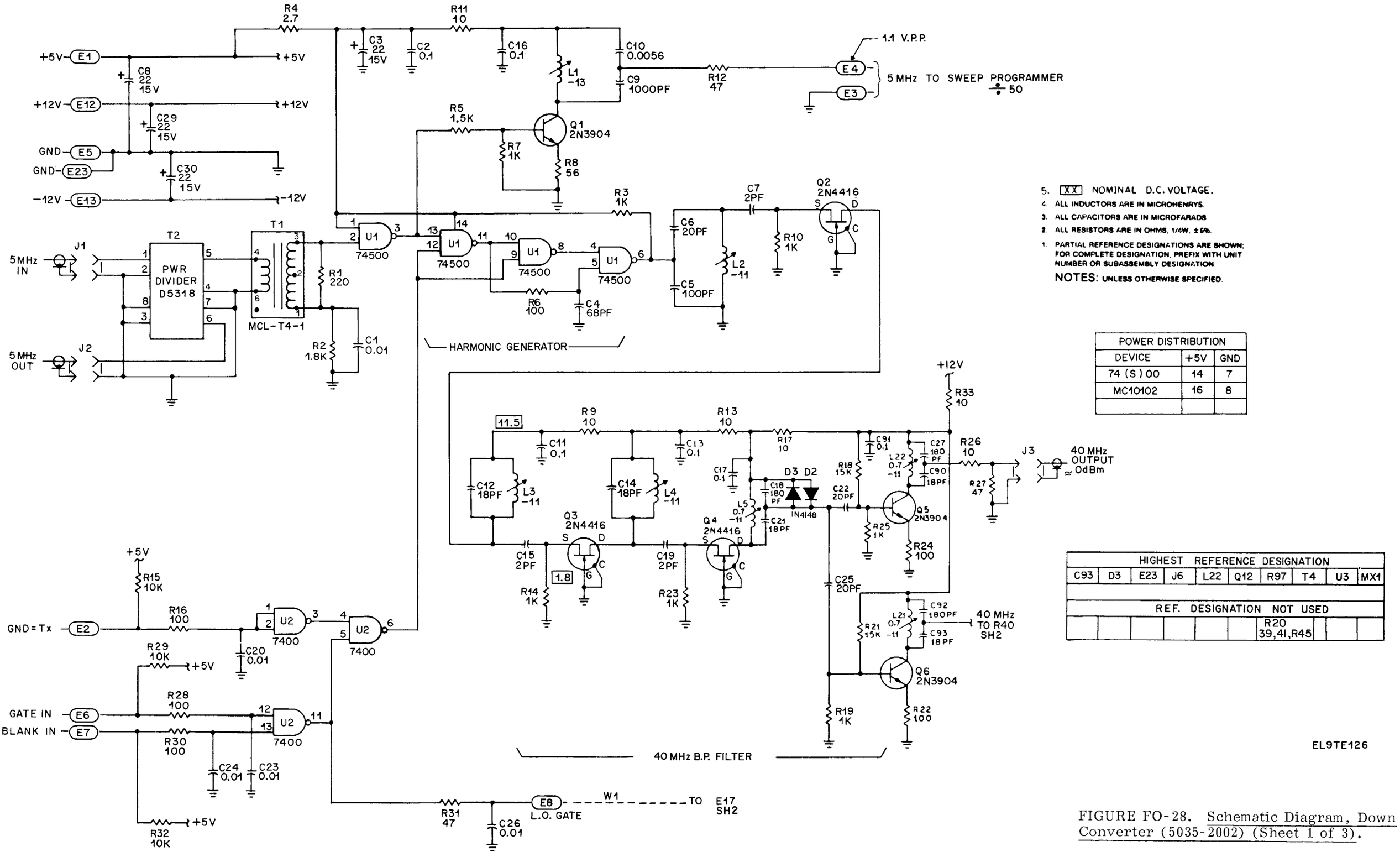


FIGURE FO-27. Down Converter Block Diagram (5035-2002).



5. [XX] NOMINAL D.C. VOLTAGE.
4. ALL INDUCTORS ARE IN MICROHENRYS.
3. ALL CAPACITORS ARE IN MICROFARADS
2. ALL RESISTORS ARE IN OHMS, 1/4W, ±5%.
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION.

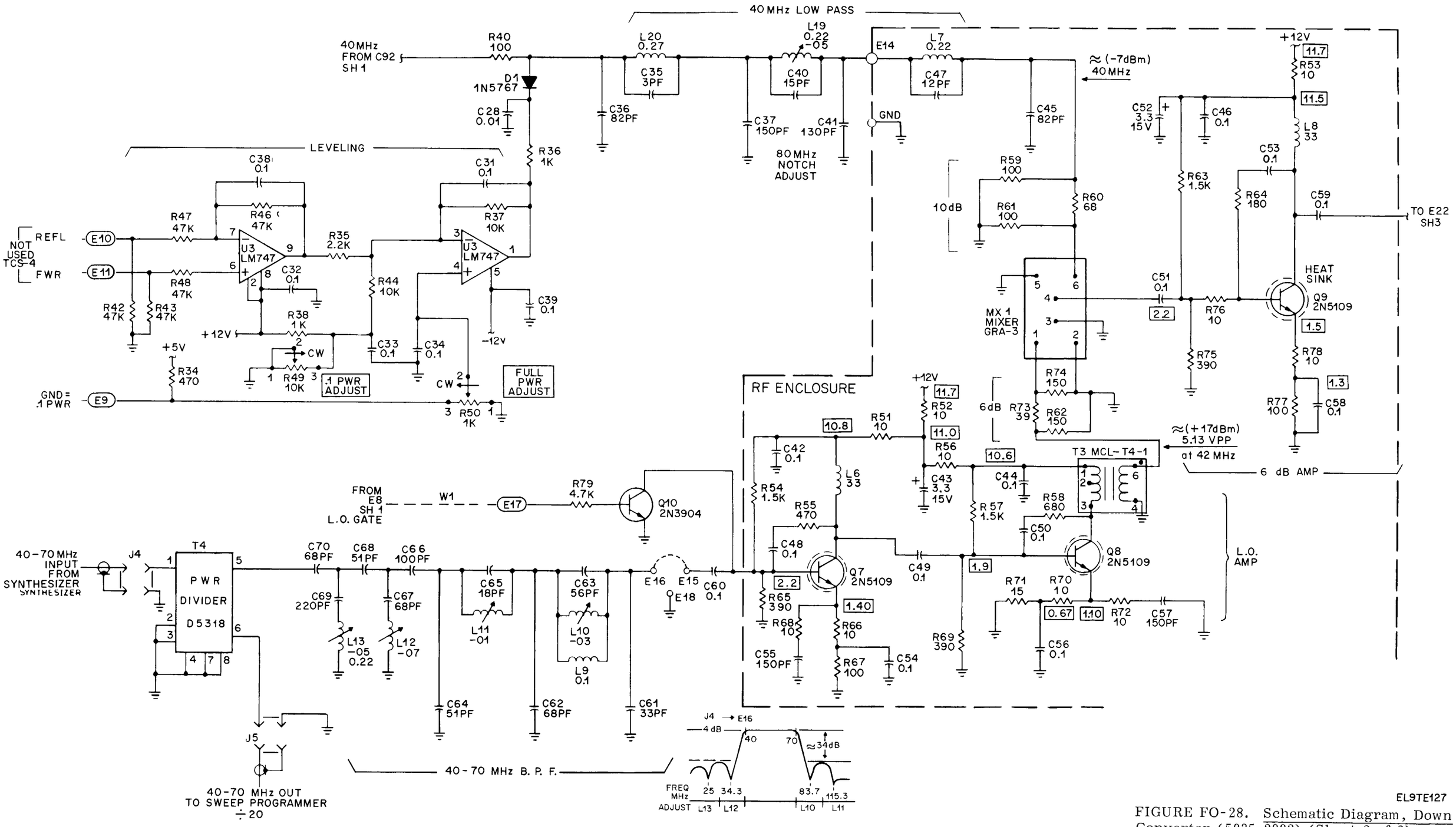
NOTES: UNLESS OTHERWISE SPECIFIED.

POWER DISTRIBUTION		
DEVICE	+5V	GND
74 (S) 00	14	7
MC10102	16	8

HIGHEST REFERENCE DESIGNATION									
C93	D3	E23	J6	L22	Q12	R97	T4	U3	MX1
REF. DESIGNATION NOT USED									
						R20 39,41,R45			

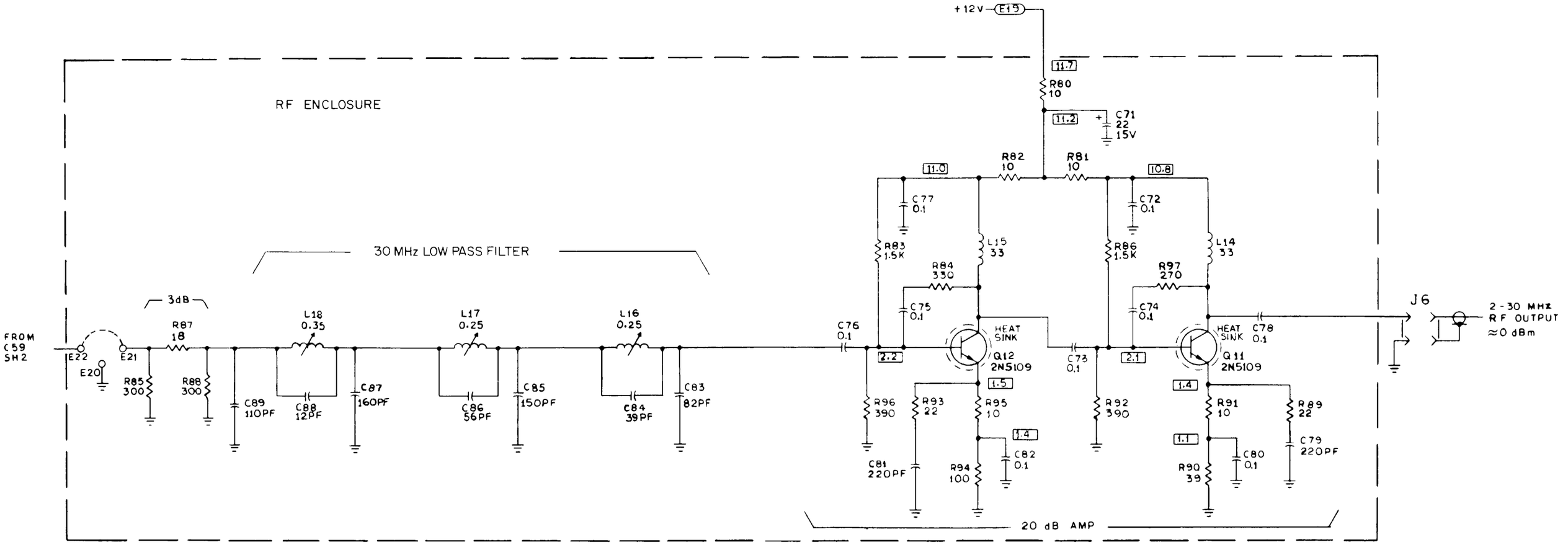
EL9TE126

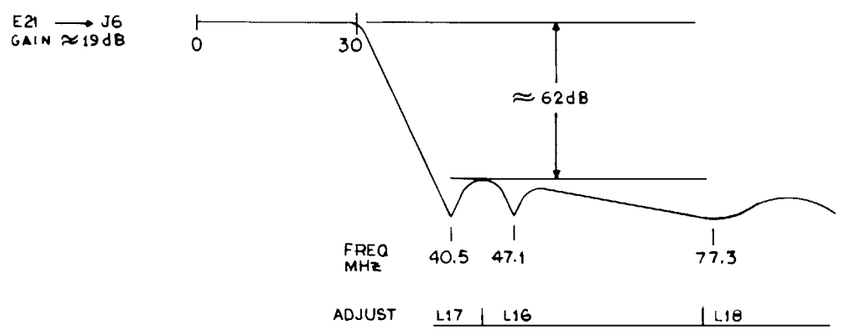
FIGURE FO-28. Schematic Diagram, Down Converter (5035-2002) (Sheet 1 of 3).



EL9TE127

FIGURE FO-28. Schematic Diagram, Down Converter (5035-2002) (Sheet 2 of 3).





EL9TE128

FIGURE FO-28. Schematic Diagram, Down Converter (5035-2002) [Sheet 3 of 3).

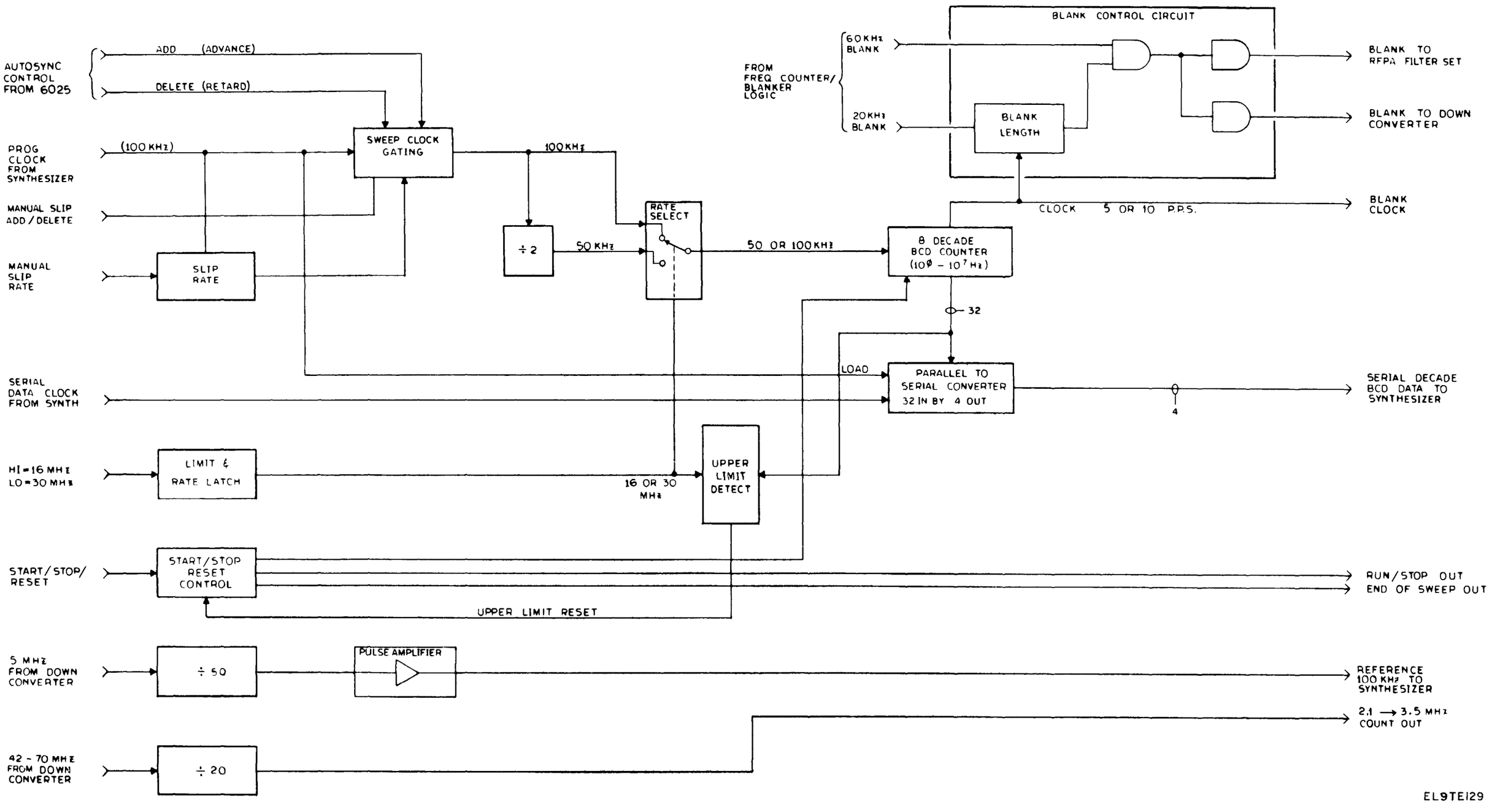
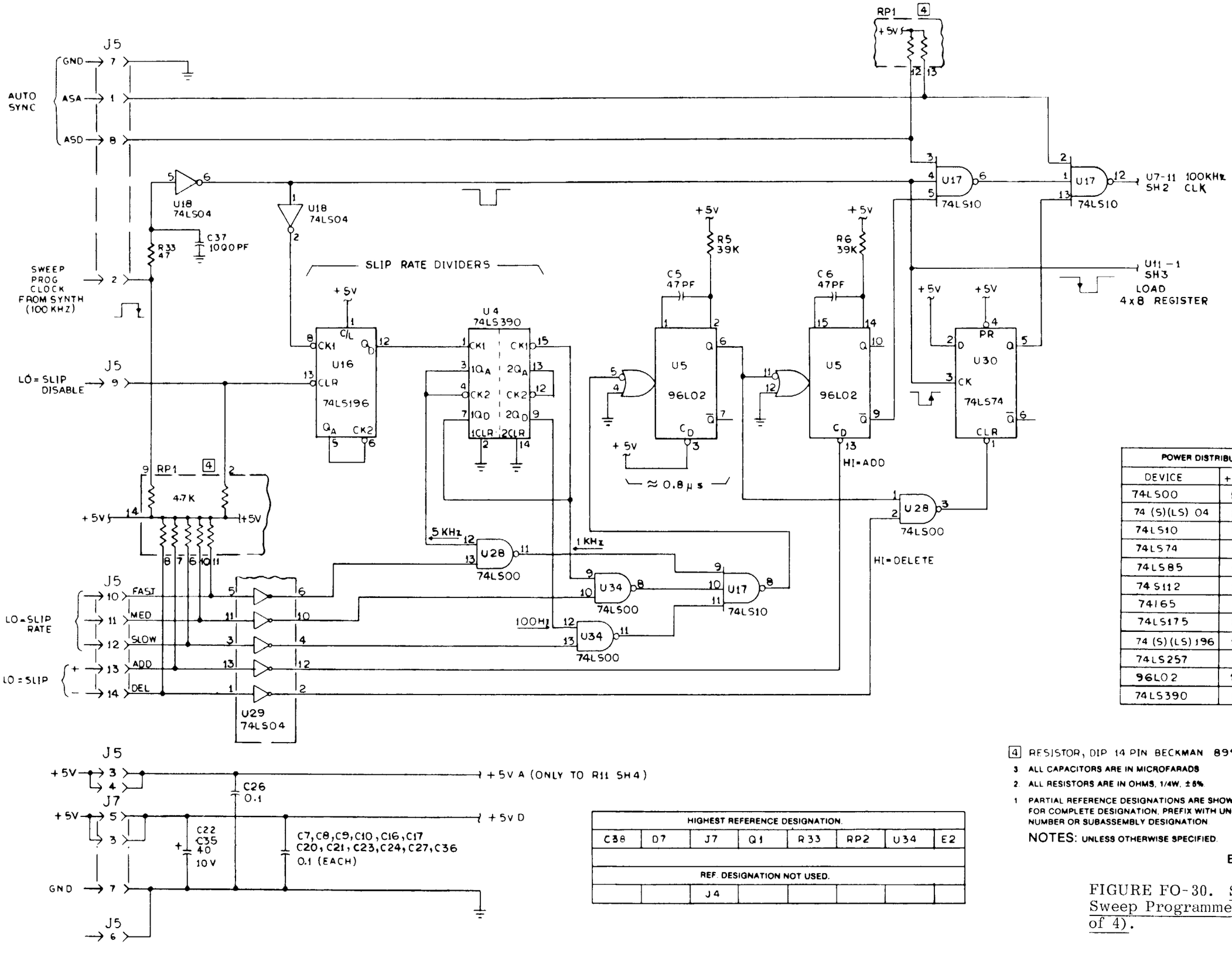


FIGURE FO-29. Sweep Programmer Block Diagram (5035-2003).



POWER DISTRIBUTION.		
DEVICE	+5VD	GND
74LS00	14	7
74 (S)(LS) 04	14	7
74LS10	14	7
74LS74	14	7
74LS85	16	8
74S112	16	8
74165	16	8
74LS175	16	8
74 (S)(LS)196	14	7
74LS257	16	8
96L02	16	8
74LS390	16	8

HIGHEST REFERENCE DESIGNATION.							
C38	D7	J7	Q1	R33	RP2	U34	E2
REF. DESIGNATION NOT USED.							
		J4					

4 RESISTOR, DIP 14 PIN BECKMAN 899-1-R 4.7K.

3. ALL CAPACITORS ARE IN MICROFARADS
2. ALL RESISTORS ARE IN OHMS, 1/4W, ±5%
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION

NOTES: UNLESS OTHERWISE SPECIFIED.

EL9TE130

FIGURE FO-30. Schematic Diagram, Sweep Programmer (5035-2003) (Sheet 1 of 4).

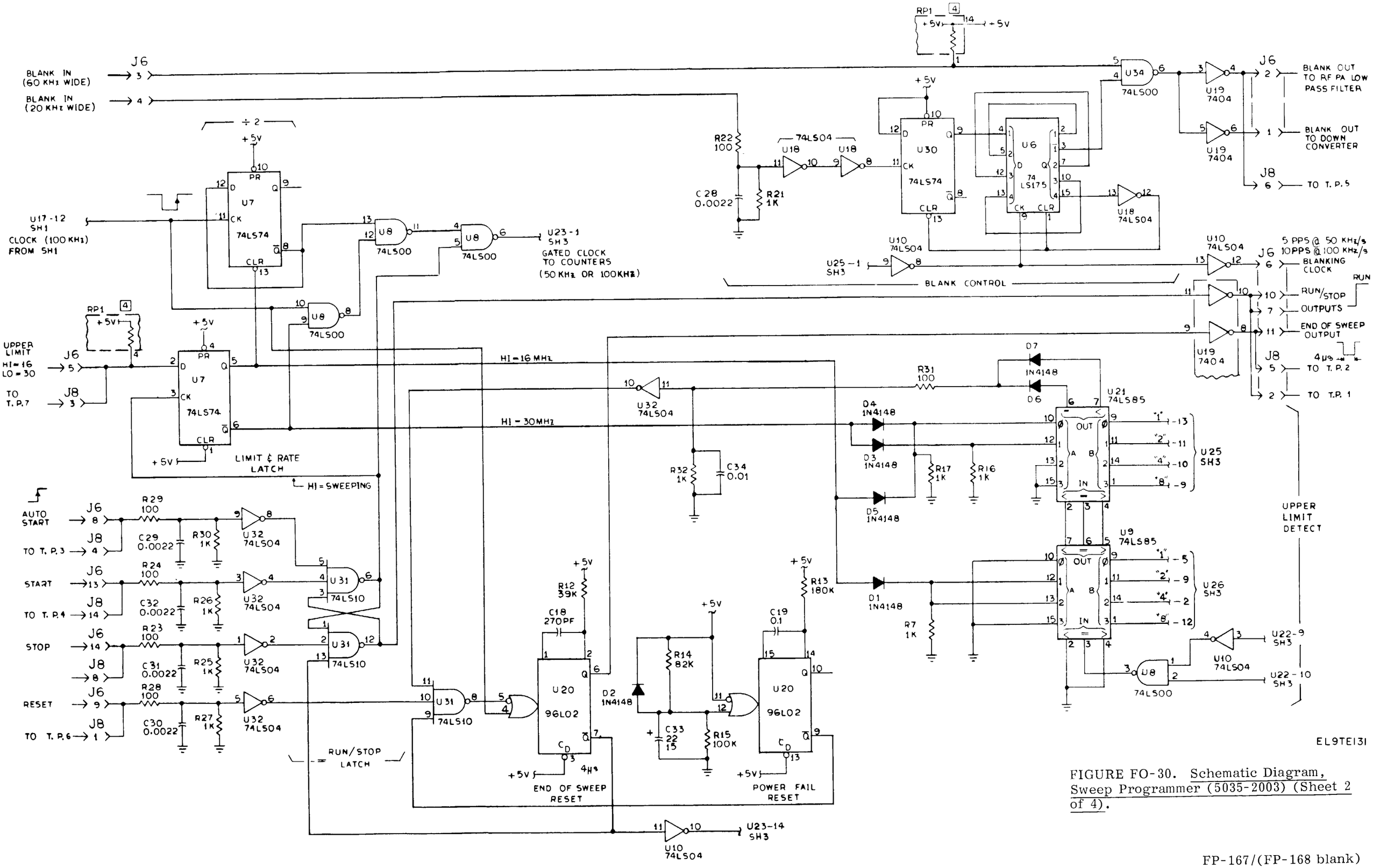
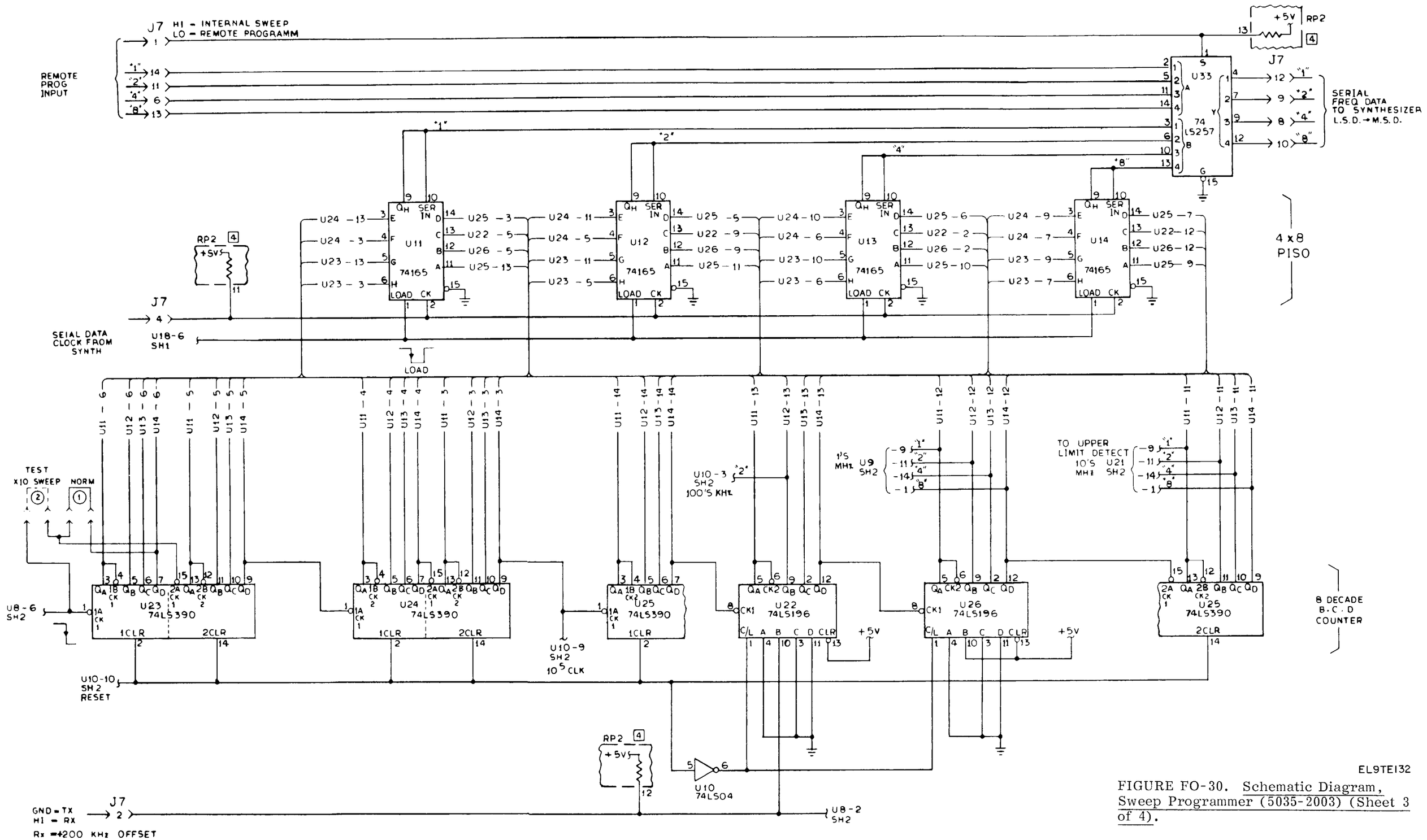


FIGURE FO-30. Schematic Diagram, Sweep Programmer (5035-2003) (Sheet 2 of 4).



EL9TEI32

FIGURE FO-30. Schematic Diagram, Sweep Programmer (5035-2003) (Sheet 3 of 4).

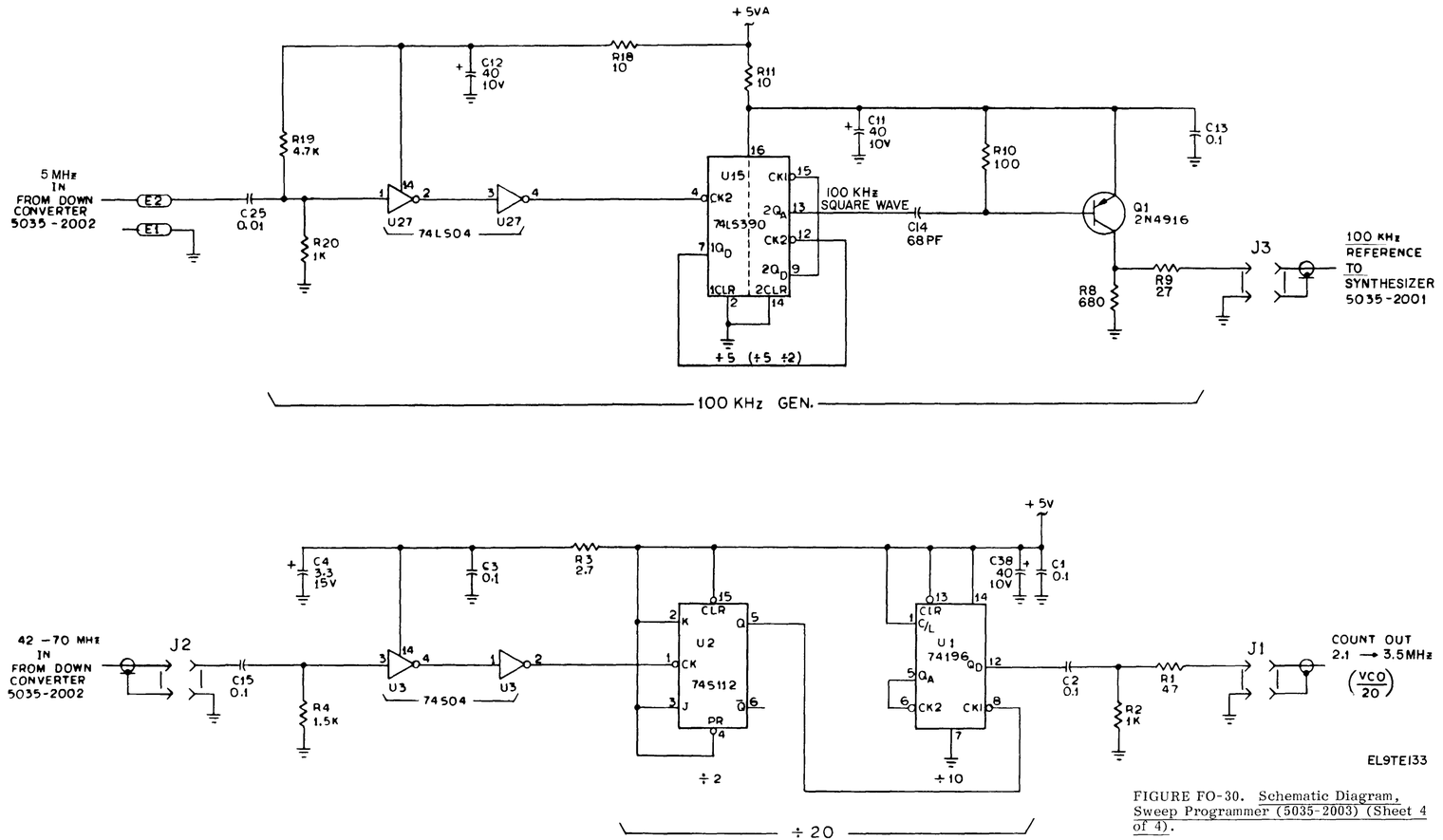
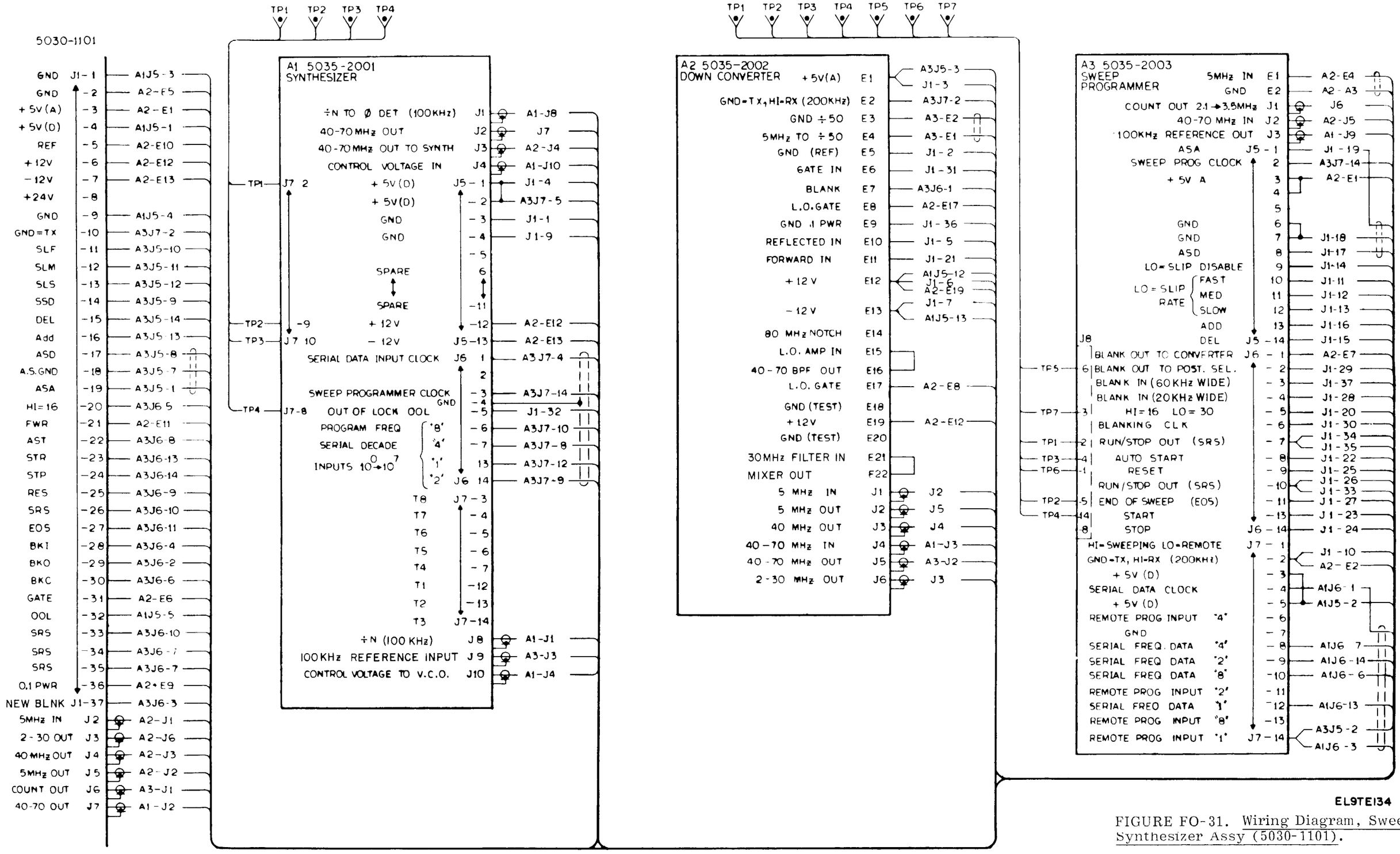


FIGURE FO-30. Schematic Diagram, Sweep Programmer (5035-2003) (Sheet 4 of 4).



EL9TE134

FIGURE FO-31. Wiring Diagram, Sweep Synthesizer Assy (5030-1101).

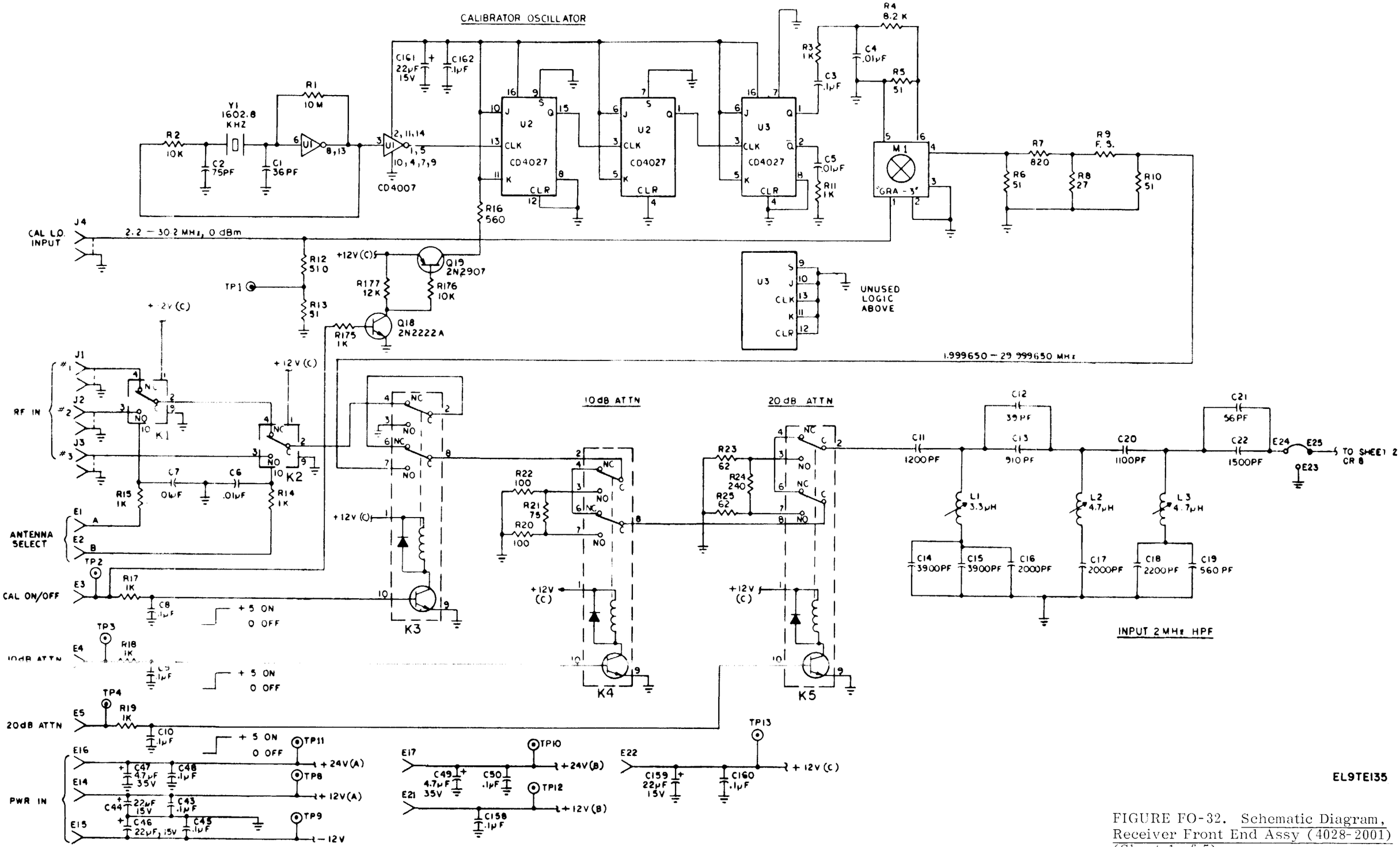
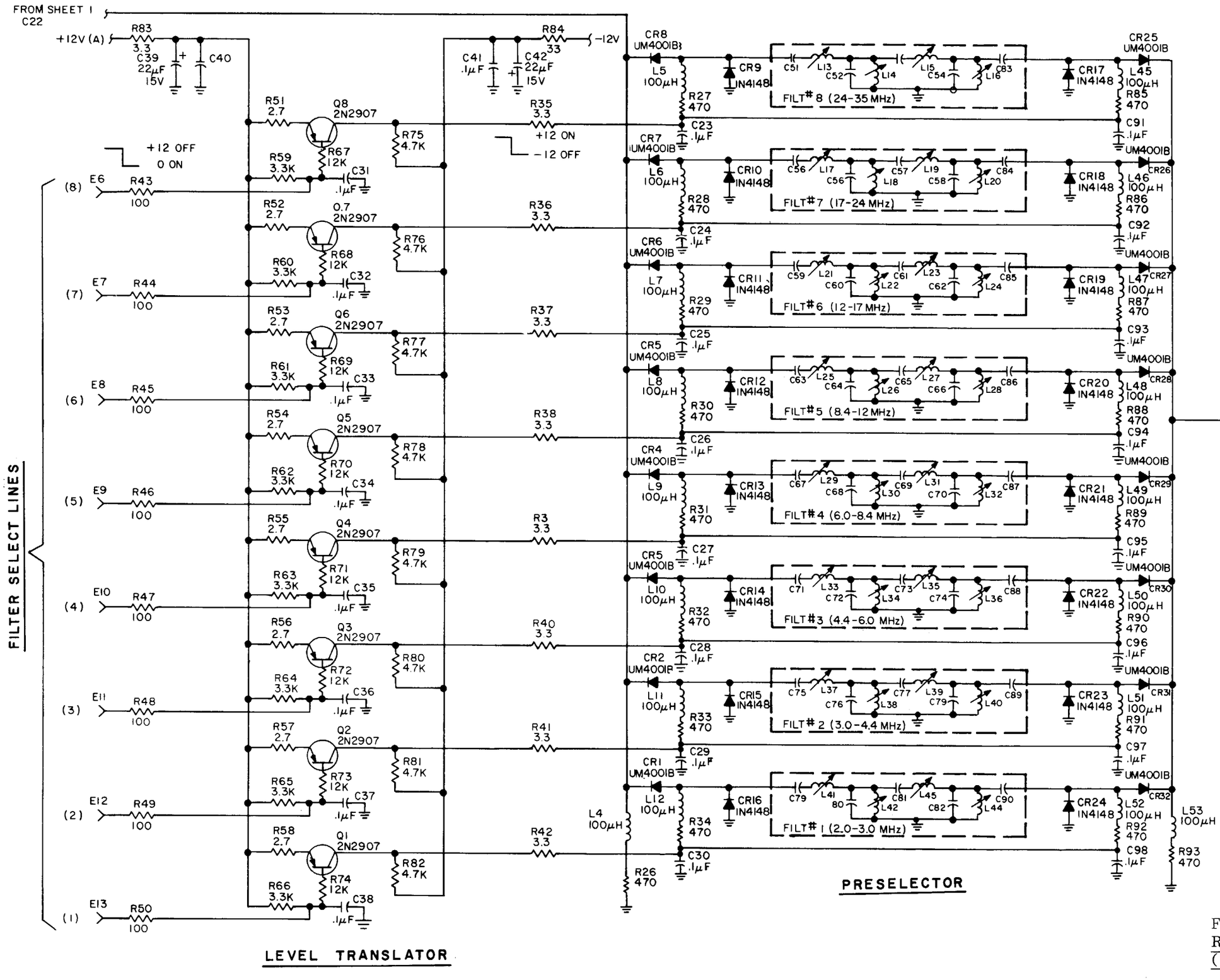


FIGURE FO-32. Schematic Diagram, Receiver Front End Assy (4028-2001) (Sheet 1 of 5).



FILTER	C	PF	L	µH
#8	51	68	13	.47
	52	300	14	.1
	53	39	15	.68
	54	200	16	.15
	83	.1µF		
#7	55	62	17	1
	56	560	18	.1
	57	47	19	1.5
	58	390	20	.15
	84	.1µF		
#6	59	82	21	1.5
	60	820	22	.15
	61	62	23	2.2
	62	510	24	.22
	85	.1µF		
#5	63	150	25	2.2
	64	1200	26	.22
	65	68	27	3.3
	66	680	28	.33
	86	.1µF		
#4	67	180	29	3.3
	68	1500	30	.33
	69	130	31	4.7
	70	1000	32	.47
	87	.1µF		
#3	71	220	33	4.7
	72	2700	34	.53
	73	160	35	6.8
	74	1500	36	.68
	88	1µF, 50V		
#2	75	300	37	6.8
	76	3000	38	.68
	77	220	39	10
	78	2000	40	1.0
	89	1µF 50V		
#1	79	510	41	8.2
	80	3900	42	1
	81	330	43	15
	82	2000	44	2.2
	90	1µF 50V		

FIGURE FO-32. Schematic Diagram, Receiver Front End Assy (4028-2001) (Sheet 2 of 5).

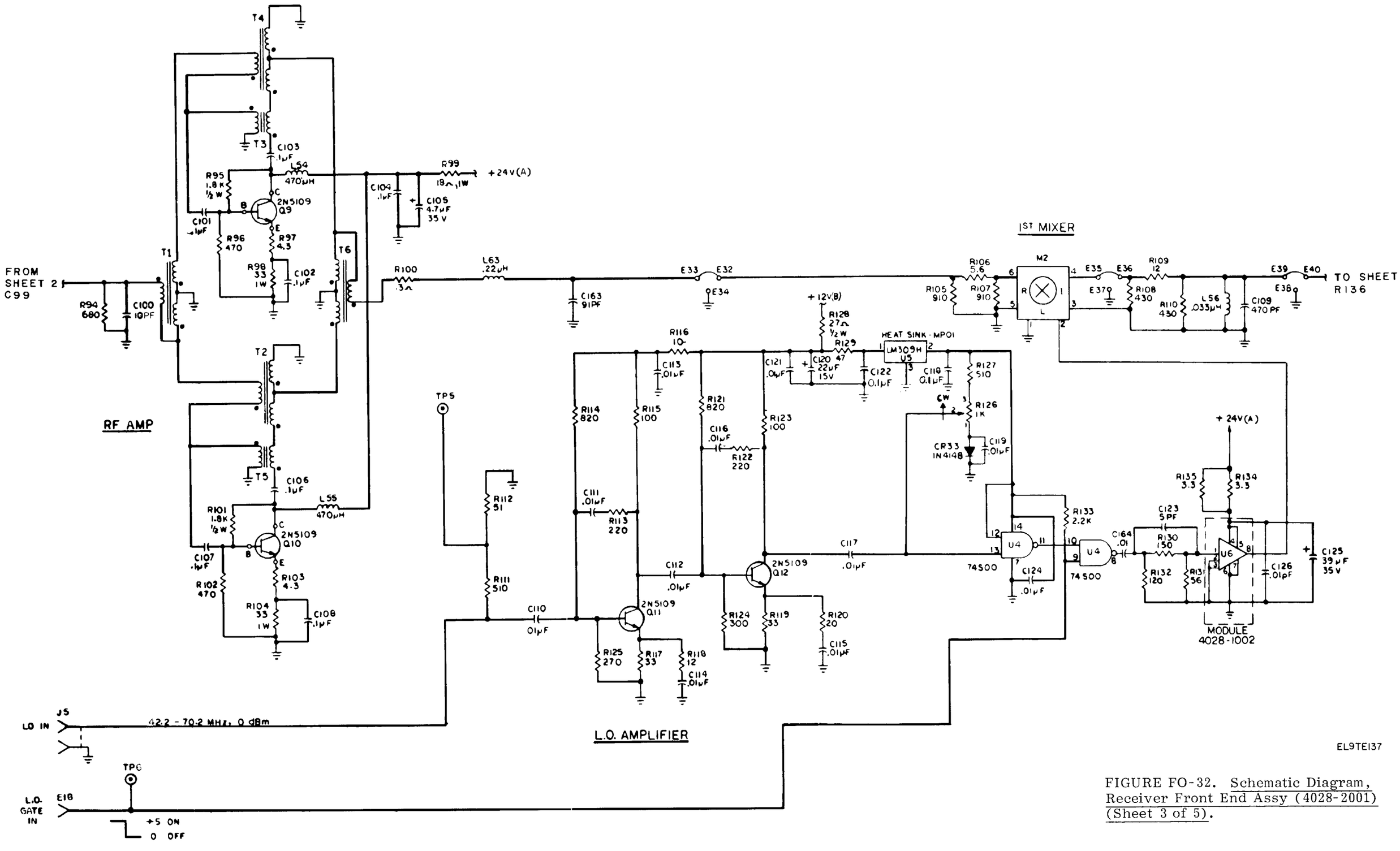


FIGURE FO-32. Schematic Diagram, Receiver Front End Assy (4028-2001) (Sheet 3 of 5).

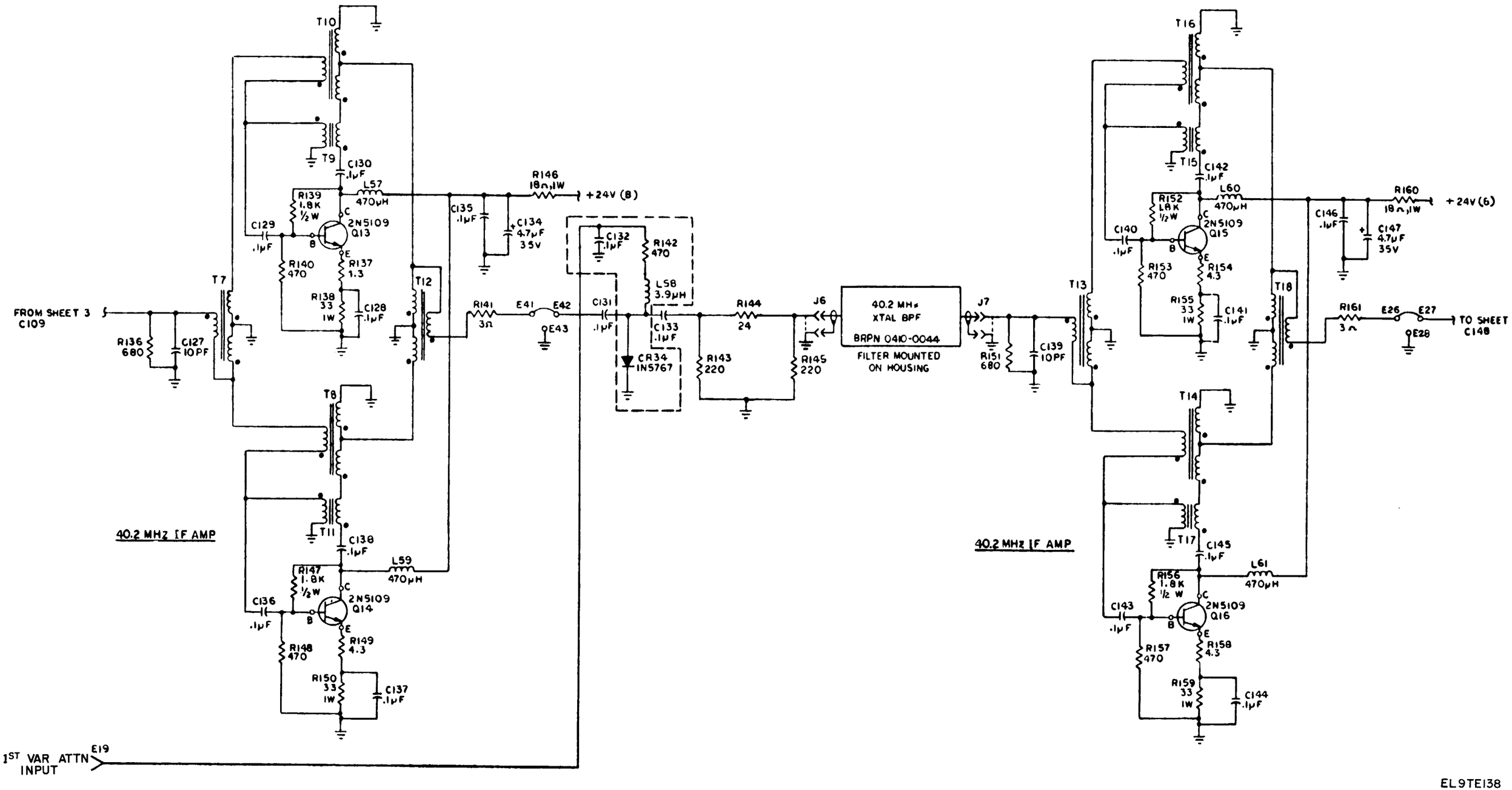
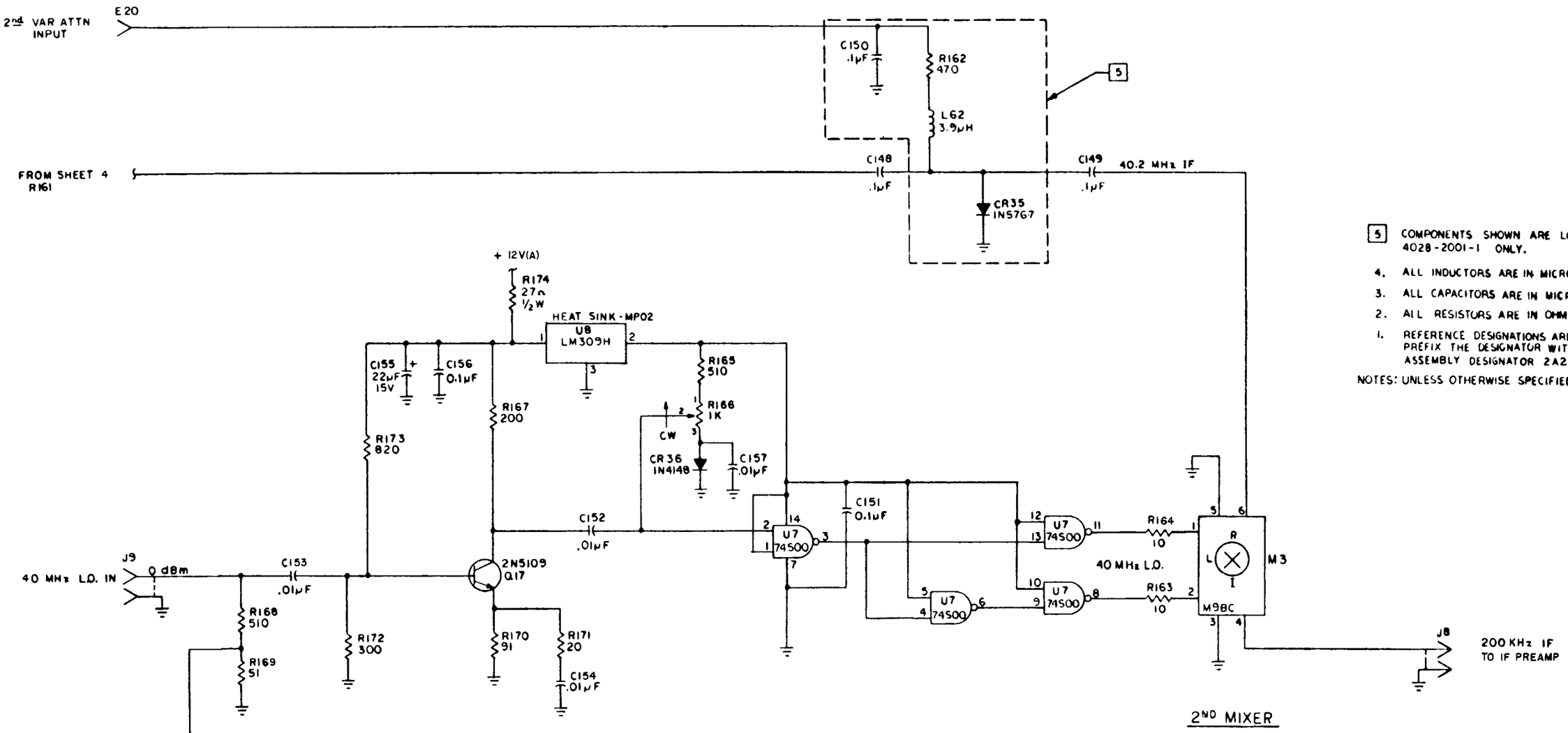


FIGURE FO-32. Schematic Diagram, Receiver Front End Assy (4028-2001) (Sheet 4 of 5).



HIGHEST REFERENCE DESIGNATION											
C164	CR36	E43	J9	K5	L63	M3	Q19	R177	T18	TP13	U8
REF DESIGNATION NOT USED											

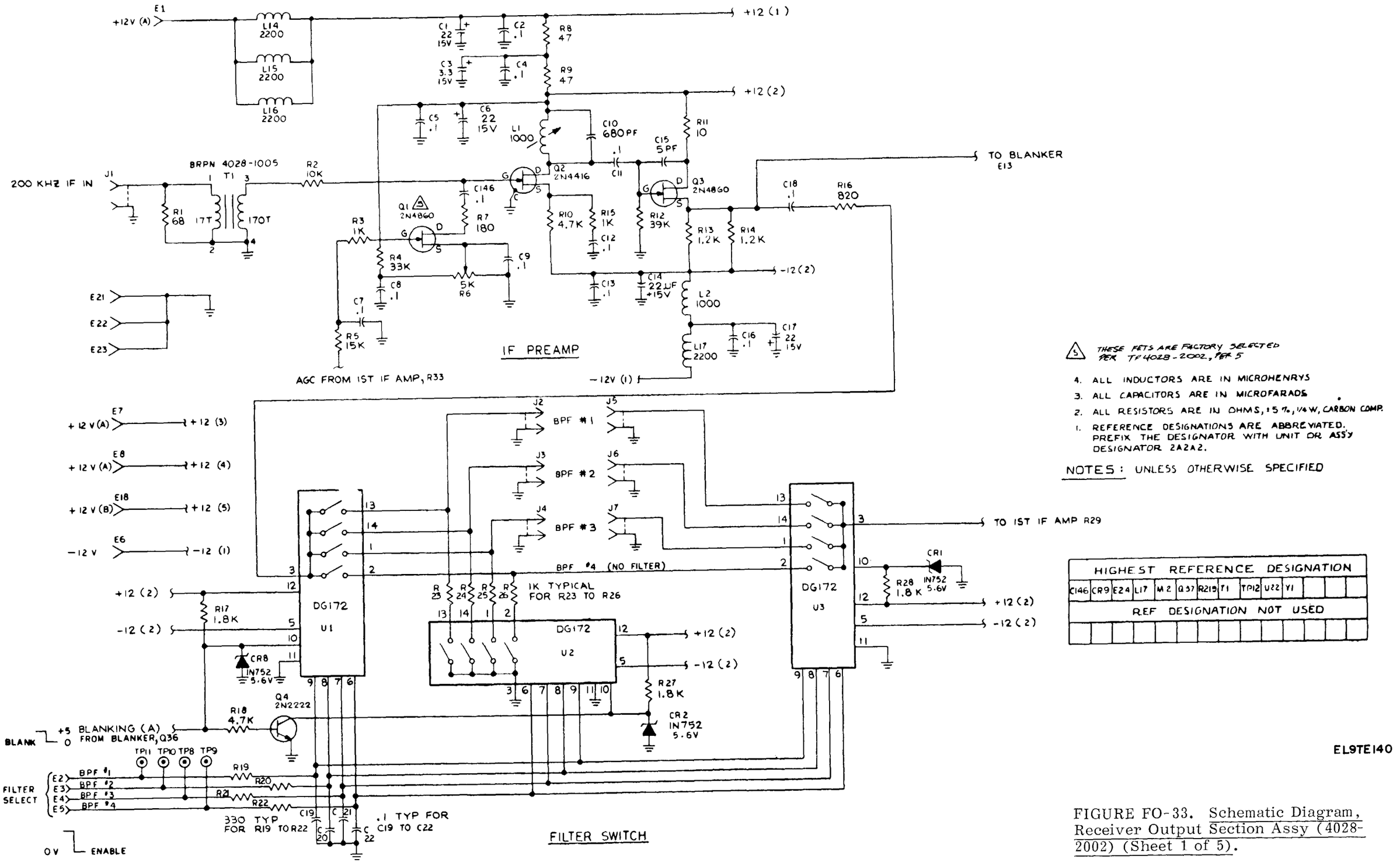
5 COMPONENTS SHOWN ARE LOADED FOR 4028-2001-1 ONLY.

4. ALL INDUCTORS ARE IN MICROHENRYS.
3. ALL CAPACITORS ARE IN MICROFARADS.
2. ALL RESISTORS ARE IN OHMS, 1/4W, ±5%.
1. REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX THE DESIGNATOR WITH UNIT OR ASSEMBLY DESIGNATOR 2A2A1.

NOTES: UNLESS OTHERWISE SPECIFIED.

EL9TE139

FIGURE FO-32. Schematic Diagram, Receiver Front End Assy (4028-2001) (Sheet 5 of 5).



S THESE FETS ARE FACTORY SELECTED PER TI 4028-2002, PAR 5

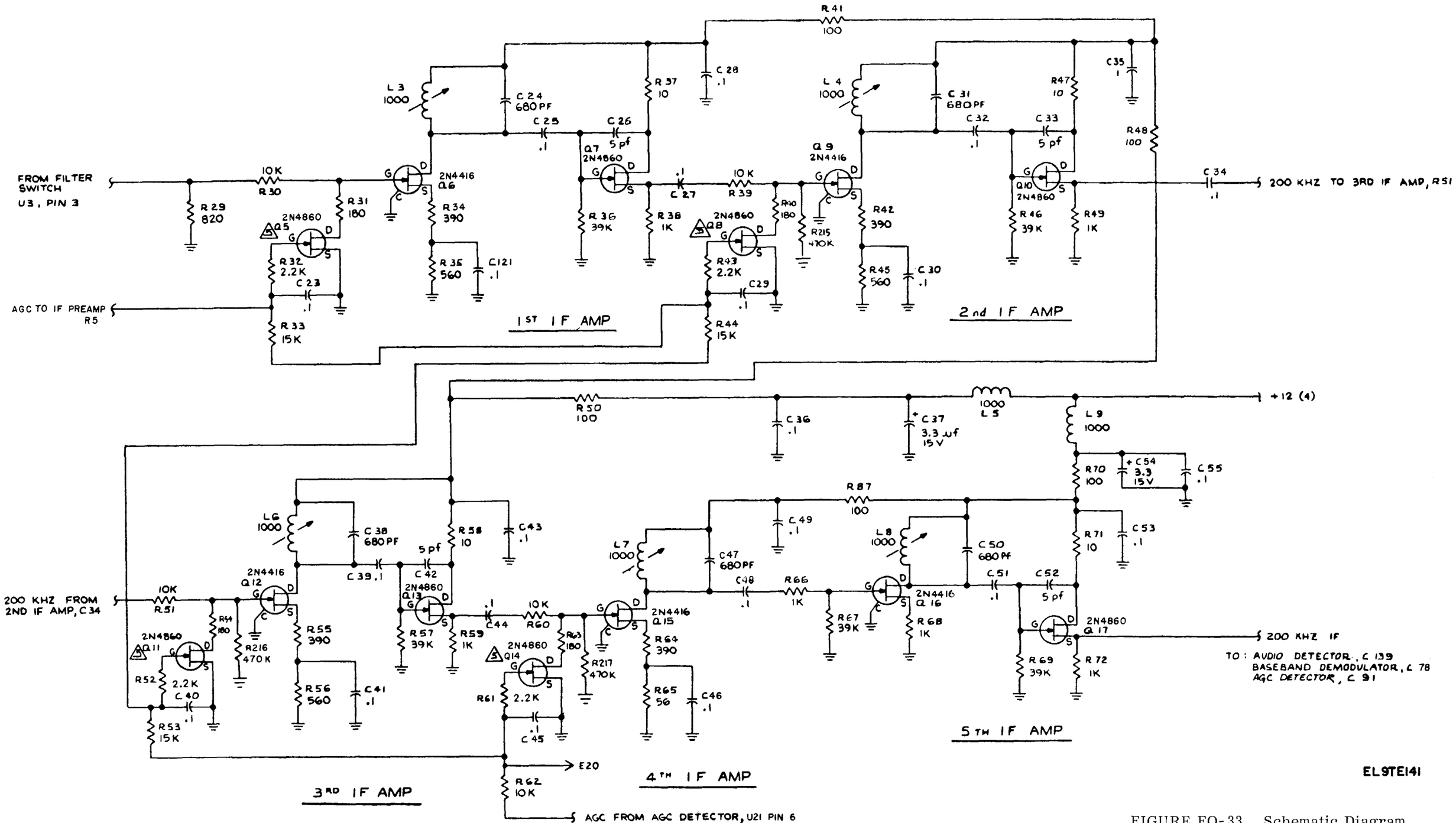
4. ALL INDUCTORS ARE IN MICROHENRYS
3. ALL CAPACITORS ARE IN MICROFARADS
2. ALL RESISTORS ARE IN OHMS, ±5%, 1/4W, CARBON COMP.
1. REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX THE DESIGNATOR WITH UNIT OR ASS'Y DESIGNATOR 2A2A2.

NOTES: UNLESS OTHERWISE SPECIFIED

HIGHEST REFERENCE DESIGNATION												
C146	CR9	E24	L17	M2	Q37	R219	T1	TP12	U22	Y1		
REF DESIGNATION NOT USED												

EL9TE140

FIGURE FO-33. Schematic Diagram, Receiver Output Section Assy (4028-2002) (Sheet 1 of 5).



EL9TE141

FIGURE FO-33. Schematic Diagram, Receiver Output Section Assy (4028-2002) (Sheet 2 of 5).

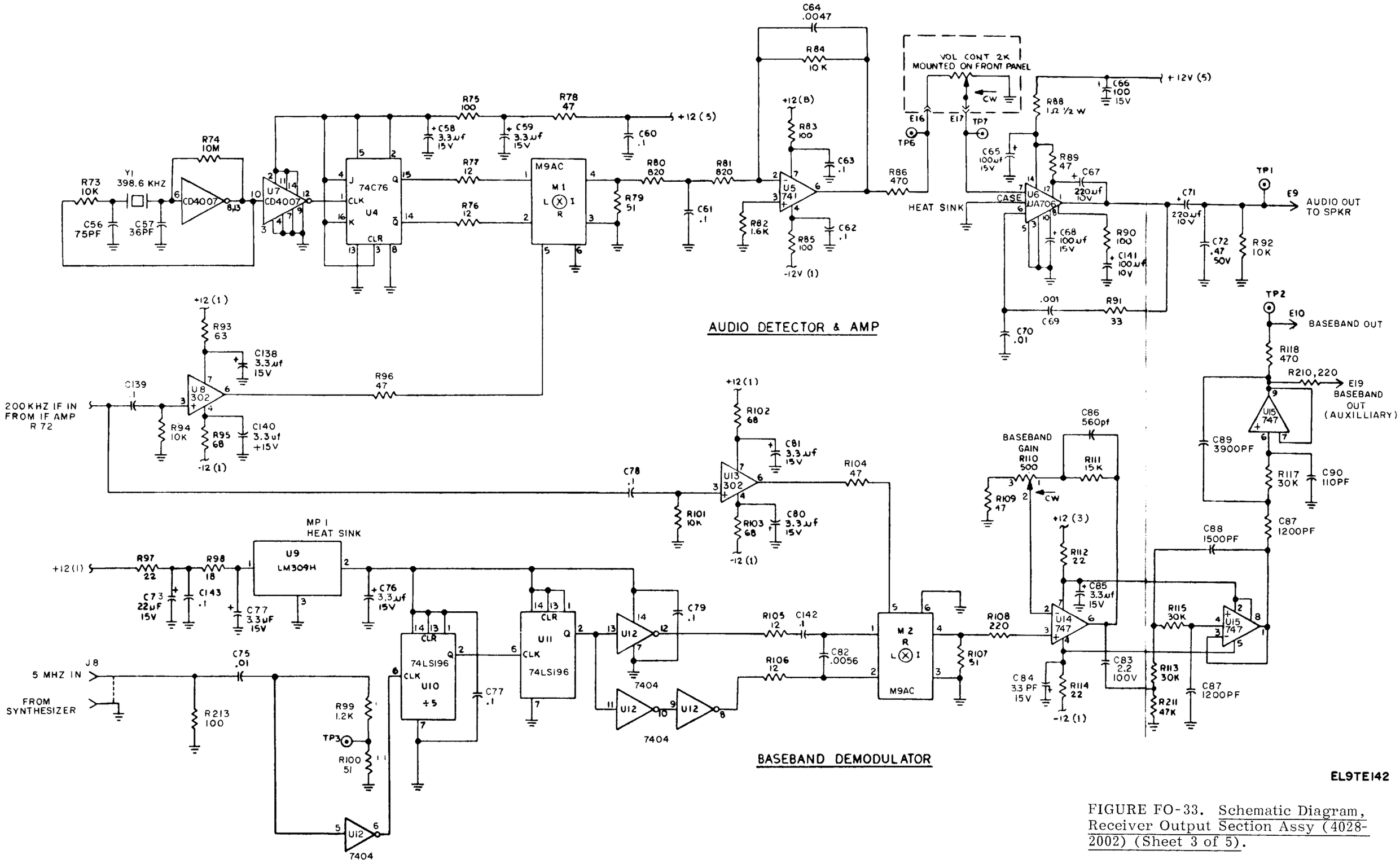
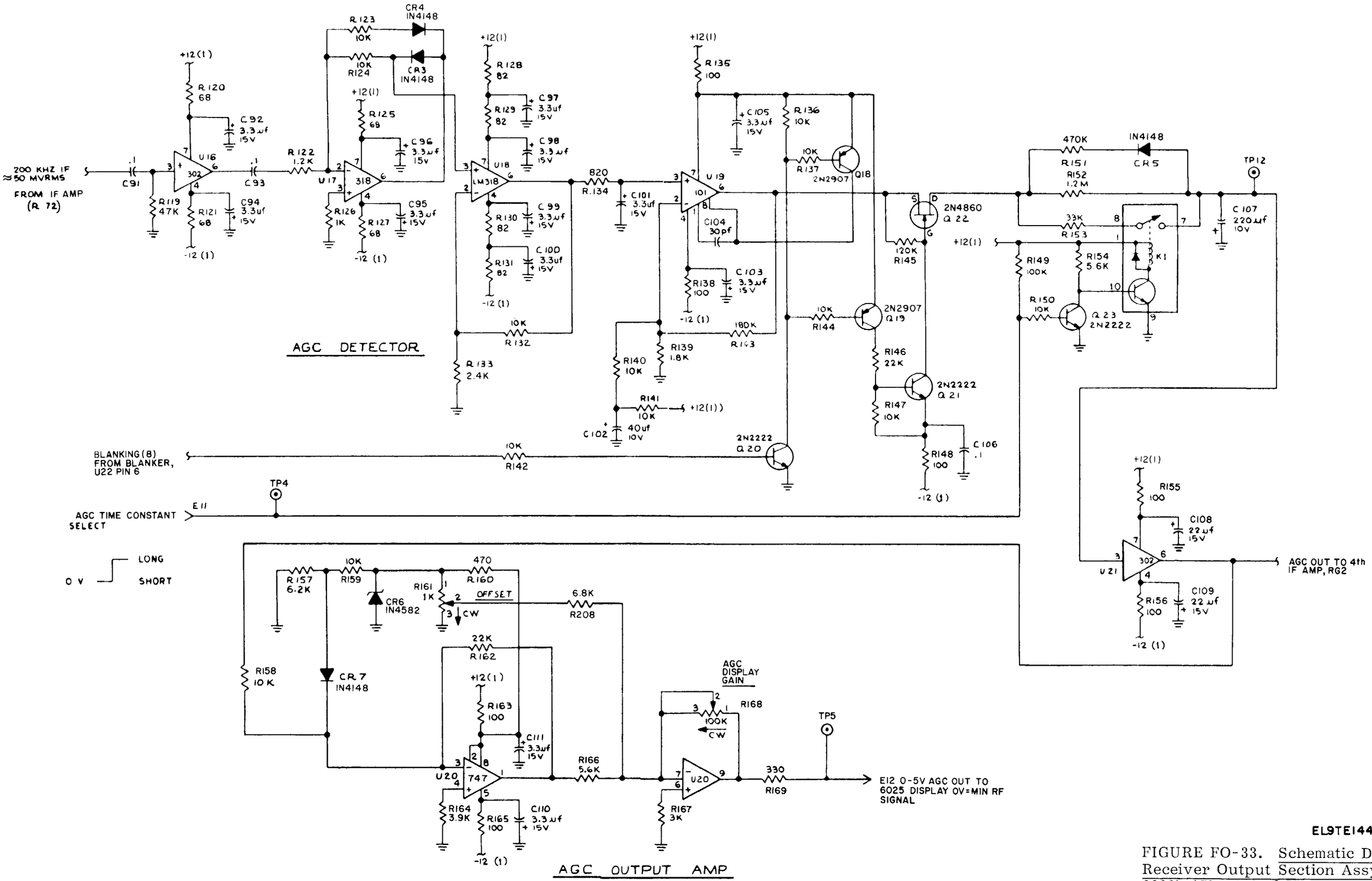


FIGURE FO-33. Schematic Diagram, Receiver Output Section Assy (4028-2002) (Sheet 3 of 5).



EL9TE144

FIGURE FO-33. Schematic Diagram, Receiver Output Section Assy (4028-2002) (Sheet 4 of 5).

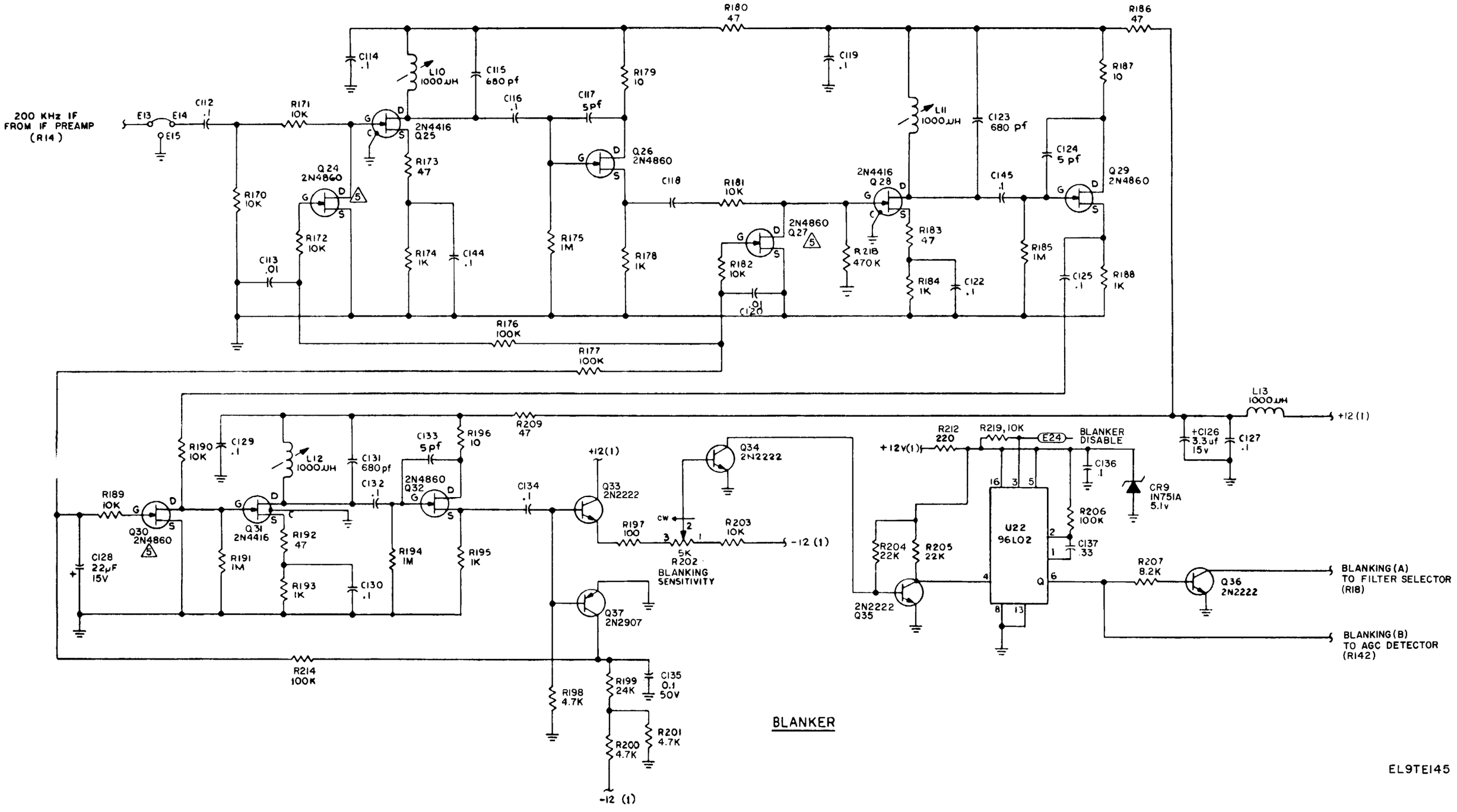
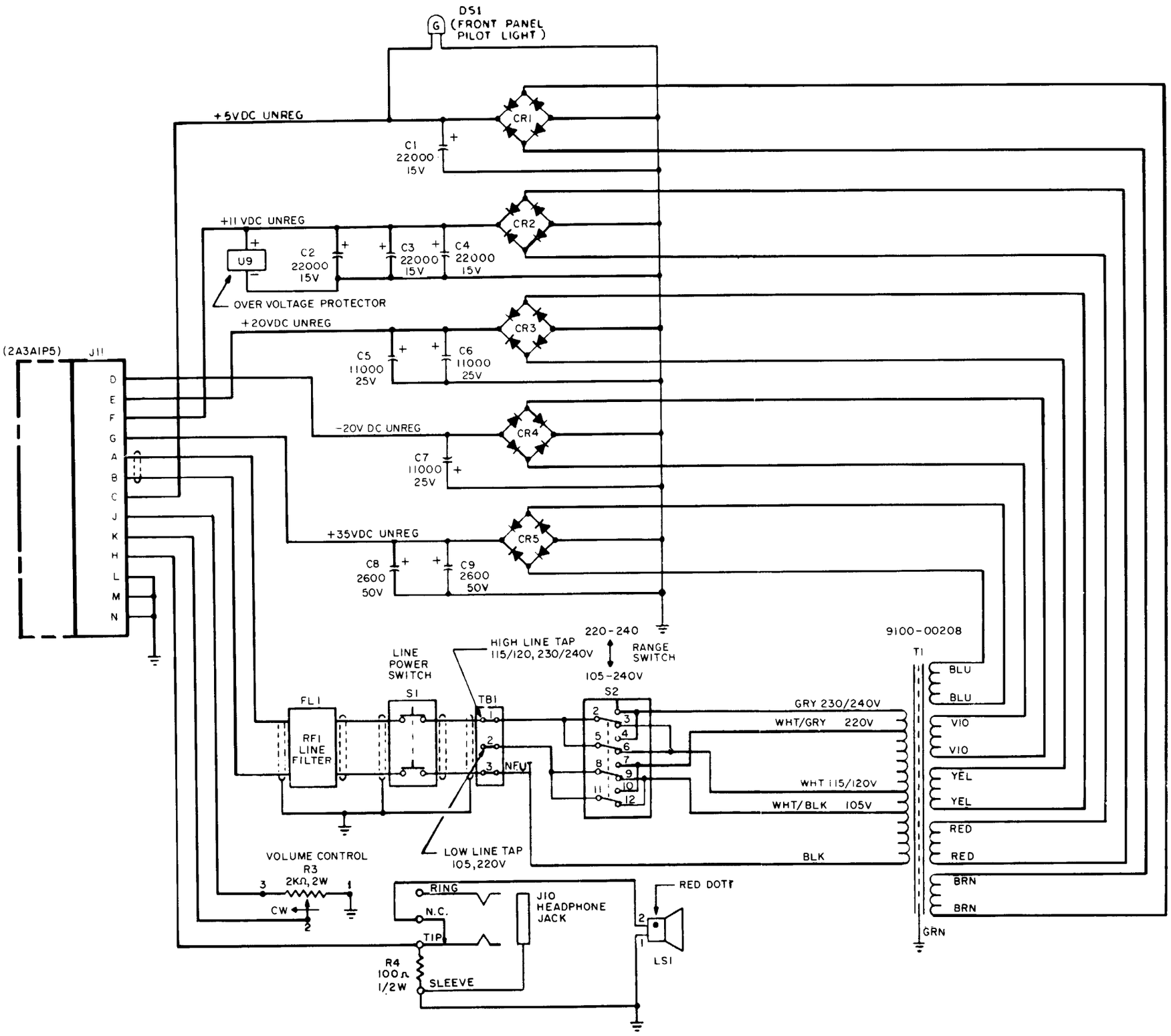


FIGURE FO-33. Schematic Diagram, Receiver Output Section Assy (4028-2002) (Sheet 5 of 5).



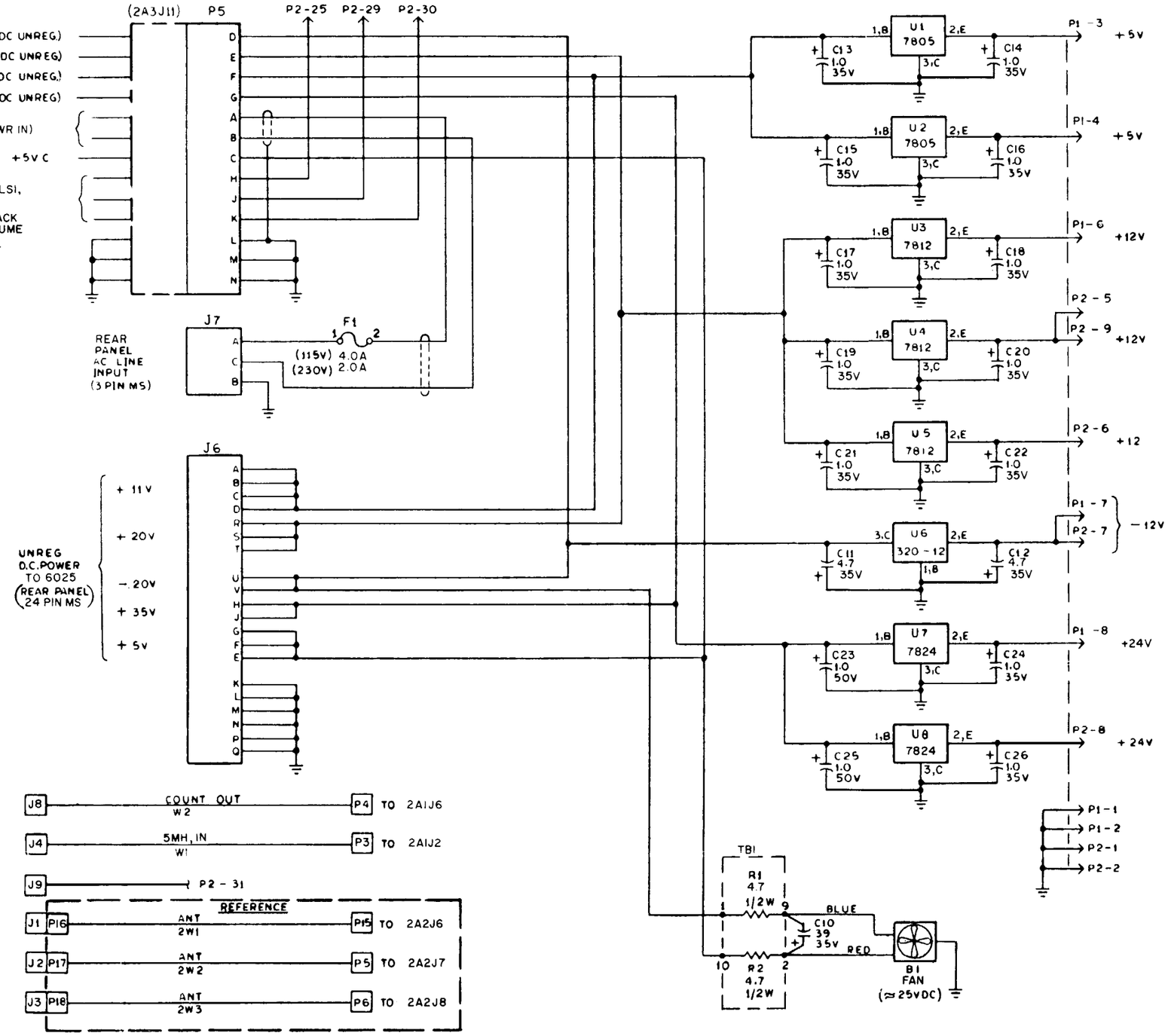
4. POWER SUPPLY SHOWN IN 115/120V SETTING
3. CR1 TO CR5 ARE MDA 990-3
2. ALL CAPACITORS ARE IN MICROFARADS.
1. REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX THE DESIGNATOR WITH UNIT OR ASSY DESIGNATOR 2 A 3.

NOTES: UNLESS OTHERWISE SPECIFIED.

HIGHEST REFERENCE DESIGNATION								
C9	CR5	DS1	FL1	J11	S2	T1	TB1	R4
LS1	U9							
REF DESIGNATION NOT USED								
	U1-U8			J1-J9				R1, R2

EL9TE146

FIGURE FO-34. Schematic Diagram, Power Supply of 4028 HF Receiver (Sheet 1 of 2).



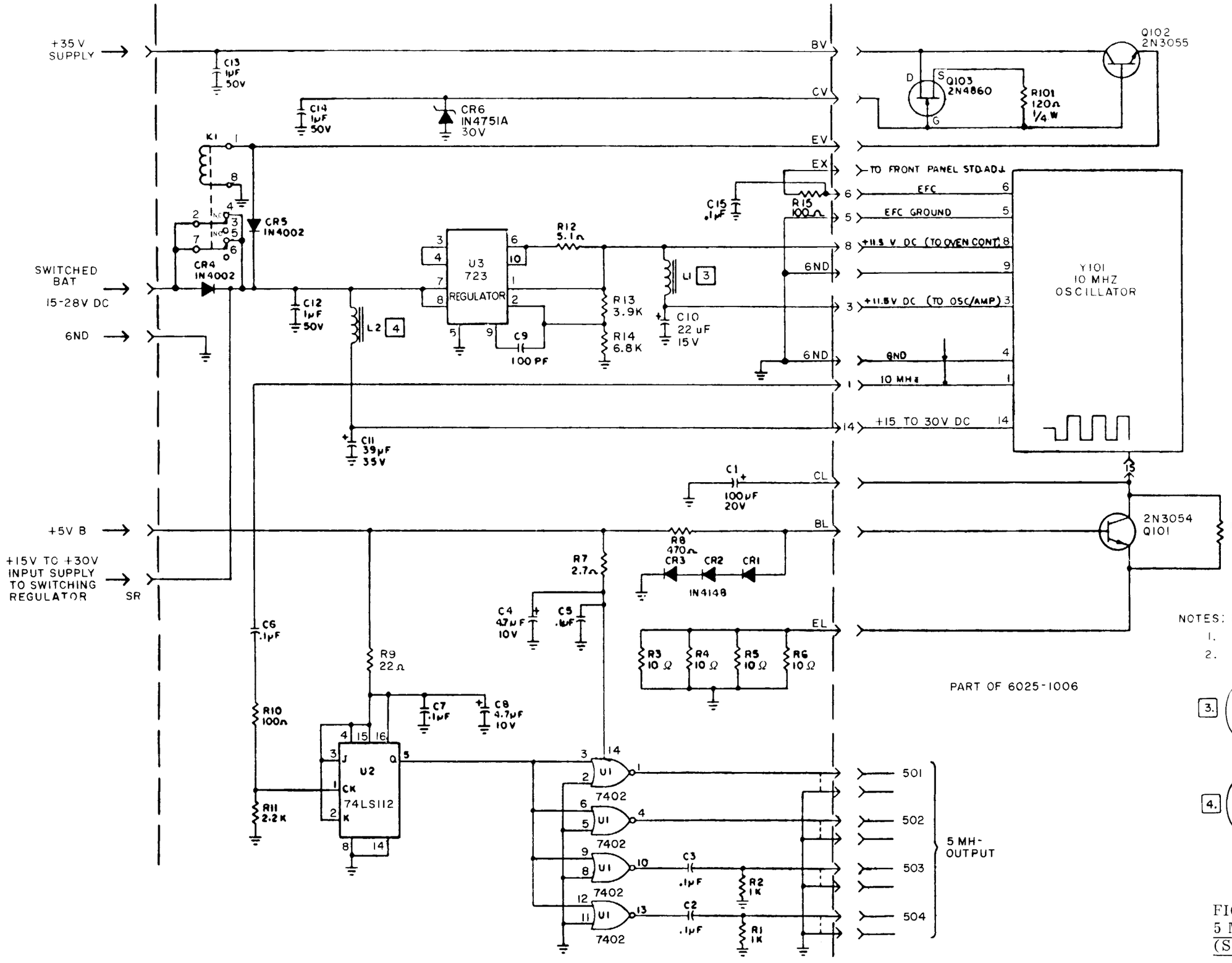
5. ALL REGULATORS MOUNTED ON REAR PANEL HEAT SINK.
4. FOR P1, P2 AND J5 CONNECTIONS SEE WIRING LIST.
3. ALL CAPACITORS ARE IN MICROFARADS.
2. ALL RESISTORS ARE IN OHMS.
1. PARTIAL REFERANCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSY DESIGNATION 283AI

NOTES: UNLESS OTHERWISE SPECIFIED.

HIGHEST REFERENCE DESIGNATION						
B1	C26	R2	U8	F1	J9	P5
REF DESIGNATIONS NOT USED						
	C1 - C9					

EL9TEI47

FIGURE FO-34. Schematic Diagram, Power Supply of 4028 HF Receiver (Sheet 2 of 2).



HIGHEST REFERENCE DESIGNATION						
C15	CR6	L2	Q-	R15	U3	K1
REF DESIGNATION NOT USED						

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE IN OHMS ±5%, 1/4, CARBON COMP.
2. ALL CAPACITORS ARE IN MICROFARADS.

L1 = 6025-3063

3. (70 TURNS #22 WIRE ON 9110-0092 BOBBIN 9110-0091 CORE)

L2 = 6025-3064

4. (40 TURNS #20 WIRE ON 9110-0092 BOBBIN 9110-0091 CORE.)

PART OF 6025-1006

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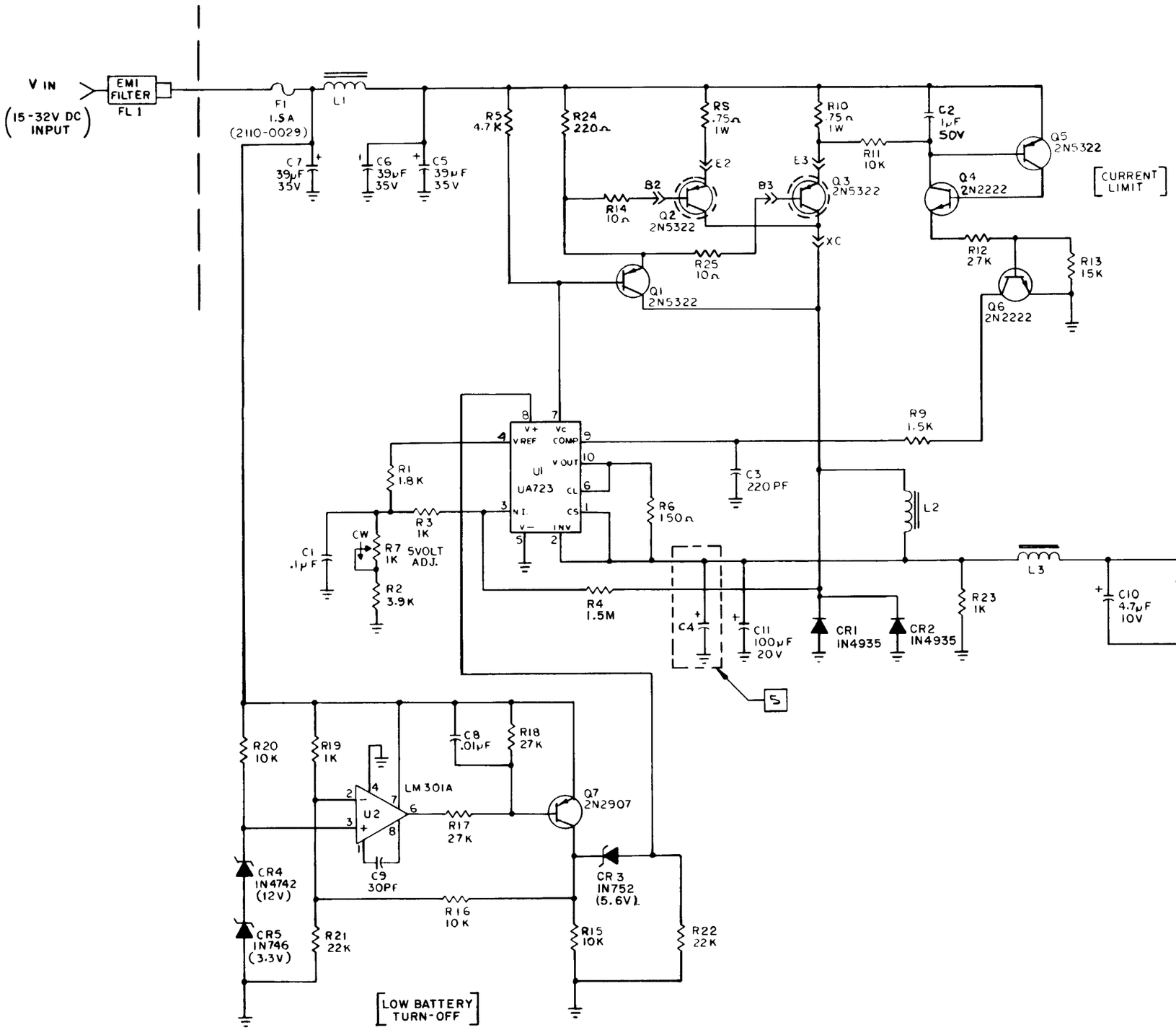
FIGURE FO-35. Schematic Diagram, 5 MHz Dist Amplifier Assy (6025-2008) (S/N 400100 and before).



NOTES: UNLESS OTHERWISE SPECIFIED

1. L1 - L3 9110-0092 BOBBIN, 9110-0091 CORE.
2. FL1, FL2 9100-0022.
3. L1 = 6025-3063 (≈5mHy, 70TURNS)
   L2 = 6025-3097 (≈2mHy, 40 TURNS)
   L3 = 6025-3064 (≈2mHy, 40 TURNS)
4. Q2 & Q3 MOUNTED OFF BOARD ON CHASSIS.
5. C4 IS NOT LOADED IN ASSY 6025-2009

HIGHEST REFERENCE DESIGNATION								
C11	CR6	F1	L3	Q7	R25	U2		
REF DESIGNATION NOT USED								

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FIGURE FO-36. Schematic Diagram, +5 Volt Switching Regulator Assy (6025-2009) (S/N 400100 and before).

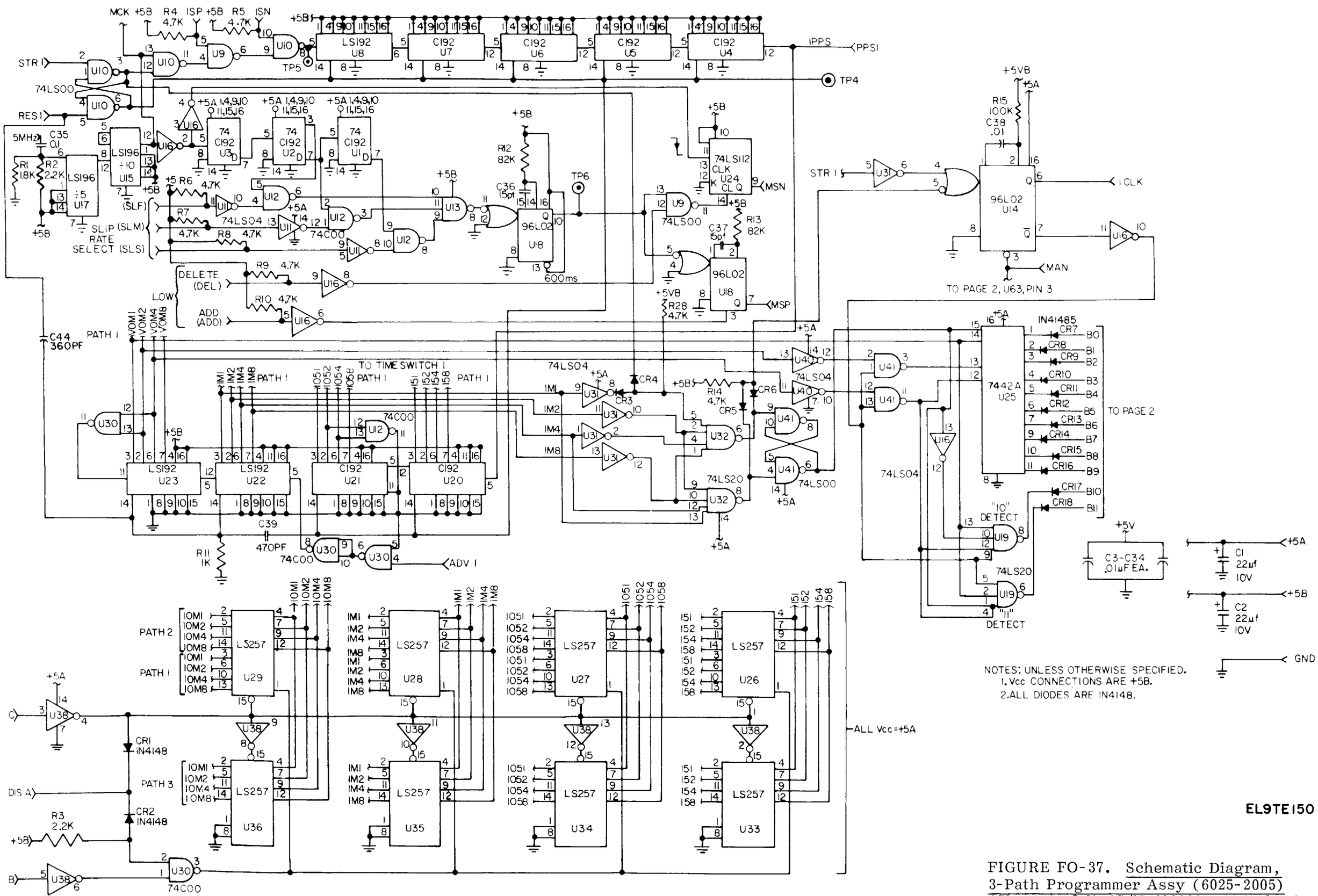
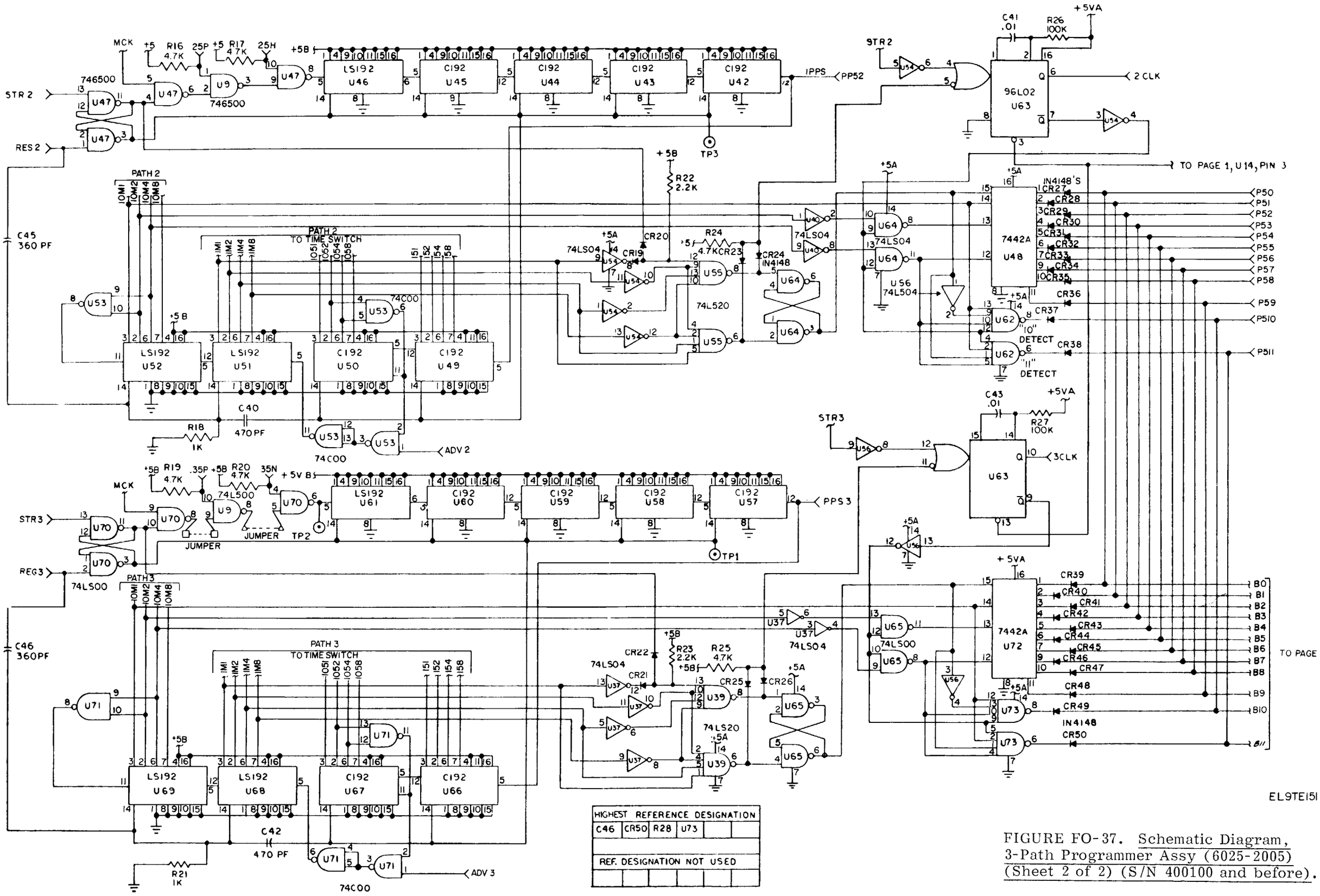
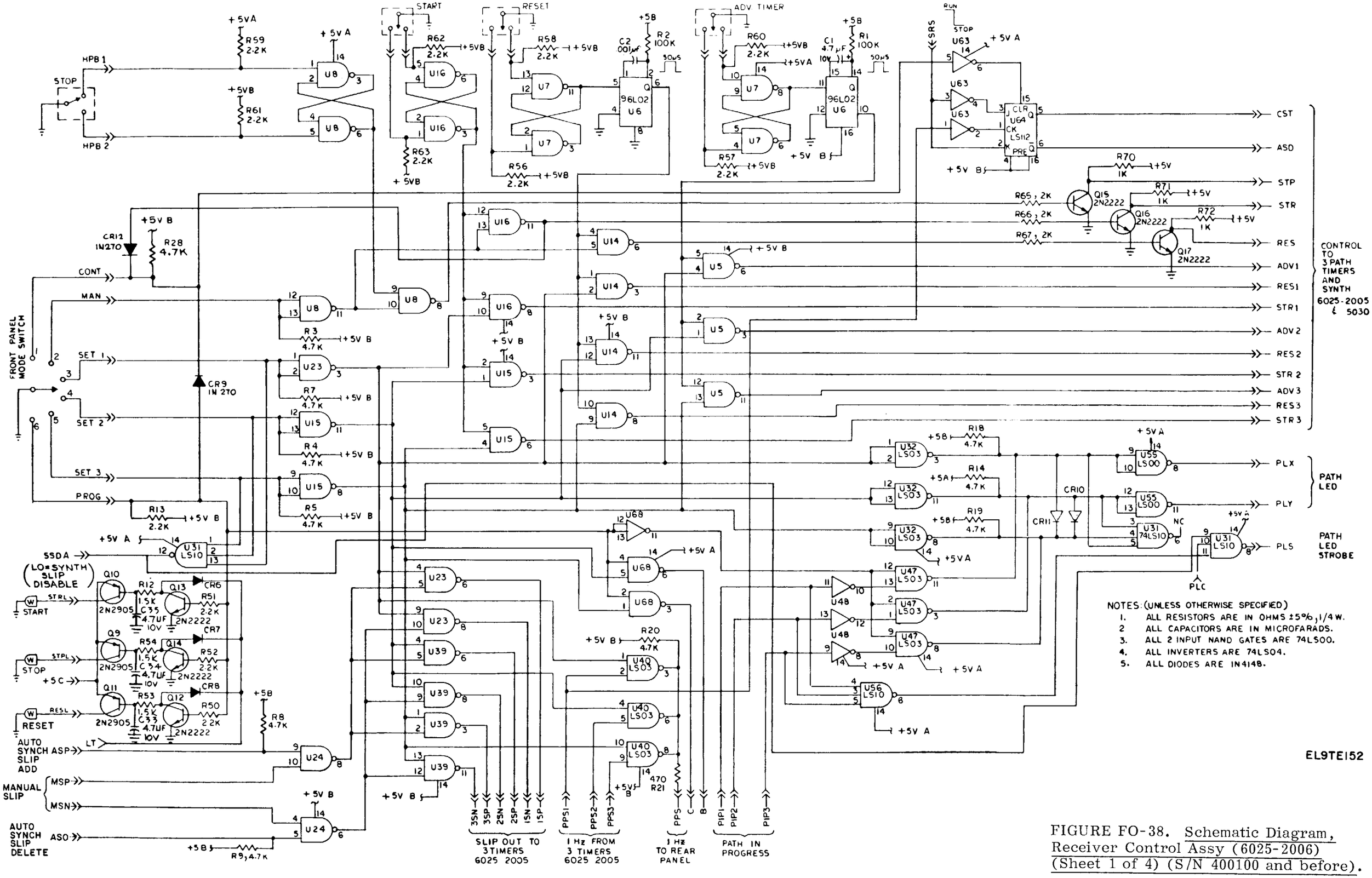


FIGURE FO-37. Schematic Diagram, 3-Path Programmer Assy (6025-2005) (Sheet 1 of 2) (S/N 400100 and before).



HIGHEST REFERENCE DESIGNATION					
C46	CR50	R28	U73		
REF. DESIGNATION NOT USED					

FIGURE FO-37. Schematic Diagram, 3-Path Programmer Assy (6025-2005) (Sheet 2 of 2) (S/N 400100 and before).



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. ALL RESISTORS ARE IN OHMS ±5%, 1/4 W.
2. ALL CAPACITORS ARE IN MICROFARADS.
3. ALL 2 INPUT NAND GATES ARE 74LS00.
4. ALL INVERTERS ARE 74LS04.
5. ALL DIODES ARE IN4148.

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FIGURE FO-38. Schematic Diagram, Receiver Control Assy (6025-2006) (Sheet 1 of 4) (S/N 400100 and before).

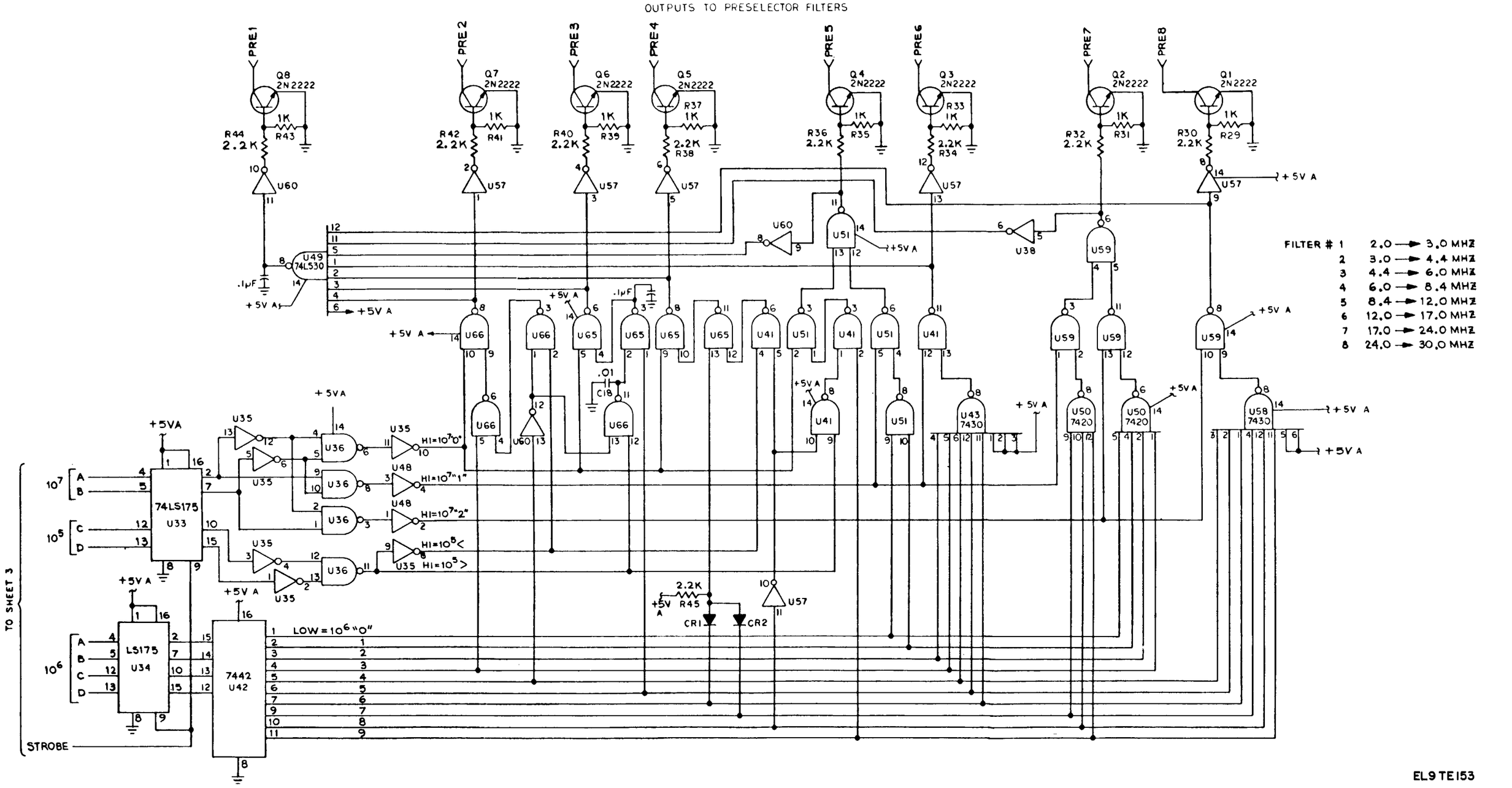

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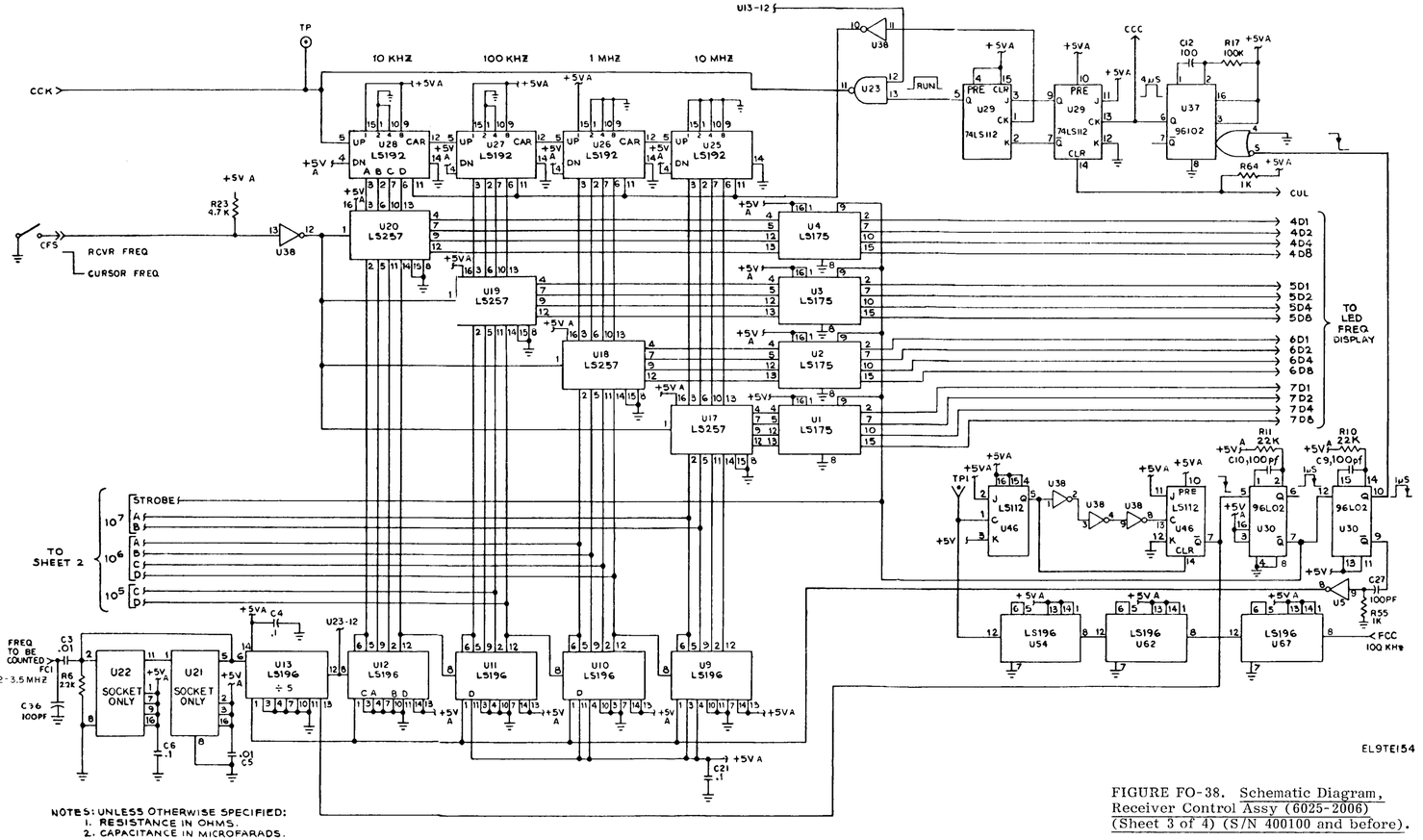
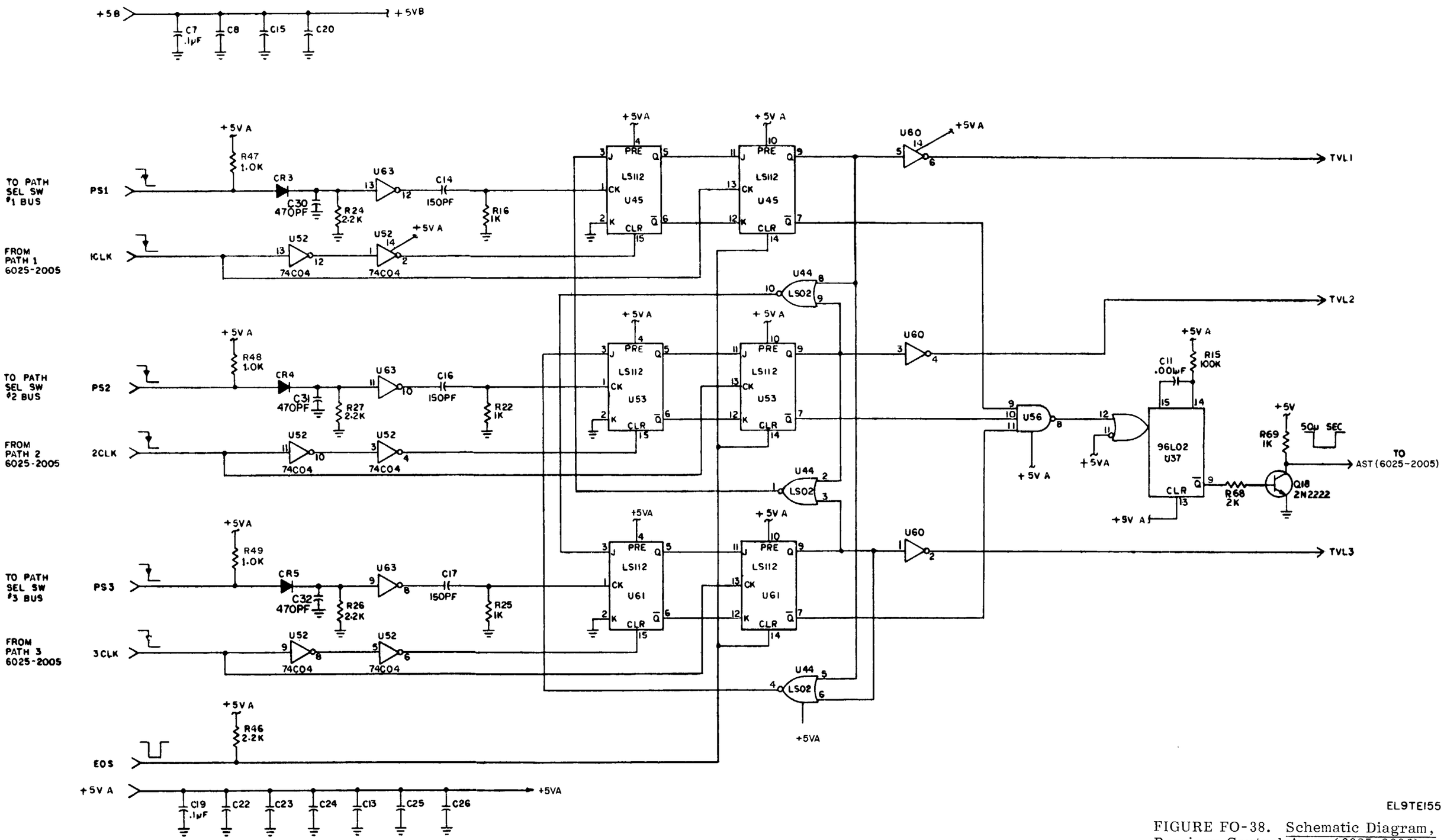
FIGURE FO-38. Schematic Diagram, Receiver Control Assy (6025-2006) (Sheet 2 of 4) (S/N 400100 and before).



NOTES: UNLESS OTHERWISE SPECIFIED:
1. RESISTANCE IN OHMS.
2. CAPACITANCE IN MICROFARADS.

FIGURE FO-38. Schematic Diagram, Receiver Control Assy (6025-2006) (Sheet 3 of 4) (S/N 400100 and before).



EL9TE155

FIGURE FO-38. Schematic Diagram, Receiver Control Assy (6025-2006) (Sheet 4 of 4) (S/N 400100 and before).